

AW87390FCR Application Design Guide

Contents

1	AW87390FCR INTRODUCTION.....	2
2	AW87390FCR INTRODUCTION TO APPLICATION SCENARIOS	4
3	AW87390FCR TYPICAL APPLICATION DIAGRAM OF HEADPHONE INPUT	5
4	AW87390FCR TYPICAL APPLICATION DIAGRAM OF LINEOUT INPUT	8
5	AW87390FCR STEREO APPLICATION SCHEMATIC.....	11
6	POWER NETWORK DESIGN NOTES	14
7	AW87390FCR I2C DEVICE ADDRESS SELECTION	19
8	AW87390FCR COMPONENT SELECTION.....	20
9	AW87390FCR PCB REFERENCE LAYOUT	23
10	AW87390FCR PCB REFERENCE ROUTING	24

1 AW87390FCR INTRODUCTION

AW87390FCR integrate Awinic's proprietary Triple-Level Triple-Rate AGC sound effect algorithm to effectively eliminate noise in music playback and improve sound quality and volume. The AW87390FCR integrates high-voltage synchronous adaptive boost, with an efficiency of up to 81%, while significantly improving the dynamic range of music. AW87390FCR noise is as low as 9.5uV, with up to 102dB signal-to-noise ratio, 0.008% ultra-low distortion and unique Triple-Level Triple-Rate technology, bringing high-quality music enjoyment.

AW87390FCR support Speaker&Receiver 2-in-1 mode application. In Receiver application, the output noise is as low as 9.5uV. At the same time, Class D Receiver has high PSRR, which can effectively suppress TDD-noise.

The AW87390FCR controls the registers through the I2C interface, and the register parameters include output voltage, PA gain, Triple-Level Triple-Rate AGC parameters, etc.

The AW87390FCR has built-in over-current protection, over-temperature protection and short-circuit protection functions to effectively protect the chip.

The AW87390FCR use FCQFN 2.5mmX2.0mmX0.55mm-16L package.

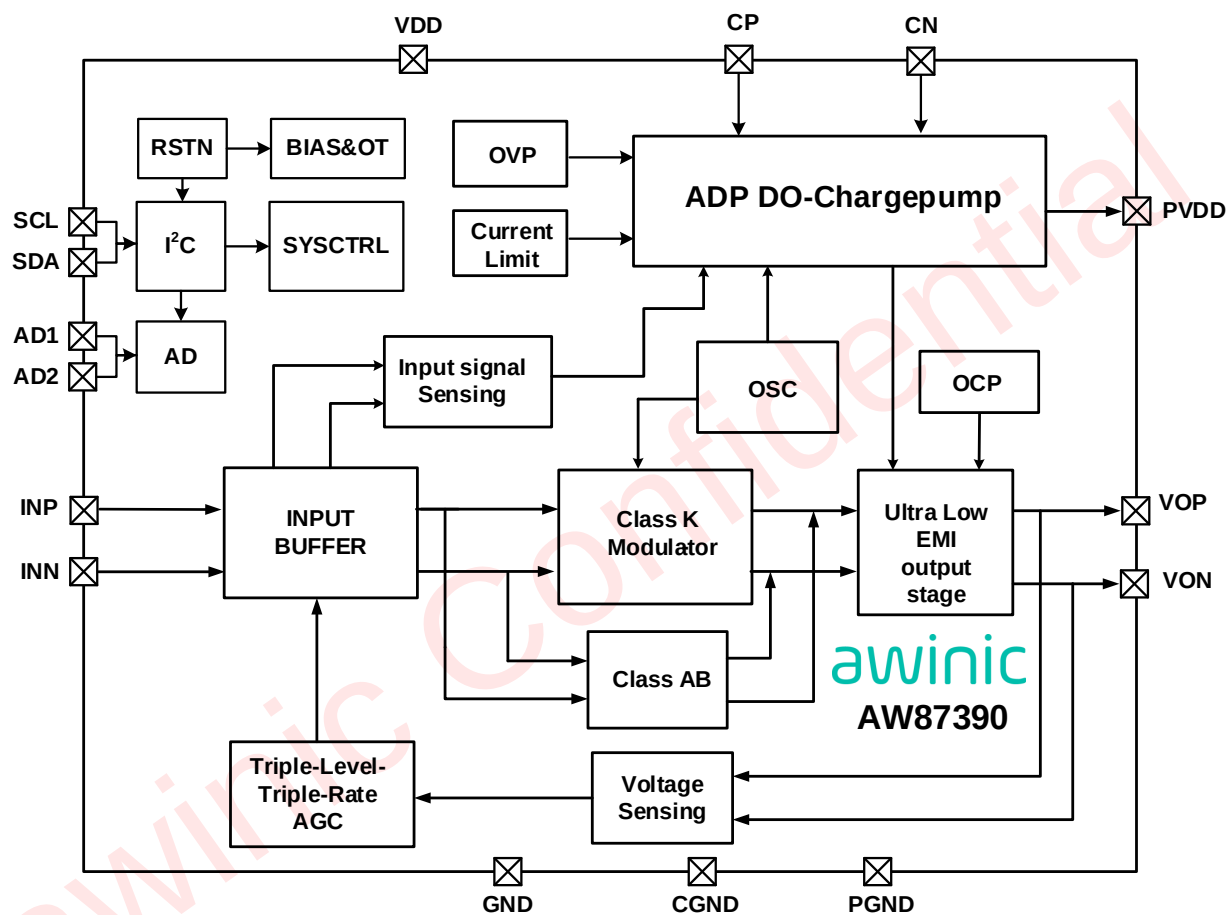


Figure 1 AW87390FCR Functional Diagram

2 AW87390FCR INTRODUCTION TO APPLICATION SCENARIOS

AW87390FCR is a high-efficiency, high-PSRR, low-noise, constant high-volume sixth-generation class-K music amplifier specially developed to improve the dynamic range of music output and improve the overall sound quality. It is commonly used in mobile phones and tablet computers.



Mobile phone



Tablet computers



Smart speaker

Figure 2 AW87390FCR Application scenarios

3 AW87390FCR TYPICAL APPLICATION DIAGRAM OF HEADPHONE INPUT

1. The red marked is the high current flow path, please pay attention to the layout;
2. The green marked is the audio signal input, generally HPH_L and HPH_REF take the pseudo-differential line to the codec of the platform together;
3. The PVDD capacitor should be an X5R capacitor with a withstand voltage value of more than 16V, and the effective capacitance value should not be less than 3uF under 8V voltage;
4. VDD needs a 10uF capacitor and a 0.1uF capacitor for decoupling;
5. SDA and SCL need to be pulled up to the platform logic level through pull-up resistors. AD1 and AD2 are the chip address selection pins. The default pull-down of the two pins is 0x58. Please refer to the manual to select the appropriate address.

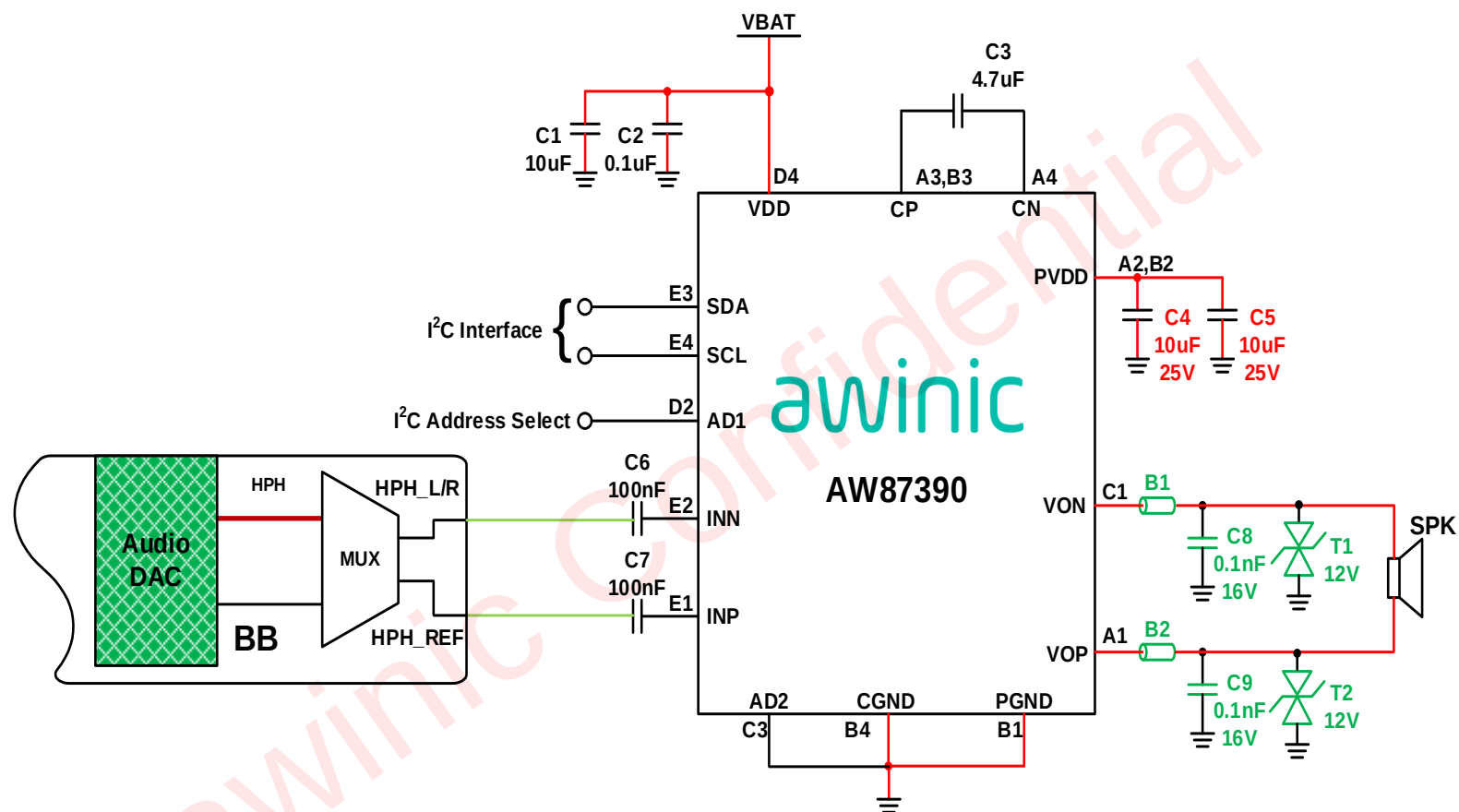


Figure 3 AW87390FCR application diagram of headphone input

Device Reference Notes

Components	Description	Typical Specification
C1	VBAT filter capacitor	10uF/6.3V(VBAT ≤ 4.4V)
C2	VBAT filter capacitor	0.1uF/6.3V(VBAT ≤ 4.4V)
C3	Changepump Converter	4.7uF/10V
C4,C5	Changepump Converter output Capacitors	Capacitance is 2 x 10uF/25V
C6,C7	Blocking Capacitors	Capacitance is 2 x 100nF/6.3V
C8,C9	EMI Filter Capacitors(optional)	The typical value is 0.1nF.Must use B1 and B2 if C8 and C9 are used.
B1,B2	EMI Filter Beads(optional)	Beads,120ohm at 100MHz,current rating >1.2A.
T1,T2	TVS for VOP.VON	12V

Table1 AW87390FCR application diagram of headphone input BOM

4 AW87390FCR TYPICAL APPLICATION DIAGRAM OF LINEOUT INPUT

1. The red marked is the high current flow path, please pay attention to the layout;
2. The green marked is the audio signal input, and OUTP and OUTN take the differential line together to the codec of the platform;
3. The PVDD capacitor should be an X5R capacitor with a withstand voltage value of more than 16V, and the effective capacitance value should not be less than 3uF under 8V voltage;
4. VDD needs a 10uF capacitor and 0.1uF capacitor for decoupling.

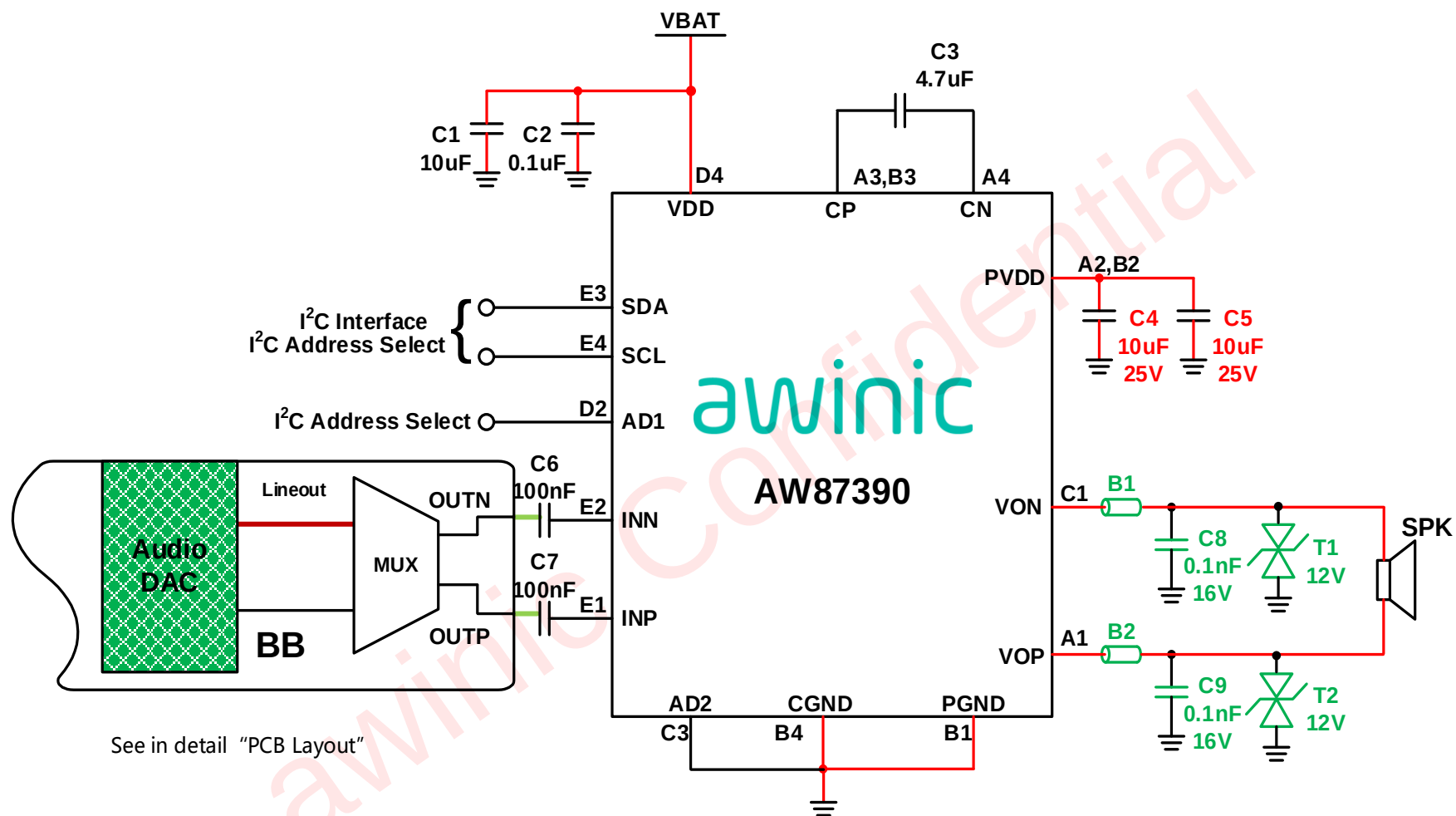


Figure 4 AW87390FCR application diagram of Lineout input

Device Reference Notes

Components	Description	Typical Specification
C1	VBAT filter capacitor	10uF/6.3V(VBAT ≤ 4.4V)
C2	VBAT filter capacitor	0.1uF/6.3V(VBAT ≤ 4.4V)
C3	Chargepump Converter	4.7uF/10V
C4,C5	Chargepump Converter output Capacitors	Capacitance is 2 x 10uF/25V
C6,C7	Blocking Capacitors	Capacitance is 2 x 100nF/6.3V
C8,C9	EMI Filter Capacitors(optional)	The typical value is 0.1nF.Must use B1 and B2 if C8 and C9 are used.
B1,B2	EMI Filter Beads(optional)	Beads,120ohm at 100MHz,current rating >1.2A.
T1,T2	TVS for VOP.VON	12V

Table2 AW87390FCR application diagram of Lineout input BOM

5 AW87390FCR STEREO APPLICATION SCHEMATIC

1. The red marked is the high current flow path, please pay attention to the layout;
2. The green marked is the audio signal input, and OUTP and OUTN take the differential line together to the codec of the platform;
3. The PVDD capacitor should be an X5R capacitor with a withstand voltage value of more than 16V, and the effective capacitance value should not be less than 3uF under 8V voltage;
4. VDD needs a 10uF capacitor and a 0.1uF capacitor for decoupling;
5. For single-ended stereo applications, the left and right channel audio PA inputs should be connected in the same way as the left and right channel outputs on the platform side. For example, when INN is selected as the input pin, both audio PAs use INN as the input pin to connect to the left and right channels of the platform. To avoid the sound phase output of the left and right channels being reversed, the sound effect will be problematic. The reference connection method is shown in Figure 5.

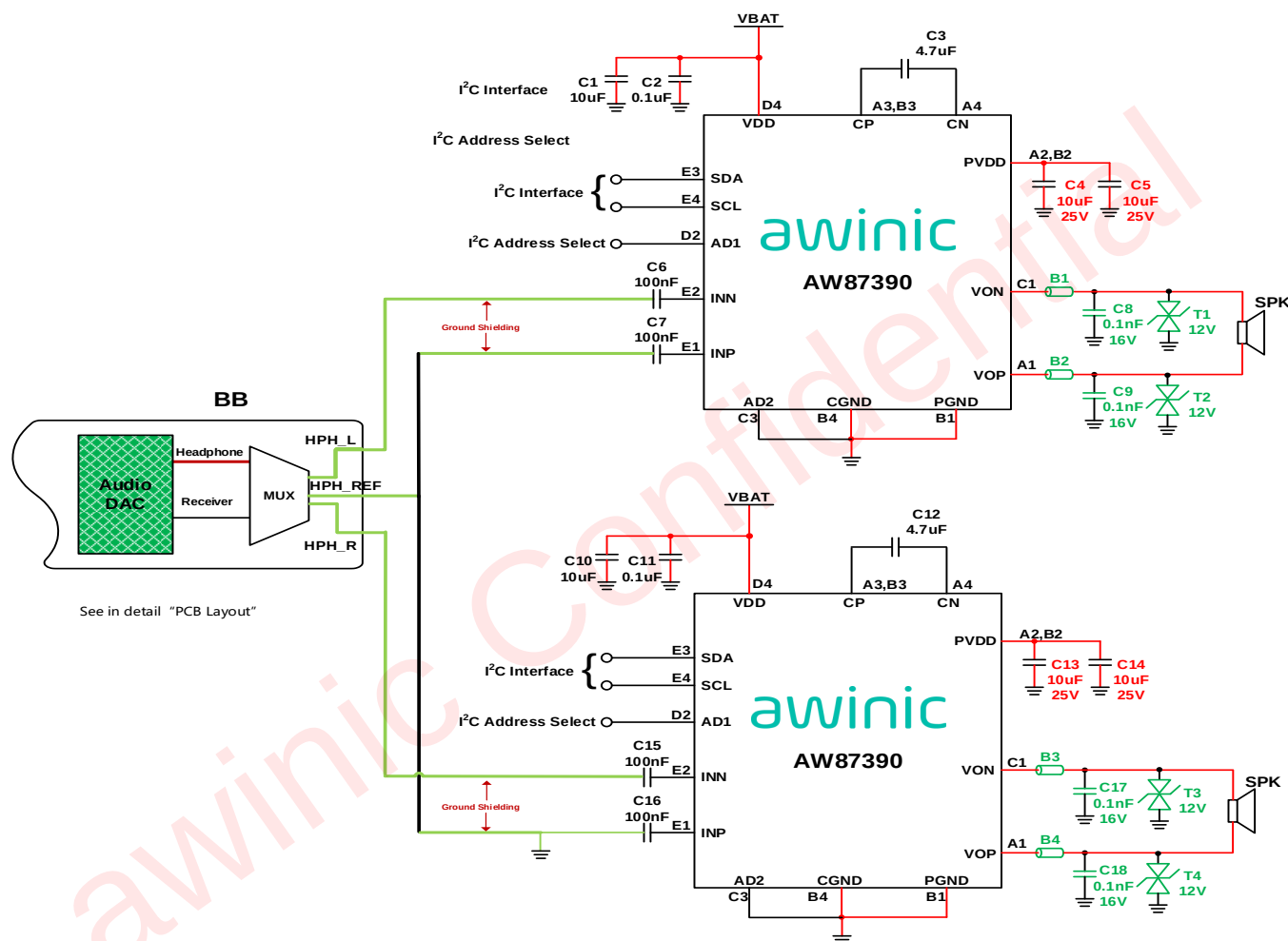


Figure 5 AW87390FCR Stereo Application Reference Schematic

Device Reference Notes

Components	Description	Typical Specification
C1,C10	VBAT filter capacitor	10uF/6.3V(VBAT ≤ 4.4V)
C2,C11	VBAT filter capacitor	0.1uF/6.3V(VBAT ≤ 4.4V)
C3,C12	Chargepump Converter	4.7uF/10V
C4,C5,C13,C14	Chargepump Converter output Capacitors	Capacitance is 4 x 10uF/25V
C6,C7,C15,C16	Blocking Capacitors	Capacitance is 4 x 100nF/6.3V
C8,C9,C17,C18	EMI Filter Capacitors(optional)	The typical value is 0.1nF.Must use B1 and B2 if C8 and C9 are used.B3 and B4 same as above.
B1,B2,B3,B4	EMI Filter Beads(optional)	Beads,120ohm at 100MHz,current rating >1.2A.
T1,T2,T3,T4	TVS for VOP.VON	12V

Table3 AW87390FCR Stereo Application Reference Schematic BOM

6 POWER NETWORK DESIGN NOTES

1. Power Network Design Overview

Reasonable power network design and distribution play an important role in improving the performance of the power network. The selection of components, reasonable layout and wiring have an important impact on the surge noise protection and stability of the power network. The reference of the power network design diagram is as follows:

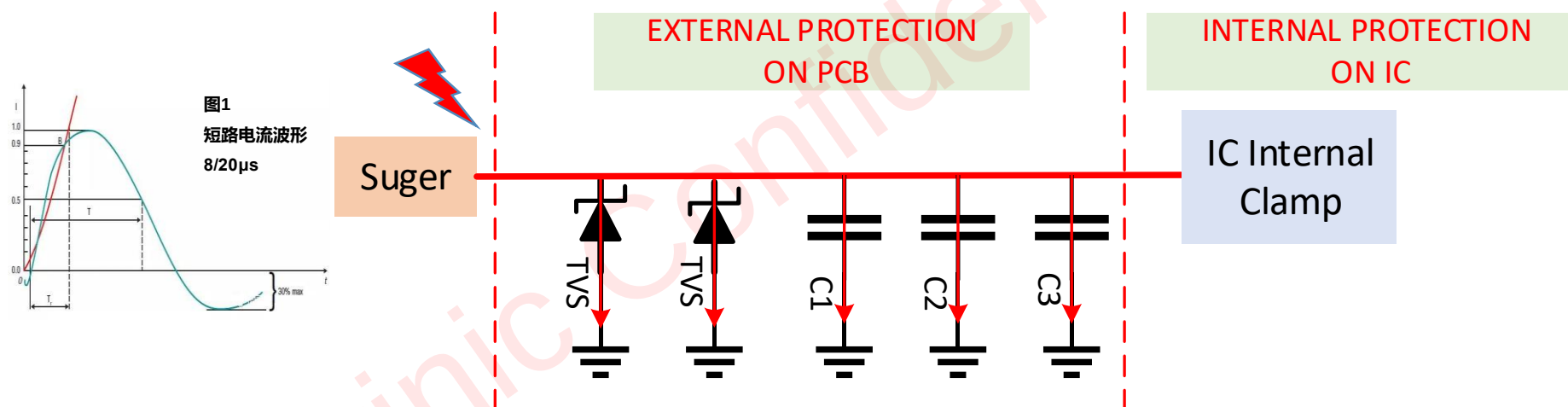


Figure 6 Power Network Reference Design Diagram

2. Power Network Design Recommendations

- 1) The principle of protection first and then filtering. For ports with both filtering and protection circuits, the protection devices

should be used to suppress overvoltage and overcurrent before filtering.

2) The TVS tube should be placed as close as possible to the external port, try to be on the same layer as the power network, and avoid changing layers as much as possible.

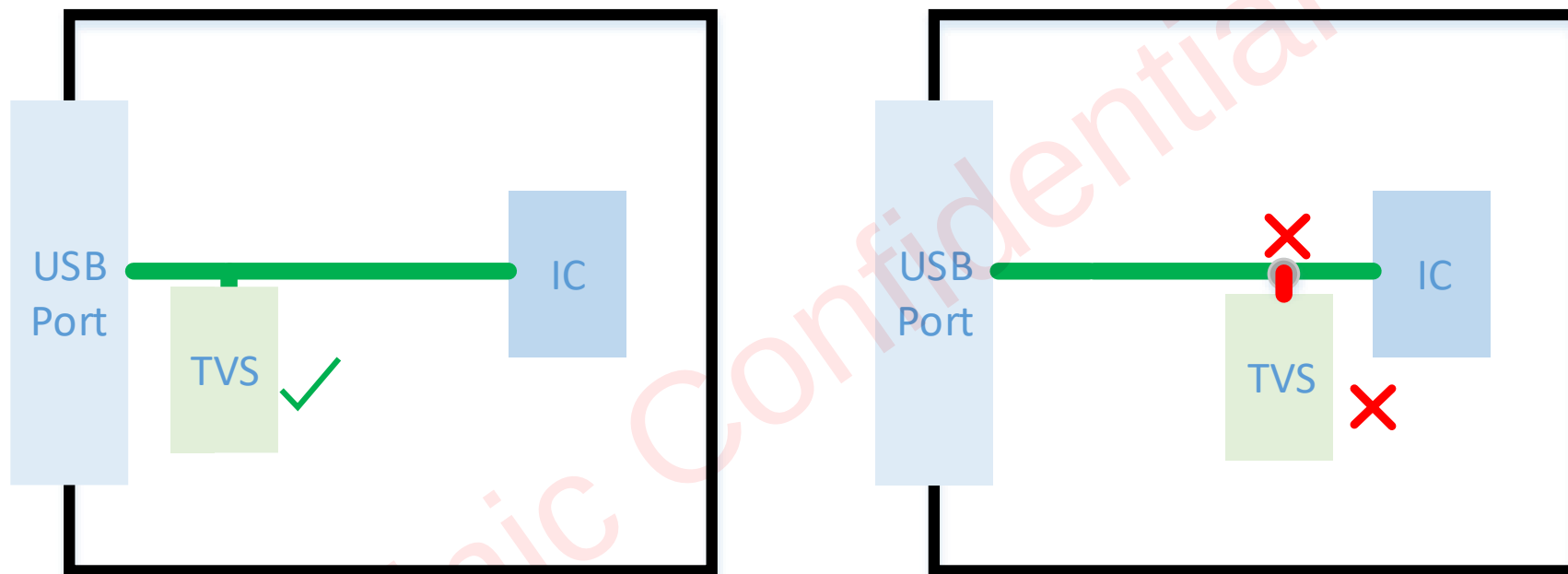


Figure 7 Place the position close to the external port and avoid changing layers

3) The protective device traces should be short and thick with reliable grounding to minimize the equivalent inductance caused by the traces and the clamp voltage bounce caused by unreliable grounding.

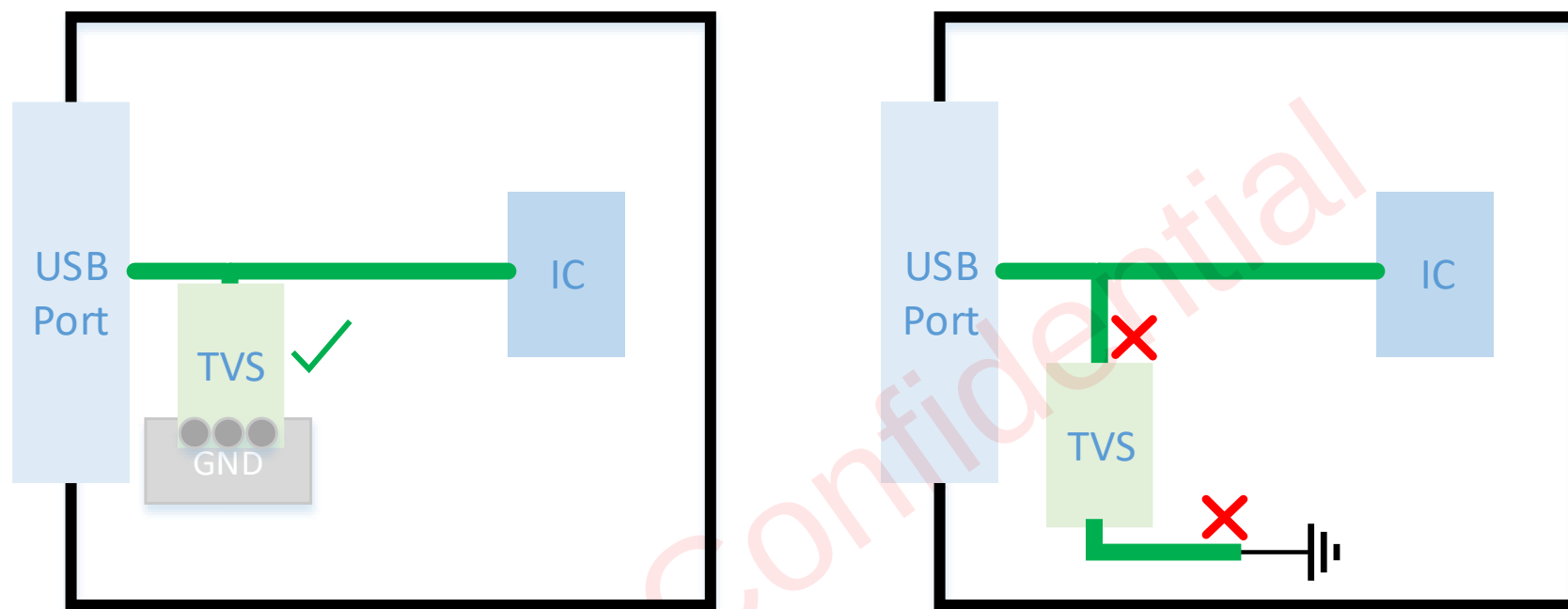


Figure 8 The traces are short and thick with reliable grounding

4) TVS selection

A. Directionality. The one-way TVS tube only clamps the positive pulse, and is generally used in the DC circuit or when there is no negative pulse. The bidirectional TVS tube can absorb positive and negative pulses and is suitable for both AC and DC signals.

B. V_{rwm} : The maximum reverse voltage that can be tolerated. When selected, this parameter should be greater than the maximum battery voltage.

C. V_{br} : reverse breakdown voltage. This voltage marks that the TVS tube begins to enter the reverse breakdown state.

D. V_c : Maximum clamping voltage. This voltage is related to the peak pulse current I_{pp} , and the generation of I_{pp} is related to the surge pulse standard. The specific V_c parameter should refer to the V_c VS I_{pp} curve in the TVS tube datasheet.

E. It is recommended to use a surface mount TVS tube with a small junction capacitance on the package.

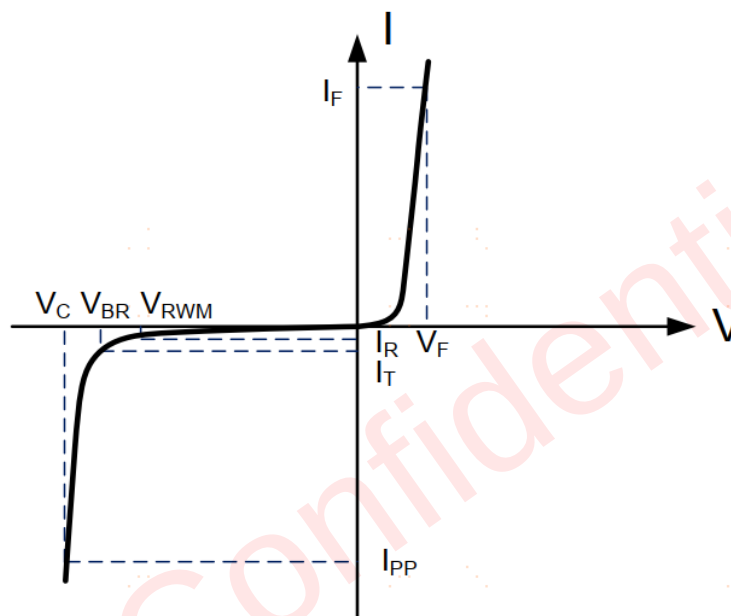


Figure 9 Example diagram of TVS tube characteristics

5) Power network capacitor selection. A capacitor with a larger value can absorb the external surge or ESD impact of the power supply network, so a 22uF or 47uF capacitor can be placed at the PA VDD terminal. Recommended model reference:

1. ESD56301D04
2. WS4.5DPX_W03010184B
3. PTVSHC2EN4V8UF

7 AW87390FCR I2C DEVICE ADDRESS SELECTION

The I2C level of AW87390FCR ranges from 1.3V to VDD, so it can support I2C interface level of 1.8V/2.8V/3.3V, and the interface level is determined by the I2C interface level of the platform. AW87390FCR can configure different I2C addresses through AD1 and AD2 pins. The AD pin has an equivalent impedance of 300K to ground inside the chip, so it can be directly connected to VDD during the process of configuring the I2C address. A resistor is connected in series between the pin and VDD. It is recommended to use 0x58 and 0x5B. The following table is the I2C address configuration description:

AD1	AD2	I ² C address
0	0	0x58
0	1	0x5A
1	0	0x59
1	1	0x5B

Table4 AW87390FCR I2C Device Address Table

8 AW87390FCR COMPONENT SELECTION

1. VDD decoupling capacitor. Appropriate power supply decoupling capacitors can improve the efficiency and best performance of audio PA. Therefore, it is recommended to choose X5R or X7R ceramic capacitors with good temperature stability and low ESR for power supply decoupling capacitors; A decoupling capacitor of 10 μ F or more is used to filter out low-frequency interference on the power supply; a 0.1 μ F decoupling capacitor is added to the closest chip power input pin to filter out high-frequency interference.
2. Fly capacitor selection. The charge pump boost capacitor needs a 0603 package 4.7 μ F/10V X5R or X7R capacitor, which can ensure that the charge pump has sufficient driving capacity when the high power or transient current is too large, and it is guaranteed that there will be no PVDD being pulled down. resulting in truncation distortion.
3. PVDD capacitor selection. The capacitance value of the decoupling capacitor and the size of ESR of the charge pump power output terminal (PVDD) will directly affect the size of the power output ripple, thus affecting the performance of the audio PA. Therefore, it is recommended to choose the X5R with 10 μ F/25V withstand voltage and low ESR. Or X7R ceramic capacitors; in order to ensure the performance of the audio PA, the PVDD capacitor is still guaranteed to have a capacity of 3 μ F or more at 8V.
4. Output magnetic bead capacitor selection. The magnetic beads and 0.1nF at the output are reserved for EMI. Customers should choose whether to use EMI suppression according to the actual situation of the project; the IMAX current of the magnetic beads can be calculated quickly using the formula $IMAX = PVDD / RL * 1.2$ (RL is the DC of SPK Impedance, 1.2 is a 20% margin); if the magnetic beads meet the IMAX current, it is recommended to choose the

model with small DCR, the AC impedance is greater than $100\Omega@100\text{MHz}$, and the product with low THD distortion, because the DCR will directly reduce the load. The effective power to the SPK leads to insufficient loudness; a large AC impedance has a better EMI suppression effect; the 0.1nF capacitor at the output end is recommended to use a capacitor with a rated withstand voltage of 16V; a capacitor with a larger value will suppress EMI better. At the same time, the static power consumption will increase.

5. Output TVS tube selection. The selection of TVS usually only needs to be higher than the PVDD voltage, but since there will still be a certain parasitic inductance on the output transmission line, the modulated square wave output by the audio PA will oscillate due to the existence of the parasitic inductance when passing through the line. There is overshoot on the edge, and if magnetic beads are added to suppress EMI, there will also be a certain edge overshoot, so after the actual project is back, it is recommended to actually test the highest overshoot voltage at both ends of the SPK, and then select the appropriate TVS to prevent the overshoot voltage. If it is too high, the TVS will break down and cause leakage, which will affect both the power consumption and the THD index of the audio.

6. The input capacitor selection C_{in} is the input coupling capacitor of the audio PA, which forms a high-pass filter with the input resistance inside the chip. The calculation formula of the input cut-off frequency is as follows:
Speaker Mode, Input high pass cutoff frequency as follows:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 9k\Omega * 100nF} = 176.9Hz$$

Receiver Mode, Input high pass cutoff frequency as follows:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} = \frac{1}{2 * \pi * 48k\Omega * 100nF} = 33.2Hz$$

9 AW87390FCR PCB REFERENCE LAYOUT

1. The audio PA uses the Charge pump to boost the voltage, the Charge pump circuit constantly switches the switch to complete the charging and discharging of the Fly capacitor. Therefore, some EMI interference may occur during operation. Therefore, the audio PA needs to be kept away from sensitive circuits during layout. (such as antenna, radio frequency, etc.) it is best to use a shielding cover for shielding.
2. Since the signal output by the audio PA is a square wave with pulse width modulation, the bead and EMI capacitor output by the audio PA should be placed as close as possible to the pins of the chip during layout; this can minimize the generation of output signals. interference.
3. All filter capacitors (including VDD and PVDD) of the audio PA should be placed close to the pins of the chip, and follow the principle that the high-frequency filter capacitors are closest to the chip pins, and the low-frequency filter capacitors come second.
4. Please place the Fly capacitor close to the pin of the chip, and try to shorten the trace length from the chip pin to the capacitor.
5. When laying out the two input coupling capacitors, please arrange them in the way of differential lines, and try to ensure the symmetry of the lines when placing them.
6. The TVS should be placed as close as possible to the path that the ESD must pass through, and the grounding of the TVS should be ensured reliably.

10 AW87390FCR PCB REFERENCE ROUTING

1. The signal line using the differential connection method is processed according to the requirements of the differential line, which is equal in length and equal width.

If the single-ended connection method is used, the grounded end is required to go "pseudo-differential" together with the signal line, and then connected to the audio reference ground of the codec of the platform, and then to the main ground through this audio reference ground.

There are two points to pay attention to when routing the differential pair:

- 1) The length of the two signal lines should be as long as possible.
- 2) The distance between the two signal lines and the distance from the ground should always remain the same, that is, they should be parallel.

There are two ways to keep parallel, one is parallel on the same plane, and the two lines go on the same level (side-by-side).

The other is that the two lines walk on the upper and lower adjacent layers (over-under); usually side-by-side is used more; if the differential line does not pay attention to controlling the distance and length, it will affect the signal integrity and delay, resulting in substandard signal quality.

2. The VDD input of the audio PA must first pass through the capacitor and then go to the pin of the chip. The line width is required to meet the maximum current required for the current set power output. The maximum input current can be quickly calculated using the following formula.

$$I_{in}=PVDD^2/R_L/\eta/V_{in}$$

PVDD----- The output voltage of the Charge pump inside the audio PA, that is, the working voltage of the audio PA output stage;

I_{in}----- Audio PA VDD pin input current;

η----- The overall working efficiency of the audio PA is about 80%;

V_{in}----- The VDD input voltage of the audio PA, generally takes the lowest working voltage of the mobile phone to calculate the maximum current (ignoring the influence of the voltage drop on the output voltage of the internal Charge pump of the audio PA);

R_L----- DC impedance of SPK;

For example: the SPK DC impedance of a project is 8 ohms, the PVDD voltage of the audio PA is set to 7.2V, and the minimum operating voltage of the mobile phone is 3.6V, then the I_{in} current can be calculated by substituting the formula as follows:

$$I_{in}=7.2*7.2 / 8 / 0.8 / 3.6=2.25A$$

That is, under the current application conditions, the IPEAK current at the VDD input of the audio PA will reach 2.25A.

Remark:

The fast calculation formula used here does not consider the parasitic impedance of the MOS transistor inside the chip and the parasitic impedance on the PCB; if these factors are taken into account, the actual calculation result will be slightly smaller.

3. Since the signal output by the audio PA is a square wave with pulse width modulation, in order to prevent interference with the output wiring of the audio PA, it is recommended to go on the inner layer of the main board, and it is recommended to brush the electromagnetic shielding film on the FPC; the line width of the output wiring can be calculated by a quick formula $I_{PEAK}=PVDD/RL$.

For example: the SPK DC impedance of a project is 8Ω , and the PVDD voltage of the audio PA is set to 7.2V, then the Ipeak current can be calculated by substituting the formula as follows:

$$I_{peak}=7.2 / 8=0.9A$$

That is, under the current application conditions, the IPEAK current at the output of the audio PA will reach 0.9A.

When routing, pay attention to the line width and the number of vias, so as to avoid insufficient line width and number of vias, which will lead to excessive voltage drop on the line and reduce the effective power loaded on the SPK.

Remark:

The fast calculation formula used here does not take into account the parasitic impedance of the PCB on the output signal path and the DCR of the magnetic beads; the actual calculation results will be slightly smaller if these factors are taken into account.

4. The trace width of the PVDD pin and the external PVDD filter capacitor can refer to the trace requirements of the audio PA output, because the output voltage and current are output by the PVDD filter capacitor, so the current and output from the PVDD filter capacitor to the PVDD pin The current at the terminals is the same.

Remark:

The line width required in LAYOUT is mainly to prevent the PCB traces from having obvious temperature rise and voltage drop due to insufficient line width or excessive via impedance during high current, which will affect the performance of the audio PA. The audio PA cannot work, so it is recommended that customers make reasonable adjustments in the LAYOUT process in combination with their own standards and process levels; if necessary, PDN simulation of a large current path can be performed to verify whether the current design is at risk.

LAYOUT REFERENCE

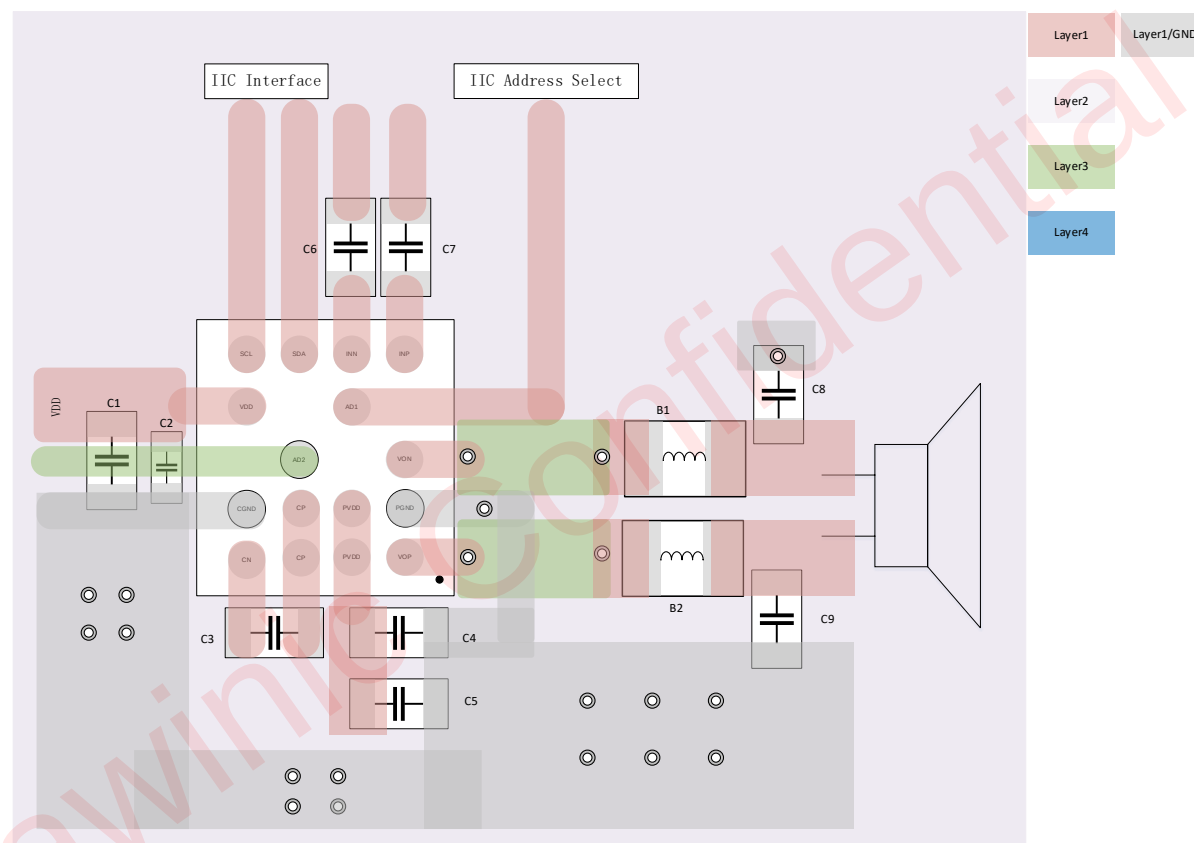


Figure 10 AW87390FCR Layout Reference

All rights reserved

The intellectual property rights of the content of this article are owned by Shanghai Awin Electronic Technology Co., Ltd. Without the written permission of the company, any other person or other company is prohibited from using it in any form (including but not limited to leaking, copying, or distributing in whole or in part) Content of this article.

Document revision history

Version	Date	illustrate
V1.0	October 2021	New document
V1.1	January 2022	1.Documentation upgrade.
V1.2	February 2022	1. Added power network description.

Table5 Document revision history