

## High Efficiency, Dual Independent 1.5A Flash LED Driver

### FEATURES

- Support Dual Color Temperature Flash LED Application
- Dual Independent and Programmable 1.5A LED Current Source
  - Flash: 11.35mA~1.5A, 128 levels  
11.72mA/level
  - Torch: 2.55mA~372mA, 128 levels  
2.91mA/level
  - Flash Timeout: 40ms~1.6s, 16 levels
  - Flash/Torch/IR Mode
- High Efficiency: 85%
- Optimized Flash LED Current During Low Battery Conditions (IVFM)
- Hardware Strobe Enable (STROBE)
- Hardware Torch Enable (TORCH/TEMP)
- Remote NTC Monitoring
- Synchronization Input for RF Power Amplifier Pulse Events (TX)
- 400kHz I<sup>2</sup>C: AW3644 (I<sup>2</sup>C Address=0x63)
- 0.4mm Pitch, CSP-12 Package  
Compatible with AW3643, AW36413, AW36414

### APPLICATION

Smartphone Camera Flash

### TYPICAL APPLICATION CIRCUIT

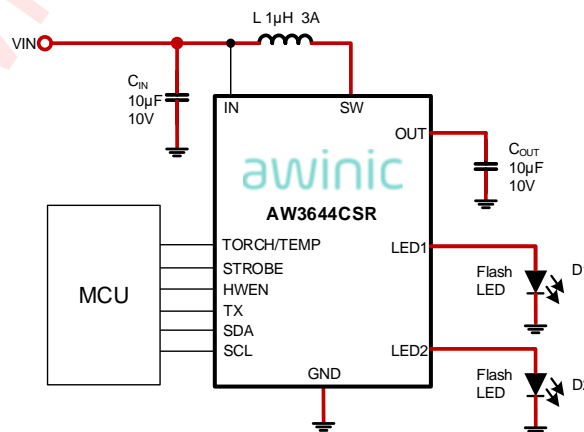


Fig 1 Typical Application Circuit of AW3644

### GENERAL DESCRIPTION

The AW3644 is a dual LED flash driver that provides a high level of adjustability within a small solution size. The AW3644 utilizes a 2MHz or 4MHz fixed-frequency synchronous boost converter to provide power to the dual 1.5A constant current LED sources. The dual 128 levels current sources provide the flexibility to adjust the current of LED1 and LED2 in Flash/Torch/IR modes. The AW3644 provides three IVFM protection modes to prevent system reset or shutdown under low battery condition.

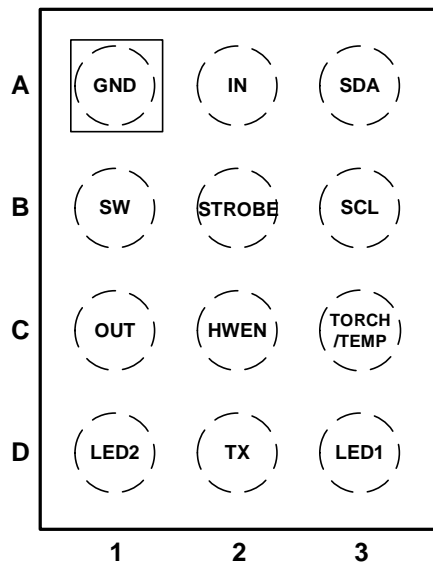
The AW3644 are controlled via an I<sup>2</sup>C - compatible interface. The main features of the AW3644 include: flash/torch current, flash timeout duration, IVFM, TX interrupt, and NTC thermistor monitor. The AW3644 also provides hardware flash and hardware torch pins (STROBE and TORCH/TEMP) to control Flash/Torch events.

The 2MHz or 4MHz switching frequency options, overvoltage protection (OVP), and adjustable current limit allow for the use of tiny, low-profile inductors and 10-µF ceramic capacitors. The device operates over a -40°C to +85°C ambient temperature range.

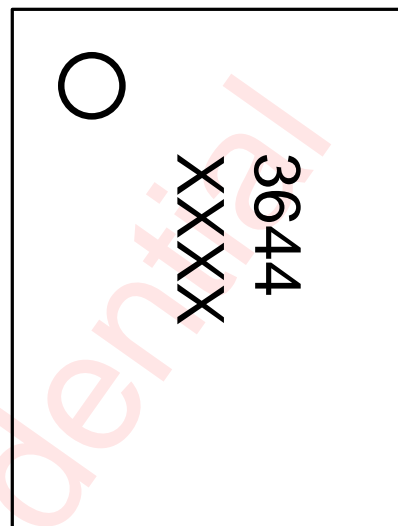
The AW3644 is available in small 0.4mm pitch 1.626mm×1.332mm CSP-12 package.

## PIN CONFIGURATION AND TOP MARK

**AW3644CSR Pin Configuration  
(Top View)**



**AW3644CSR Top Mark  
(Top View)**



3644 - AW3644CSR  
XXXX - Manufacture Tracking Code

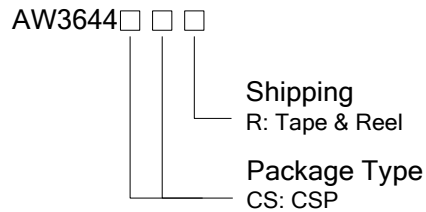
**Fig 2 Pin Configuration and Top Mark**

## PIN DEFINITION

| No. | NAME       | TYPE   | DESCRIPTION   |
|-----|------------|--------|---|
| A1  | GND        | Ground | Ground  |
| A2  | IN         | Power  | Input voltage connection. Connect IN to GND with a 10μF or larger ceramic capacitor.  |
| A3  | SDA        | I/O    | Serial data input/output of the I <sup>2</sup> C interface.   |
| B1  | SW         | Power  | Switch pin of the step-up DC-DC convertor.  |
| B2  | STROBE     | I/O    | Active high hardware flash enable. Drive STROBE high to turn on Flash pulse. Internal pull down resistor of 300kΩ between STROBE and GND. |
| B3  | SCL        | I/O    | Serial clock input of the I <sup>2</sup> C interface.   |
| C1  | OUT        | Power  | Step-up DC-DC converter output. Connect a 10μF ceramic capacitor between OUT and GND.   |
| C2  | HWEN       | I/O    | Active high enable pin. High = Standby, Low = Shutdown/Reset. Internal pull down resistor of 300kΩ between HWEN and GND.                  |
| C3  | TORCH/TEMP | I/O    | Torch terminal input or threshold detector for NTC temperature sensing and current scale back.  |
| D1  | LED2       | Power  | High-side current source output for flash LED2.   |
| D2  | TX         | I/O    | Power amplifier synchronization input. Internal pull down resistor of 300kΩ between TX and GND.   |
| D3  | LED1       | Power  | High-side current source output for flash LED1.   |

## ORDERING INFORMATION

| Part Number | Temperature | Package                   | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form                |
|-------------|-------------|---------------------------|---------|----------------------------|---------------------------|------------------------------|
| AW3644CSR   | -40°C~85°C  | 1.626mm×1.332mm<br>CSP-12 | 3644    | MSL1                       | ROHS+HF                   | 3000 units/<br>Tape and Reel |



## AWINIC FLASH LED DRIVER SERIES

| Product | Channels | Type         | Description   | Package |
|---------|----------|--------------|---|---------|
| AW3644  | 2        | Boost        | High Efficiency, Dual Independent 1.5A Flash LED Driver                   | CSP-12  |
| AW36414 | 2        | Boost        | High Efficiency, Dual Independent 1.5A Flash LED Driver                   | CSP-12  |
| AW3643  | 2        | Boost        | High Efficiency, Dual 1.5A Flash LED Driver                               | CSP-12  |
| AW36413 | 2        | Boost        | High Efficiency, Dual 1.5A Flash LED Driver                               | CSP-12  |
| AW3648  | 1        | Boost        | High Efficiency, 1.5A Flash LED Driver                                    | CSP-12  |
| AW3642  | 1        | Boost        | High Efficiency, 1.5A Flash LED Driver                                    | CSP-9   |
| AW3641E | 1        | Charge Pump  | Flash Current & Flash Timer Programmable 1A Flash LED Driver              | DFN-10L |
| AW36402 | 1        | Current Sink | 200mA 1-wire Configurable Front Flash LED Driver with Ultra Small Package | DFN-6L  |
| AW36404 | 1        | Current Sink | 400mA 1-wire Configurable Front Flash LED Driver with Ultra Small Package | DFN-8L  |
| AW36406 | 1        | Current Sink | 600mA PWM Configurable Front Flash LED Driver with Ultra Small Package    | DFN-8L  |

## TYPICAL APPLICATION CIRCUITS

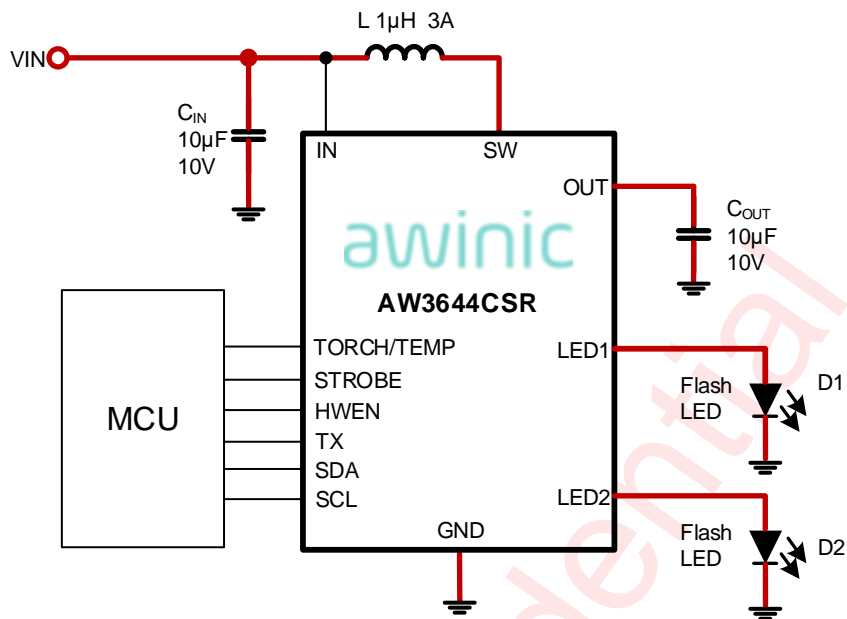


Fig 3 AW3644 Application Circuit

### Notice for Typical Application Circuits:

- 1: Please place  $C_{IN}$ ,  $C_{OUT}$  as close to the chip as possible.
- 2: Connect the inductor on the top layer close to the SW pin.
- 3: For the sake of driving capability, the power lines, output lines, and the connection lines of L and LED should be short and wide as possible.

## ABSOLUTE MAXIMUM RATINGS<sup>(NOTE1)</sup>

| PARAMETERS   |     | Range                  | Unit |
|--|-----|------------------------|------|
| IN, SW, OUT, LED1, LED2                              |     | -0.3 to 6              | V    |
| HWEN, SCL, SDA, STROBE, TORCH/TEMP, TX               |     | -0.3 to (VIN+0.3)      | V    |
| Continuous power dissipation                         |     | Internally limited     |      |
| Max Junction Temperature T <sub>JMAX</sub>           |     | 155                    | °C   |
| Storage Temperature T <sub>STG</sub>                 |     | -65 to 150             | °C   |
| Maximum lead temperature (soldering)                 |     | 260                    | °C   |
| Junction to Ambient Thermal Resistance $\theta_{JA}$ |     | 79.2                   | °C/W |
| ESD, All Pins <sup>(NOTE2)</sup>                     | HBM | ±2000                  | V    |
|  | CDM | ±1500                  | V    |
| Latch-Up (Test method: JEDEC STANDARD NO.78D)        |     | +IT: +200<br>-IT: -200 | mA   |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETERS                             | Range      | Unit |
|--|------------|------|
| V <sub>IN</sub>                        | 2.7 to 5.5 | V    |
| Junction temperature (T <sub>J</sub> ) | -40 to 125 | °C   |
| Ambient temperature (T <sub>A</sub> )  | -40 to 85  | °C   |

*NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

*NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9*

## ELECTRICAL CHARACTERISTICS

Typical limits tested at  $T_A=25^{\circ}\text{C}$ . Minimum and maximum limits apply over the full operating ambient temperature range( $-40^{\circ}\text{C}\leq T_A\leq 85^{\circ}\text{C}$ ). Unless otherwise specified,  $V_{IN}=3.6\text{V}$ ,  $\text{HWEN}=V_{IN}$ .

| Symbol                                | Description                                | Test Condition   | Min  | Typ | Max  | Unit               |
|---------------------------------------|--|--|------|-----|------|--------------------|
| <b>Vin Supply</b>                     |  |  |      |     |      |                    |
| $V_{IN}$                              | Input operating range                      |  | 2.7  |     | 5.5  | V                  |
| $I_Q$                                 | Quiescent supply current                   | Device not switching, pass mode  |      | 0.4 | 0.8  | mA                 |
| $I_{SB}$                              | Standby supply current                     | Device disabled, $\text{HWEN}=1.8\text{V}$<br>$2.5\text{V}\leq V_{IN}\leq 5.5\text{V}$ |      | 3   | 10   | $\mu\text{A}$      |
| $I_{SD}$                              | Shutdown supply current                    | Device disabled, $\text{HWEN}=0\text{V}$<br>$2.5\text{V}\leq V_{IN}\leq 5.5\text{V}$   |      | 0.1 | 1    | $\mu\text{A}$      |
| UVLO                                  | Under voltage lockout threshold            | Falling $V_{IN}$   |      | 2.5 |      | V                  |
|                                       |  | Rising $V_{IN}$  |      | 2.6 |      | V                  |
| <b>Current Source Specifications</b>  |  |  |      |     |      |                    |
| $I_{LED1/2}$                          | Current source accuracy                    | $V_{OUT}=4\text{V}$ ,<br>flash code=0x7F=1.5A  | -7%  | 1.5 | 7%   | A                  |
|                                       |  | $V_{OUT}=4\text{V}$ ,<br>torch code=0x3F=186mA   | -10% | 186 | 10%  | mA                 |
| $V_{OVP}$                             | $V_{OUT}$ over-voltage protect threshold   | ON threshold   | 4.85 | 5   | 5.15 | V                  |
|                                       |  | OFF threshold  | 4.75 | 4.9 | 5.05 |                    |
| <b>Boost Converter Specifications</b> |  |  |      |     |      |                    |
| $R_{PMOS}$                            | PMOS switch on-resistance                  |  |      | 85  |      | $\text{m}\Omega$   |
| $R_{NMOS}$                            | NMOS switch on-resistance                  |  |      | 60  |      | $\text{m}\Omega$   |
| $I_{CL}$                              | Switch current limit                       | Reg 0x07, bit[0]=0   | -12% | 1.9 | 12%  | A                  |
|                                       |  | Reg 0x07, bit[0]=1   | -12% | 2.8 | 12%  |                    |
| $F_{SW}$                              | Switching frequency                        | Reg 0x07, bit[1]=0   | -6%  | 2   | 6%   | MHz                |
|                                       |  | Reg 0x07, bit[1]=1   | -6%  | 4   | 6%   |                    |
| $V_{IVFM}$                            | Input voltage flash monitor trip threshold | Reg 0x02, bits[3:1]="000"  | -3%  | 2.9 | 3%   | V                  |
| $I_{NTC}$                             | NTC current                                |  | -6%  | 50  | 6%   | $\mu\text{A}$      |
| $V_{TRIP}$                            | NTC comparator trip threshold              | Reg 0x09, bit[3:1]="100"   | -6%  | 0.6 | 6%   | V                  |
| $T_{SD}$                              | Thermal shutdown threshold                 |  |      | 155 |      | $^{\circ}\text{C}$ |
|                                       | Thermal shutdown hysteresis                |  |      | 20  |      |                    |

| Symbol   | Description                  | Test Condition         | Min | Typ | Max             | Unit |
|--|------------------------------|------------------------|-----|-----|-----------------|------|
| <b>I<sup>2</sup>C-Compatible Interface Specifications(SCL,SDA)</b> |                              |                        |     |     |                 |      |
| V <sub>IL</sub>  | Input logic low              |                        | 0   |     | 0.4             | V    |
| V <sub>IH</sub>  | Input logic high             |                        | 1.2 |     | V <sub>IN</sub> | V    |
| V <sub>OL</sub>  | Output logic low             | I <sub>LOAD</sub> =3mA |     |     | 0.4             | V    |
| <b>HWEN, STROBE, TORCH/TEMP, TX Voltage Specifications</b>         |                              |                        |     |     |                 |      |
| V <sub>IL</sub>  | Input logic low              |                        | 0   |     | 0.4             | V    |
| V <sub>IH</sub>  | Input logic high             |                        | 1.2 |     | V <sub>IN</sub> | V    |
| R <sub>PD</sub>  | Internal pull down resistors |                        |     | 300 |                 | kΩ   |

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## I<sup>2</sup>C INTERFACE TIMING

| Symbol                | Description                               | Min | Typ | Max | Units |
|-----------------------|---|-----|-----|-----|-------|
| F <sub>SCL</sub>      | Interface Clock frequency                 |     |     | 400 | kHz   |
| T <sub>DEGLITCH</sub> | Deglitch time                             | SCL | 200 |     | ns    |
|                       |   | SDA | 250 |     | ns    |
| T <sub>HD:STA</sub>   | (Repeat-start) Start condition hold time  | 0.6 |     |     | μs    |
| T <sub>LOW</sub>      | Low level width of SCL                    | 1.3 |     |     | μs    |
| T <sub>HIGH</sub>     | High level width of SCL                   | 0.6 |     |     | μs    |
| T <sub>SU:STA</sub>   | (Repeat-start) Start condition setup time | 0.6 |     |     | μs    |
| T <sub>HD:DAT</sub>   | Data hold time                            | 0   |     |     | μs    |
| T <sub>SU:DAT</sub>   | Data setup time                           | 0.1 |     |     | μs    |
| T <sub>R</sub>        | Rising time of SDA and SCL                |     |     | 0.3 | μs    |
| T <sub>F</sub>        | Falling time of SDA and SCL               |     |     | 0.3 | μs    |
| T <sub>SU:STO</sub>   | Stop condition setup time                 | 0.6 |     |     | μs    |
| T <sub>BUF</sub>      | Time between start and stop condition     | 1.3 |     |     | μs    |

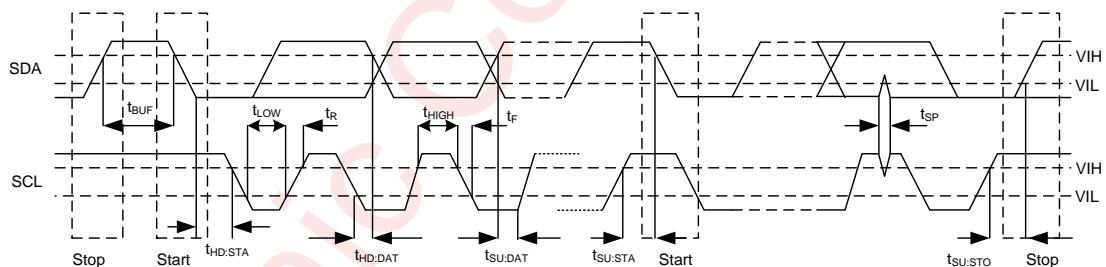


Fig 4 I<sup>2</sup>C INTERFACE TIMING



## TYPICAL CHARACTERISTICS

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = IN, C<sub>IN</sub> = C<sub>OUT</sub> = 2×10 μF and L=1 μH, unless otherwise noted .

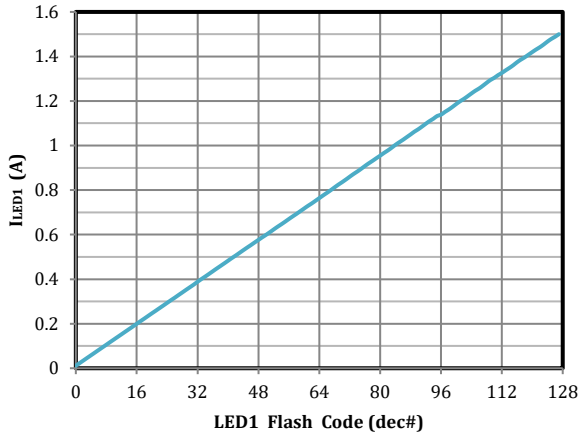


Fig 5. LED1 Flash Current vs Brightness Code

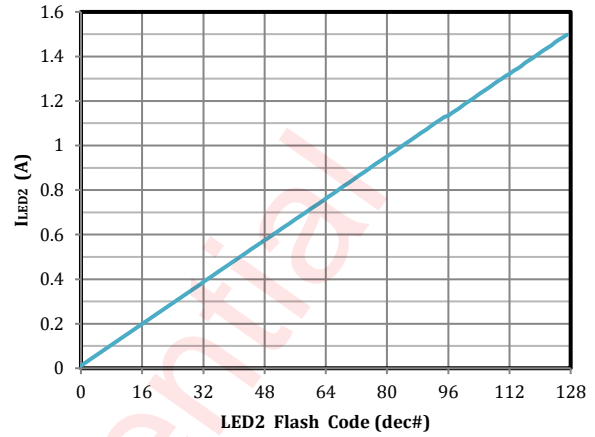


Fig 6. LED2 Flash Current vs Brightness Code

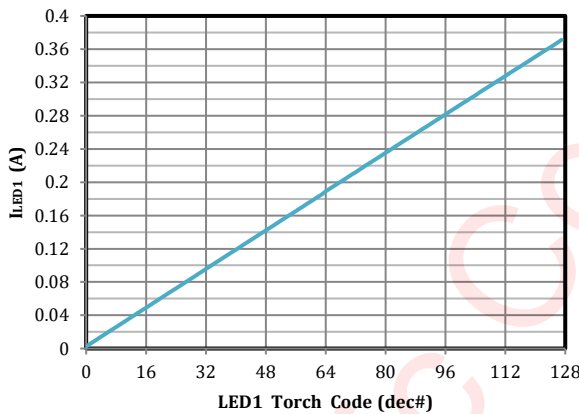


Fig 7. LED1 Torch Current vs Brightness Code

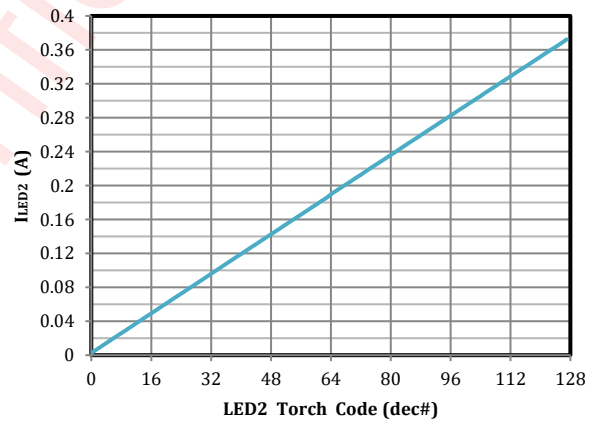


Fig 8. LED2 Torch Current vs Brightness Code

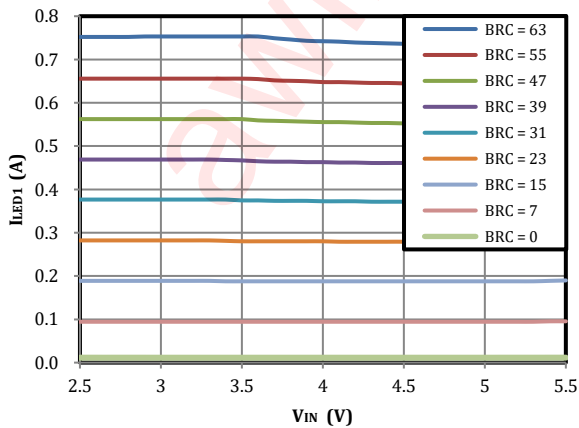


Fig 9. LED1 Flash Current vs Input Voltage

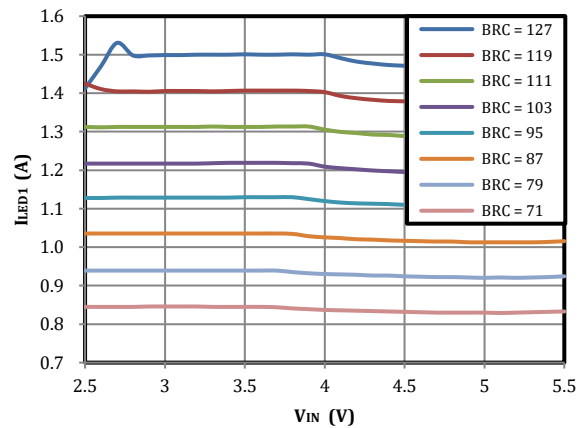


Fig 10. LED1 Flash Current vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = IN, C<sub>IN</sub> = C<sub>OUT</sub> = 2×10 μF and L=1 μH, unless otherwise noted .

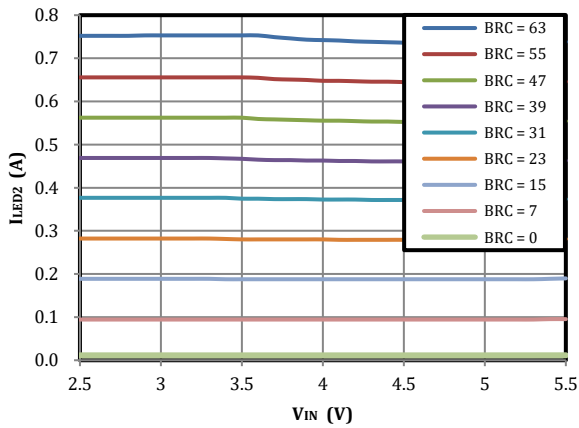


Fig 11. LED2 Flash Current vs Input Voltage

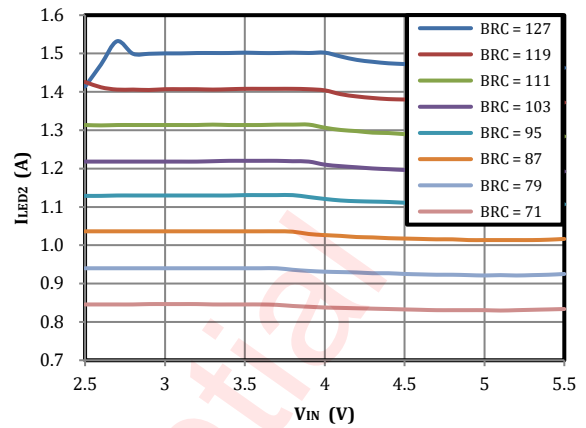


Fig 12. LED2 Flash Current vs Input Voltage

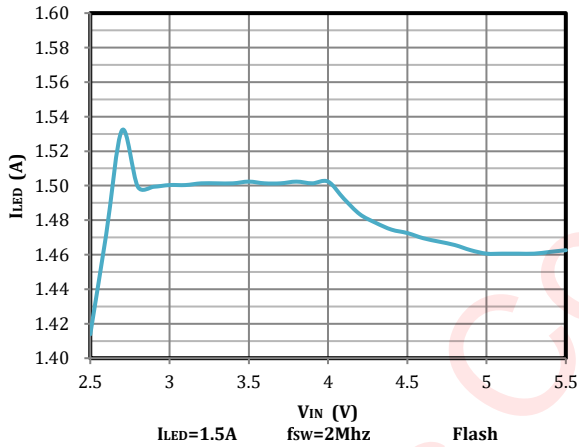


Fig 13. LED1/2 Flash Current vs Input Voltage

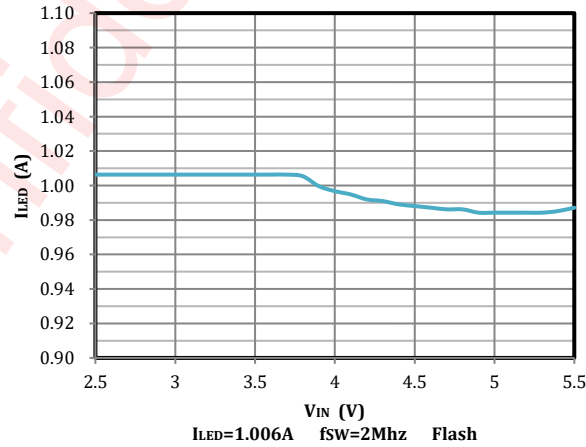


Fig 14. LED1/2 Flash Current vs Input Voltage

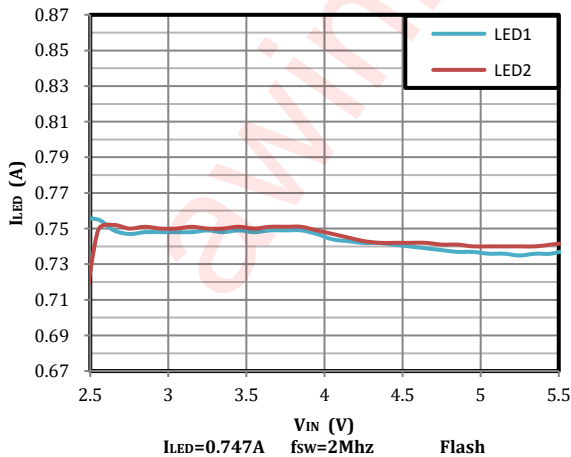


Fig 15. LED1 & LED2 Current vs Input Voltage

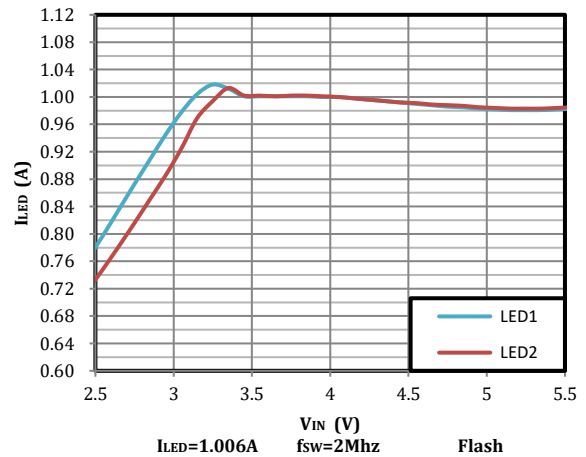


Fig 16. LED1 & LED2 Current vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = IN, C<sub>IN</sub> = C<sub>OUT</sub> = 2×10 μF and L=1 μH, unless otherwise noted .

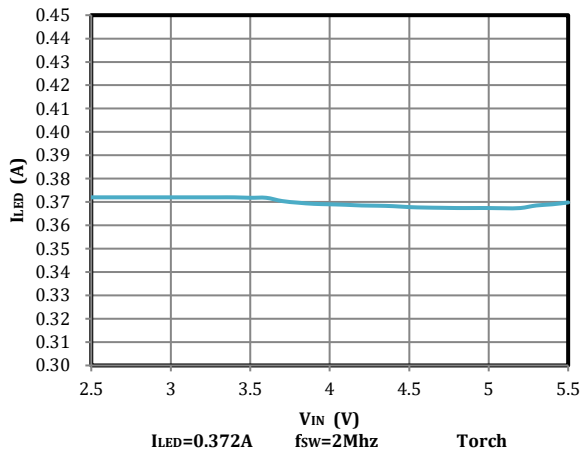


Fig 17. LED1/2 Torch Current vs Input Voltage

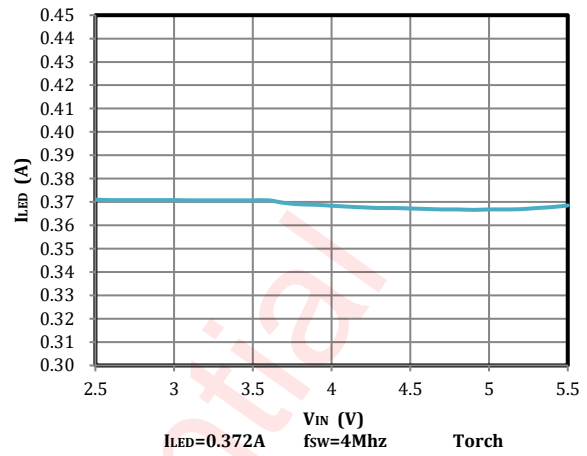


Fig 18. LED1/2 Torch Current vs Input Voltage

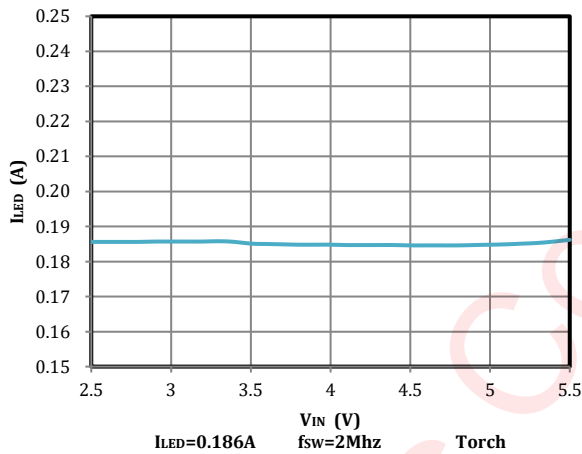


Fig 19. LED1/2 Torch Current vs Input Voltage

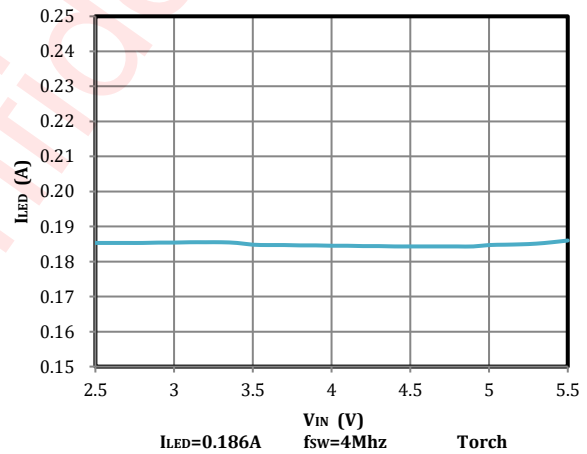


Fig 20. LED1/2 Torch Current vs Input Voltage

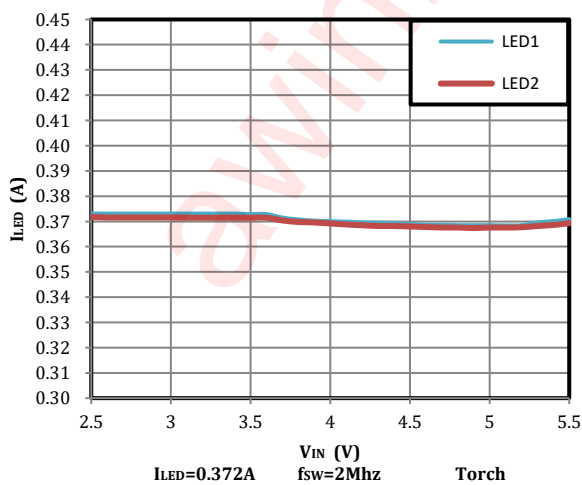


Fig 21. LED1 & LED2 Current vs Input Voltage

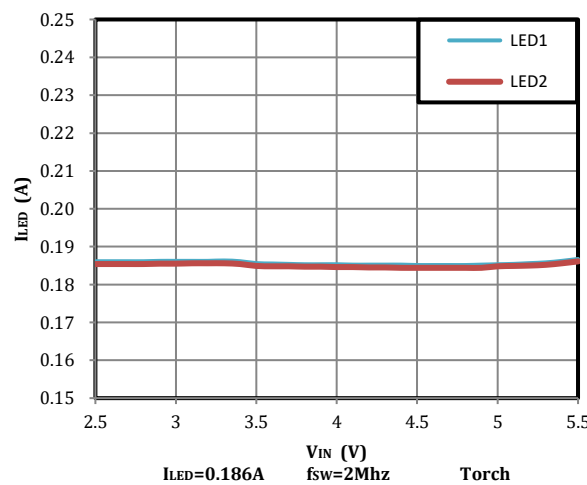


Fig 22. LED1 & LED2 Current vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = IN, C<sub>IN</sub> = C<sub>OUT</sub> = 2×10 μF and L=1 μH, unless otherwise noted .

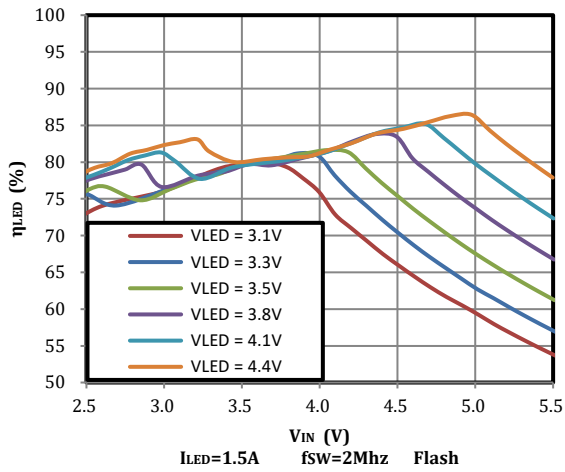


Fig23. LED Efficiency vs Input Voltage

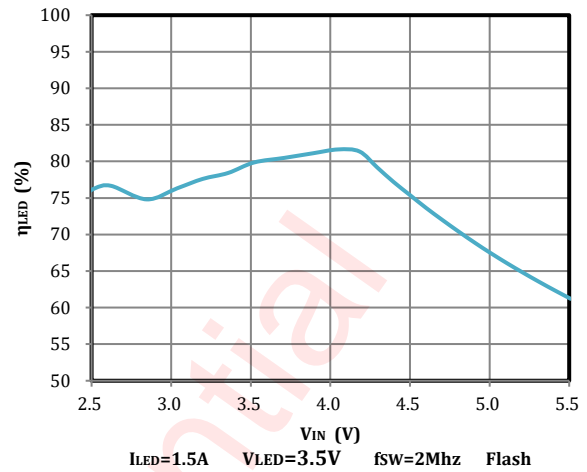


Fig24. LED Efficiency vs Input Voltage

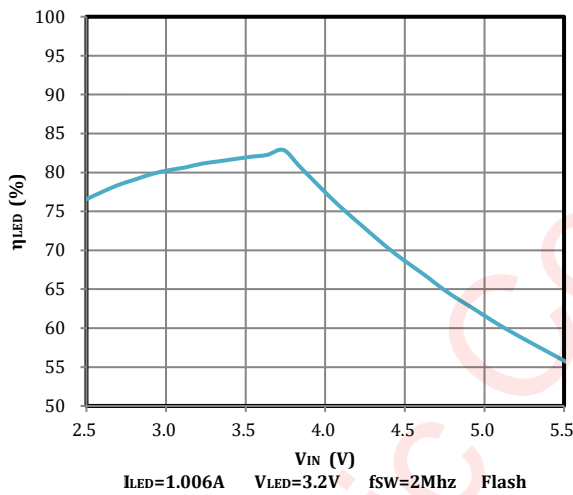


Fig25. LED Efficiency vs Input Voltage

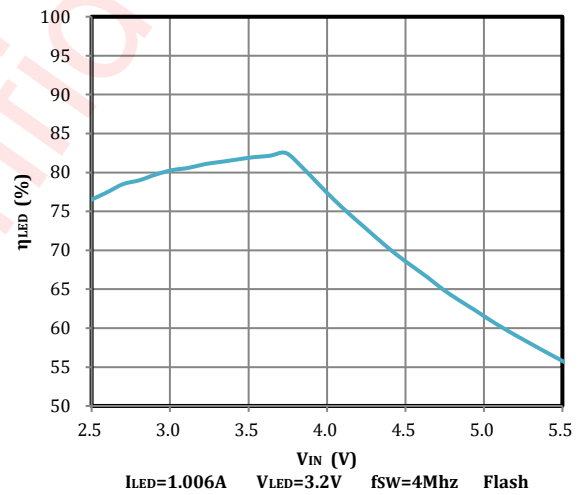


Fig26. LED Efficiency vs Input Voltage

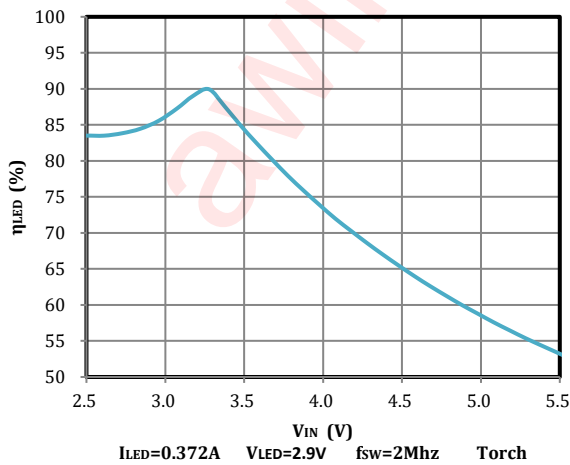


Fig 27. LED Efficiency vs Input Voltage

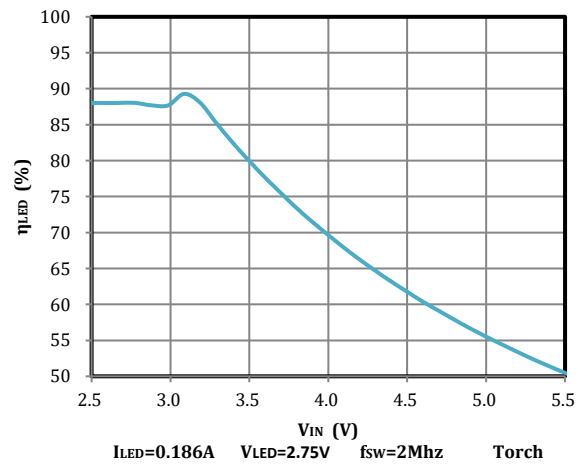


Fig 28. LED Efficiency vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = IN, C<sub>IN</sub> = C<sub>OUT</sub> = 2×10 μF and L=1 μH, unless otherwise noted .

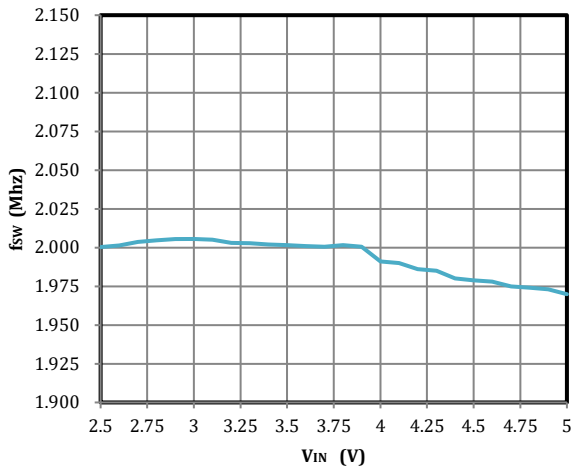


Fig 29. 2-Mhz Frequency vs Input Voltage

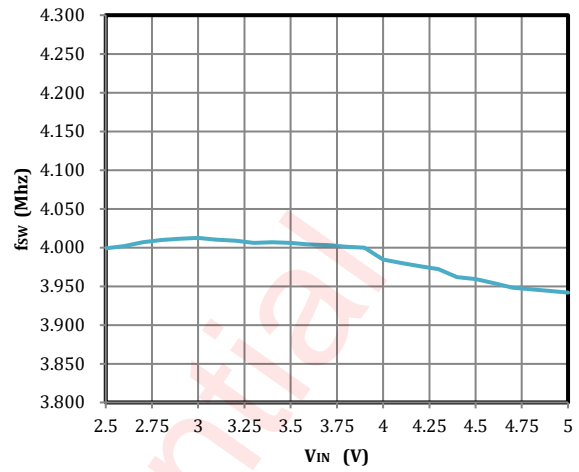


Fig 30. 4-Mhz Frequency vs Input Voltage

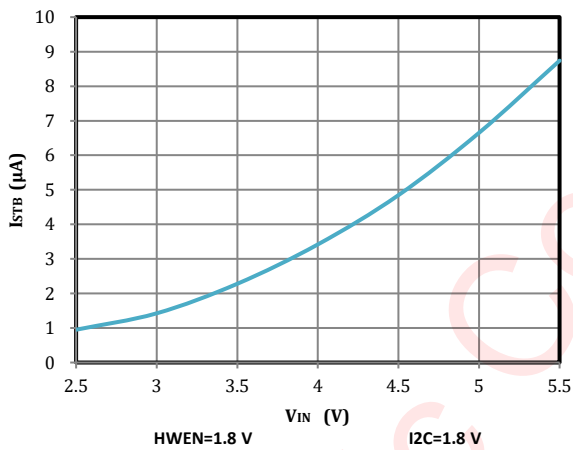


Fig 31. Standby Current vs Input Voltage

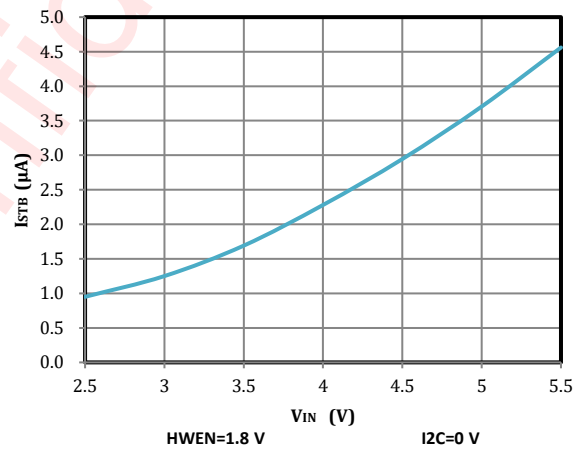


Fig 32. Standby Current vs Input Voltage

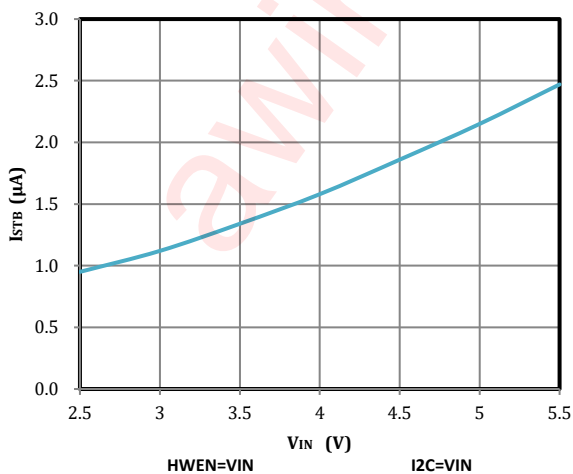


Fig 33. Standby Current vs Input Voltage

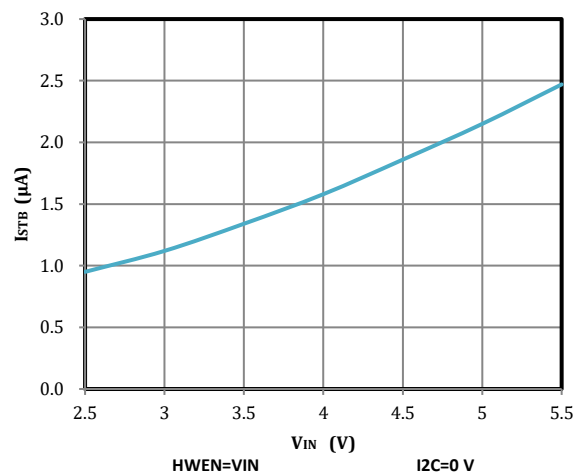


Fig 34. Standby Current vs Input Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = IN, C<sub>IN</sub> = C<sub>OUT</sub> = 2×10 μF and L=1 μH, unless otherwise noted .

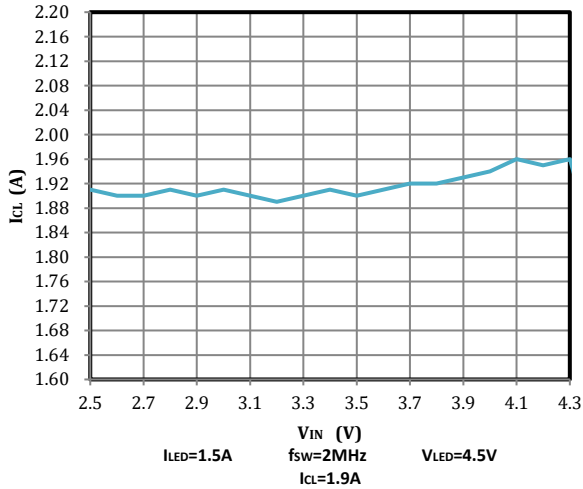


Fig 35. Inductor Current Limit vs Input Voltage

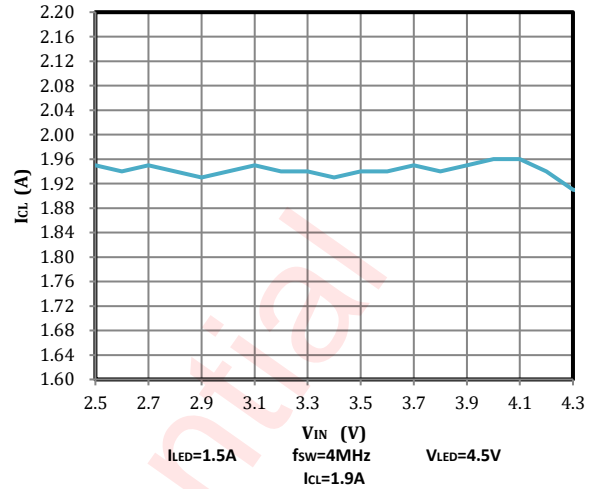


Fig 36. Inductor Current Limit vs Input Voltage

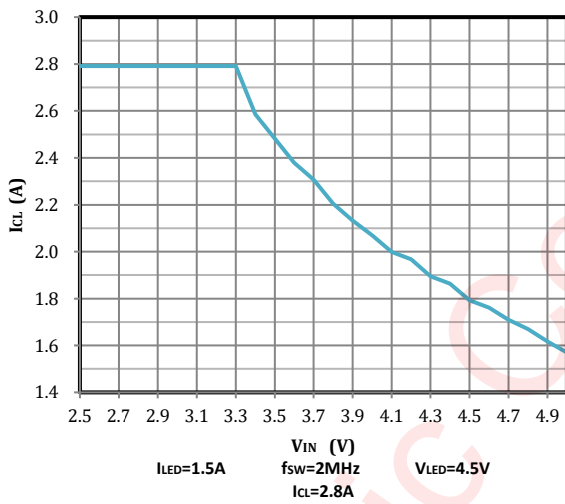


Fig 37. Inductor Current Limit vs Input Voltage

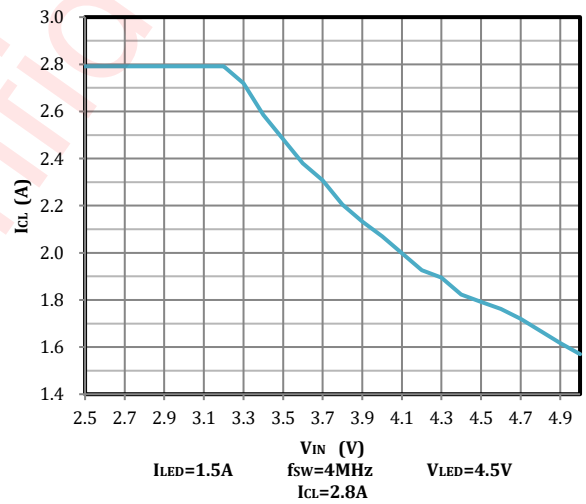


Fig 38. Inductor Current Limit vs Input Voltage

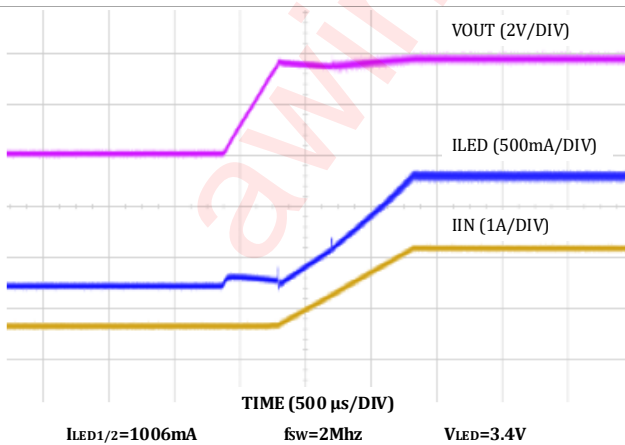


Fig 39. Ramp Up

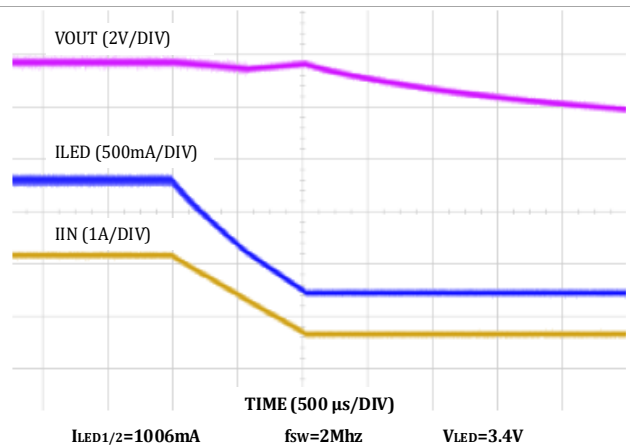
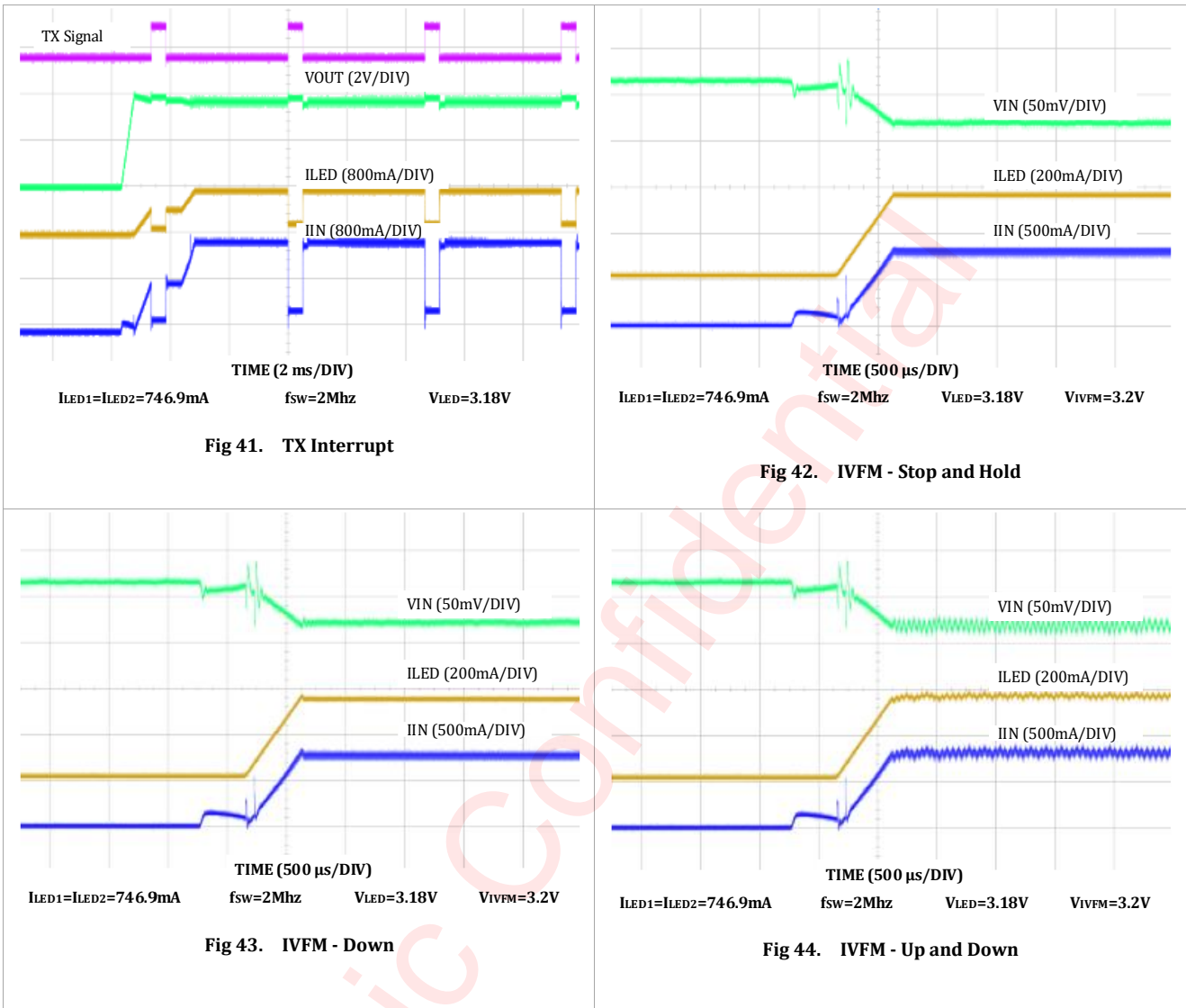


Fig 40. Ramp Down

Typical Characteristics (continued)

Ambient temperature is 25°C, input voltage is 3.6 V, HWEN = IN, C<sub>IN</sub> = C<sub>OUT</sub> = 2×10 μF and L=1 μH, unless otherwise noted .



## DETAILED FUNCTIONAL DESCRIPTION

The AW3644 is a high-power white LED flash driver capable of delivering up to 1.5A in either of the two parallel LEDs. The device incorporates a 2MHz or 4MHz constant frequency-synchronous current-mode PWM boost converter and dual high-side current sources to regulate the LED current over the 2.7V to 5.5V input voltage range.

The AW3644 PWM DC-DC boost converter switches and boosts the output to maintain at least  $V_{HR}$  across each of the current sources (LED1/2). This minimum headroom voltage ensures that both current sources remain in regulation. If the input voltage is above the LED voltage + current source headroom voltage, the device would not switch, but turn the PMOS on continuously (Pass mode). In Pass mode the difference between  $(V_{IN} - I_{LED} \times R_{PMOS})$  and the voltage across the LED is dropped across the current source.

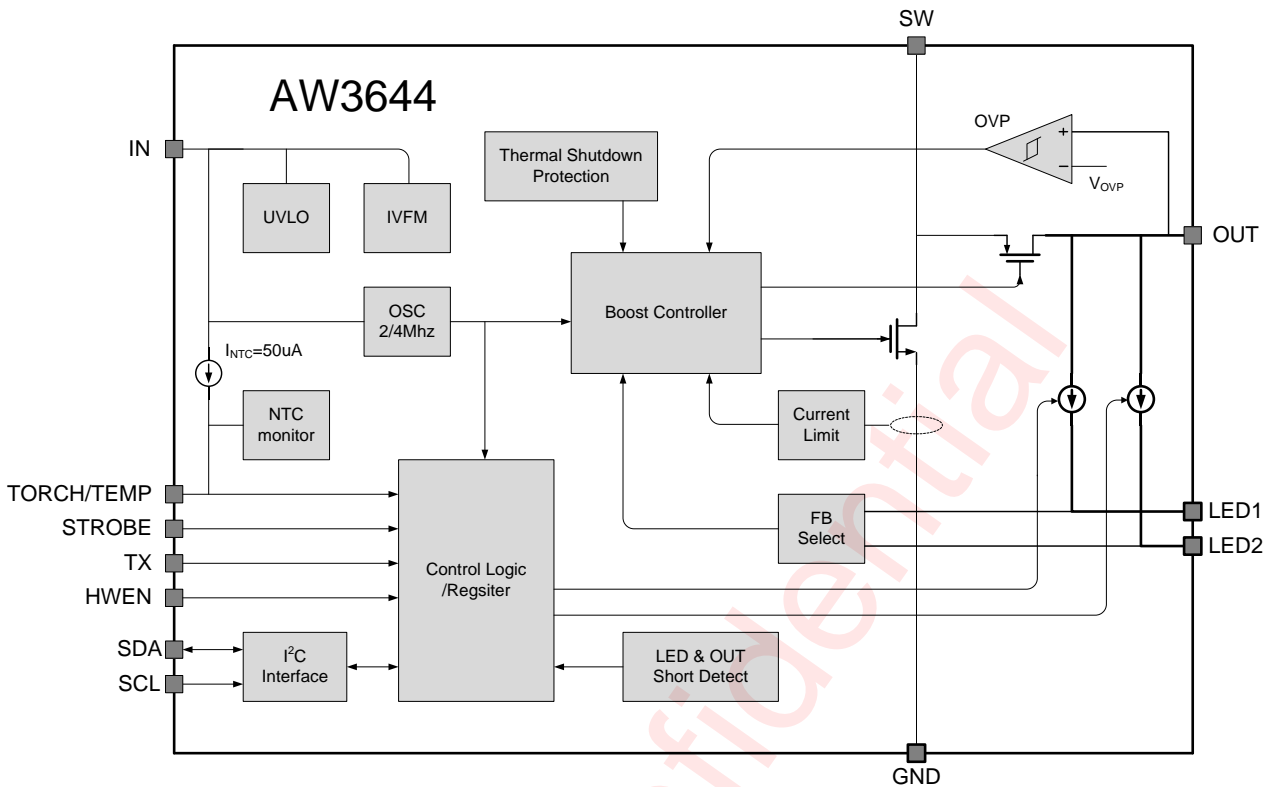
The AW3644 has three logic inputs including a hardware Flash Enable (STROBE), a hardware Torch Enable (TORCH/TEMP, TORCH = default), and a Flash Interrupt input (TX) designed to interrupt the flash pulse during high battery-current conditions. These logic inputs have internal 300k $\Omega$  (typical) pull-down resistors to GND.

Additional features of the AW3644 include an internal comparator for LED thermal sensing via an external NTC thermistor and an input voltage monitor that can reduce the Flash current during low  $V_{IN}$  conditions. It also has a Hardware Enable (HWEN) pin that can be used to reset the state of the device and the registers by pulling the HWEN pin to ground.

Control is done via an I<sup>2</sup>C-compatible interface. This includes adjustment of the Flash and Torch current levels, changing the Flash Timeout Duration, and changing the switch current limit. Additionally, there are flag and status bits that indicate flash current timeout, LED over-temperature condition, LED failure (open/short), device thermal shutdown, TX interrupt, and  $V_{IN}$  under-voltage conditions.



## FUNCTIONAL BLOCK DIAGRAM



## FEATURE DESCRIPTION

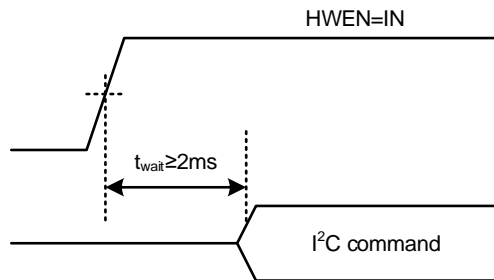
### HWEN & I<sup>2</sup>C INTERFACE

AW3644 has a logic input HWEN pin to enable/disable the device. When HWEN is set low, the device goes into shutdown mode, the I<sup>2</sup>C interface is disabled and all I<sup>2</sup>C registers are reset to default. In shutdown mode the device does not respond to any I<sup>2</sup>C command. When HWEN is set high, the device goes into standby mode, the I<sup>2</sup>C interface is enabled, and the device can respond to I<sup>2</sup>C command.

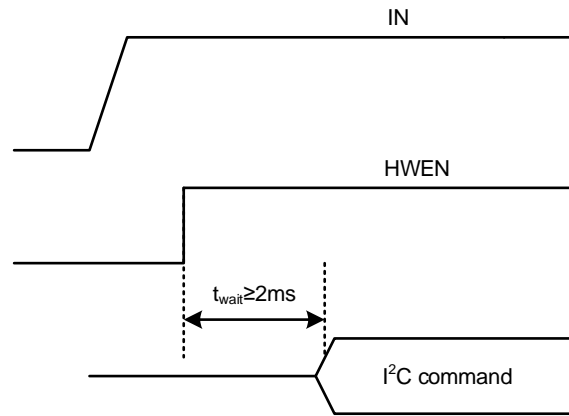
There are two kinds of power-up sequences, shown in Figure 45 and Figure 46.

If HWEN is tied to IN pin in application, once IN goes above around V<sub>POR</sub> (2.0V), HWEN should stay high for at least  $t_{wait}=2ms$  time before any I<sup>2</sup>C command can be accepted.

If HWEN is driven by a GPIO, once HWEN goes from low to high, HWEN should stay high for at least  $t_{wait}=2ms$  time before any I<sup>2</sup>C command can be accepted.



**Fig 45 Power-Up Sequence with HWEN Tied to IN**



**Fig 46 Power-Up Sequence with HWEN Driven by GPIO**

### **SOFT RESET**

By setting bit[7](Software Reset Bit) to a '1' in the Boost Configuration Register(0x07) via I2C interface will reset the AW3644 internal circuit and all configuration registers, after the soft reset command is input through I2C, it needs to wait at least 2ms before any other I2C command can be accepted.

### **FLASH MODE**

In Flash Mode, the LED current sources (LED1/2) provide 128 target current levels from 11.35mA to 1.5A. The Flash currents are adjusted via the LED1 and LED2 Flash Brightness Registers. Flash mode is activated by the Enable Register(setting M1, M0 to '11'), or by pulling the STROBE pin HIGH when the pin is enabled (Enable Register). Once the Flash sequence is activated the current source (LED1/2) ramps up to the programmed Flash current by stepping through all current steps until the programmed current is reached.

When the device is enabled in Flash Mode through the Enable Register, all mode bits in the Enable Register are cleared after a flash timeout event.

### **TORCH MODE**

In Torch mode, the LED current sources (LED1/2) provide 128 target current levels from 2.55mA to 372mA on AW3644. The Torch currents are adjusted via the LED1 and LED2 Torch Brightness Registers. Torch mode is activated by the Enable Register (setting M1, M0 to '10'), or by pulling the TORCH/TEMP pin HIGH when the pin is enabled (Enable Register) and set to Standby Mode. Once the TORCH sequence is activated the active current sources (LED1/2) ramps up to the programmed Torch current by stepping through all current steps until the programmed current is reached. The rate at which the current ramps is determined by the value chosen in the Timing Register.

Torch Mode is not affected by Flash Timeout or by a TX Interrupt event.

### **IR MODE**

In IR Mode, the target LED current is equal to the value stored in the LED1/2 Flash Brightness Registers. When IR mode is enabled (setting M1, M0 to '01'), the boost converter turns on and set the output equal to the input (pass-mode). At this point, toggling the STROBE pin enables and disables the LED1/2 current sources (if enabled). The strobe pin can only be set to be Level sensitive, meaning all timing of the IR pulse is externally controlled. In IR Mode, the current sources do not ramp the LED outputs to the target. The current transitions immediately from off to on and then on to off.

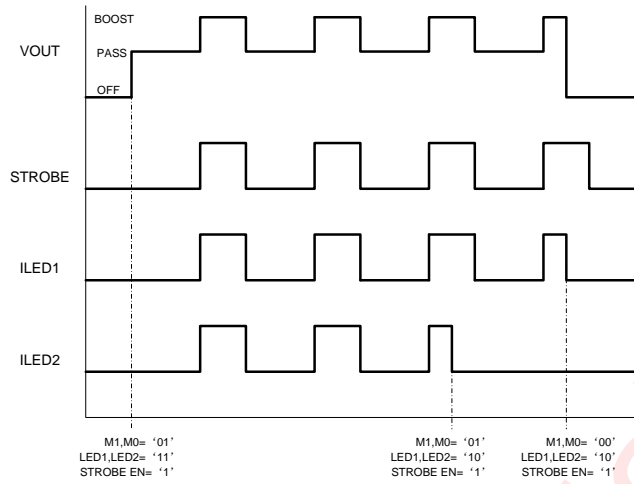


Fig 47 IR Mode with Boost

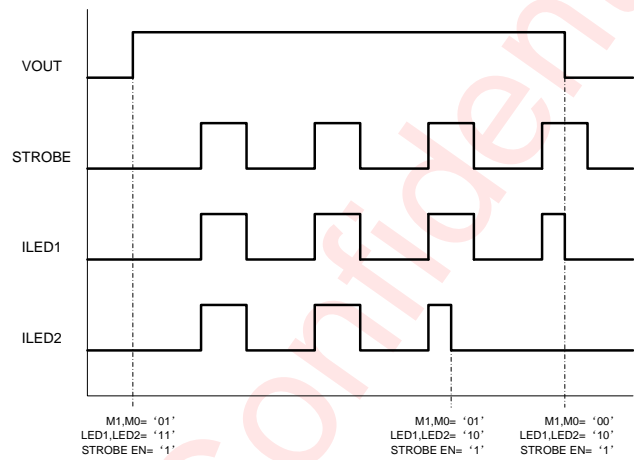


Fig 48 IR Mode Pass Only

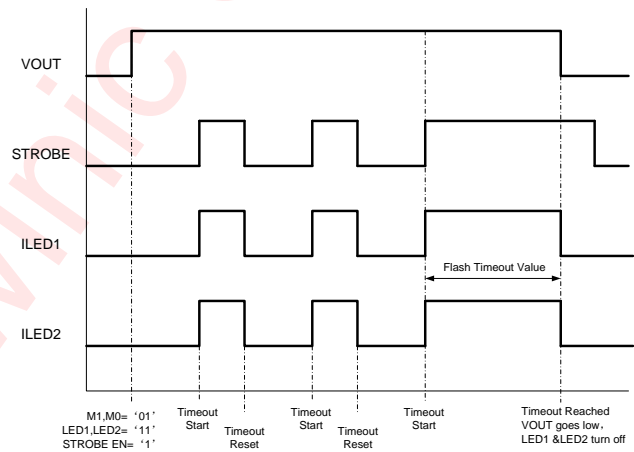


Fig 49 IR Mode Timeout

### SOFT START-UP

Turn on of the AW3644 Torch and Flash modes can be done through the Enable Register. On start-up, when  $V_{OUT}$  is less than  $V_{IN}$  the internal synchronous PMOS turns on as a current source and delivers 200mA (typical) to the output capacitor. During this time the current source (LED) is off. When the voltage across the output

capacitor reaches 2.2 V (typical) the current source turns on. At turn-on the current source steps through each FLASH or TORCH level until the target LED current is reached. This gives the device a controlled turn-on and limits inrush current from the  $V_{IN}$  supply.

### **PASS MODE**

The AW3644 starts up in Pass Mode and stays there until Boost Mode is needed to maintain regulation. In Pass Mode the boost converter does not switch, and the synchronous PMOS turns fully on bringing  $V_{OUT}$  up to  $V_{IN} - I_{LED} \times R_{PMOS}$ . In Pass Mode the inductor current is not limited by the peak current limit. If the voltage difference between  $V_{OUT}$  and  $V_{LED}$  falls below  $V_{HR}$ , the device switches to Boost Mode. By setting bit2 of Boost Configuration Register (0x07) to a '1', AW3644 can be forced into pass mode only state regardless the  $V_{HR}$ , which must be set before system enter Boost mode, once system enter Boost mode, the bit2 of Boost Configuration Register (0x07) is invalid unless setting the device enter standby mode, or by setting the SW RESET bit to a '1', or by removing power to the AW3644.

### **POWER AMPLIFIER SYNCHRONIZATION (TX)**

The TX pin is a Power Amplifier Synchronization input. This is designed to reduce the flash LED current and thus limit the battery current during high battery current conditions such as PA transmit events. When the AW3644 is engaged in a Flash event, and the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed Torch current setting. If the TX pin is then pulled low before the Flash pulse terminates, the LED current returns to the previous Flash current level. At the end of the Flash time-out, whether the TX pin is high or low, the LED current turns off.

The TX input can be disable by setting bit[7] (TX Enable) to a '0' in the Enable Register(0x01).

### **INPUT VOLTAGE FLASH MONITOR (IVFM)**

The AW3644 has the ability to adjust the flash current based upon the voltage level present at the IN pin utilizing the Input Voltage Flash Monitor (IVFM). The adjustable threshold ranges from 2.9 V to 3.6 V in 100mV steps as well as adjustable hysteresis, with three different usage modes (Stop and Hold, Down, Up and Down). The IVFM threshold and hysteresis are controlled by bits[5:3] and bit[2] respectively, in the IVFM Register(0x02). The Flags2 Register has the IVFM flag bit set when the input voltage crosses the IVFM threshold value. Additionally, the IVFM threshold sets the input voltage boundary that forces the AW3644 to either stop ramping the flash current during startup in Stop and Hold Mode, or to actively adjust the LED current lower in Down Mode, or to continuously adjust the LED current up and down in Up & Down Mode.

- Stop and Hold Mode: Stops Current Ramp and holds the level for the remaining flash, If  $V_{IN}$  falls below the IVFM threshold value.
- Down Mode: Adjust current down if  $V_{IN}$  falls below the IVFM threshold value and stops decreasing once  $V_{IN}$  rises above the IVFM threshold (or plus a hysteresis). The AW3644 will decrease the current throughout the flash pulse anytime  $V_{IN}$  falls below the IVFM threshold, not just once. The flash current will not increase again until the next flash.
- Up & Down Mode: Adjust current down if  $V_{IN}$  falls below the IVFM threshold value and adjusts current up if  $V_{IN}$  rise above the IVFM threshold (or plus a hysteresis). In Up & Down mode, the LED current will continually adjust with the rising and falling of  $V_{IN}$  throughout the entire flash pulse.

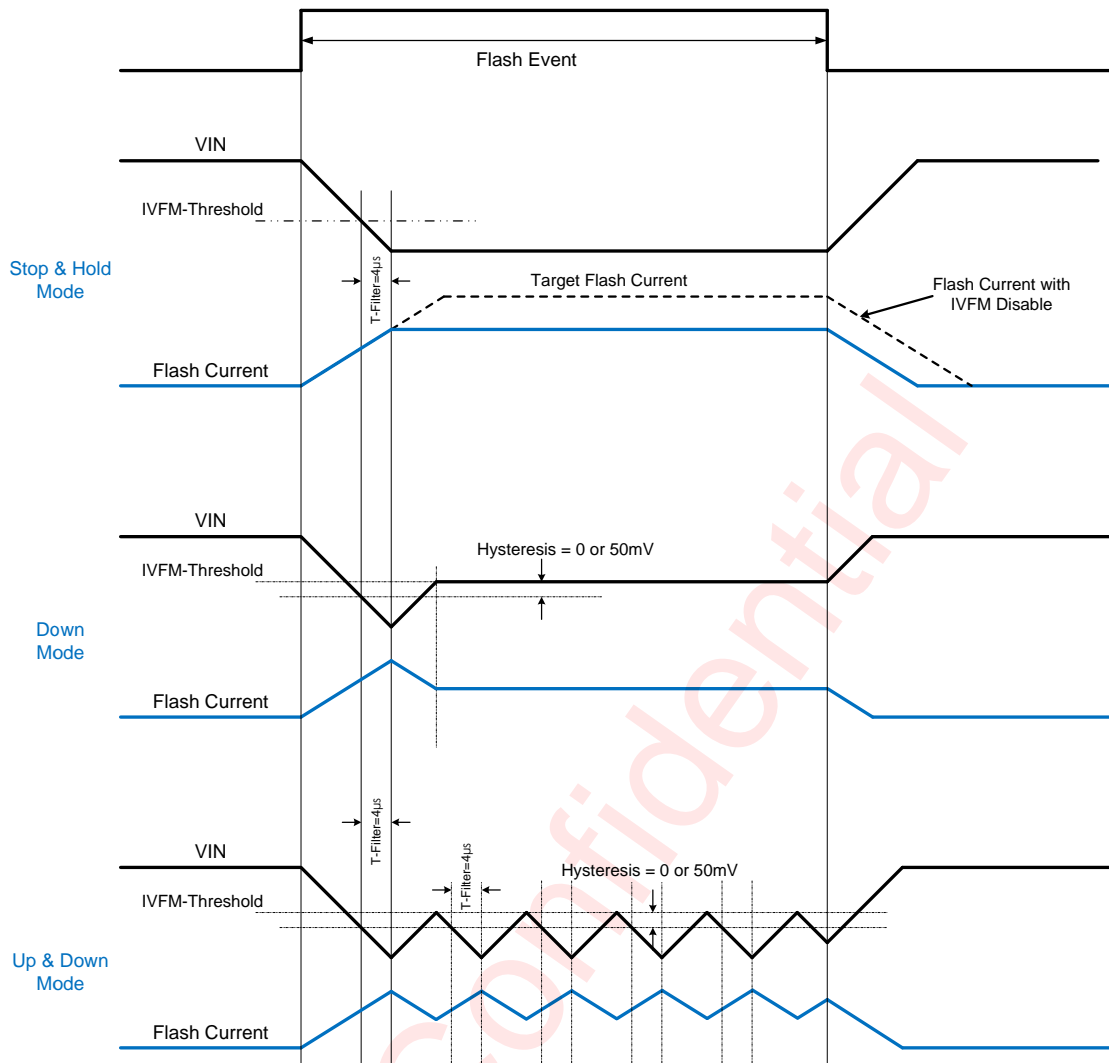


Fig 50 IVFM Modes

### FLASH TIMEOUT

The Flash Timeout period sets the maximum time of one flash event, whether a flash stop command is received or not. The AW3644 has 16 timeout levels ranging from 40ms to 1.6s (see [TIMING CONFIGURATION REGISTER \(0X08\)](#) for more detail). Flash Timeout applies to both Flash and IR modes, and it continues to count when the Flash mode is forced into Torch mode during a TX high event. The mode bits are cleared and bit[0] is set in the Flags1 register(0x0A) upon a Flash Timeout. This fault flag can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting HWEN to '0', or by setting the SW RESET bit to a '1', or by removing power to the AW3644.

### CURRENT LIMIT

When the inductor current limit is reached, the AW3644 terminates the charging phase of the switching cycle until the next switching period. If the over-current condition persists, the device operates continuously in current limit. The AW3644 features two selectable inductor current limits(1.9A and 2.8A) that are programmable by bit[0] in Boost configuration Register(0x07).

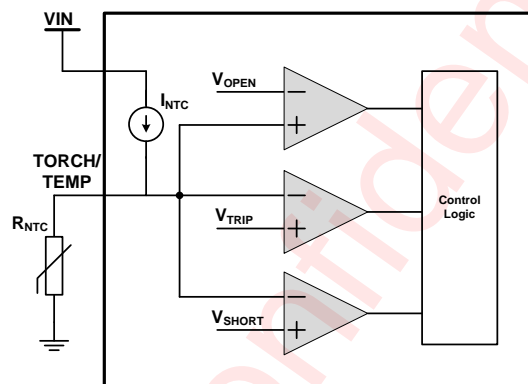
Since the current limit is sensed in the NMOS switch, there is no mechanism to limit the current when the device operates in Pass Mode (current does not flow through the NMOS in pass mode). The mode bits are not cleared upon a Current Limit event, but a flag bit[3] is set in the Flags1 register(0x0A).

This fault flag can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting HWEN to '0', or by setting the SW RESET bit to a '1', or by removing power to the AW3644.

### **NTC THERMISTOR INPUT (TORCH/TEMP)**

The TORCH/TEMP pin, when set to TEMP mode, serves as a threshold detector and bias source for negative temperature coefficient (NTC) thermistors. When the voltage at TEMP goes below the programmed threshold, bit[0] is set to a '1', and the AW3644 is placed into standby mode. The NTC threshold voltage is adjustable from 200 mV to 900 mV in 100-mV steps. The NTC bias current is set to 50µA. The NTC detection circuitry can be enabled or disabled via the Enable Register. If enabled, the NTC block turns on and off during the start and stop of a Flash/Torch event.

Additionally, the NTC input looks for an open NTC connection and a shorted NTC connection. If the NTC input falls below 100 mV, the NTC short flag is set(bit[4] in the Flags2 Register), and the AW3644 is forced into standby mode. If the NTC input rises above 2.3 V, the NTC Open flag is set(bit[3] in the Flags2 Register), and the AW3644 is forced into standby mode. These fault detections can be individually disabled/enabled via the NTC Open Fault Enable bit and the NTC Short Fault Enable bit in Temp register(0x09)



**Fig 51 Temp Detection Diagram**

The AW3644 is not available for operation until Flags2 register is cleared. The three NTC fault flags can be reset to '0' by reading back the Flags2 Register (0x0B), or by setting HWEN to '0', or by setting the SW RESET bit to a '1', or by removing power to the AW3644.

### **UNDERVOLTAGE LOCKOUT (UVLO)**

The AW3644 has an internal comparator that monitors the voltage at IN and forces the AW3644 into standby if the input voltage drops to 2.5 V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in the Flags1 Register (0x0A). If the input voltage rises above 2.5 V, the AW3644 is not available for operation until there is an I<sup>2</sup>C read of the Flags1 Register (0x0A). Upon a read, the Flags1 register is cleared, and normal operation can resume if the input voltage is greater than 2.5 V.

### **VOUT SHORT FAULT**

The Output Short Fault flag reads back a '1' if the device is active in Flash or Torch mode and the boost output experiences a short condition. VOUT short condition occurs if the voltage at OUT goes below 2.3V (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 2.048ms before the VOUT Short flag is valid. The mode bits are cleared upon an the VOUT short fault. The AW3644 is not available for operation until VOUT Fault flags is cleared. The VOUT Short Faults can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting HWEN to '0', or by setting the SW RESET bit to a '1', or by removing power to the AW3644.

**LED SHORT FAULT**

The LED Short Fault flags read back a '1' if the device is active in Flash or Torch mode and either active LED output experiences a short condition. An LED short condition is determined if the voltage at LED1 or LED2 goes below 500mV (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 256 $\mu$ s before the LED Short Fault flag is valid. The mode bits are cleared upon an LED short fault. The AW3644 is not available for operation until the LED Short Fault flags is cleared. The LED Short Faults can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting HWEN to '0', or by setting the SW RESET bit to a '1', or by removing power to the AW3644.

**OVERVOLTAGE PROTECTION (OVP)**

The output voltage is limited to typically 5 V. In situations such as an open LED, the AW3644 raises the output voltage in order to try and keep the LED current at its target value. When VOUT reaches 5 V (typ.) the overvoltage comparator trips and turns off the internal NMOS. When VOUT falls below the "V<sub>OVP</sub> Off Threshold", the AW3644 begins switching again. The mode bits are cleared, and the OVP Fault flag is set, when an OVP condition is present for three rising OVP edges. This prevents momentary OVP events from forcing the device to shut down. The AW3644 is not available for operation until the OVP Fault flag is cleared. The OVP Fault can be reset to '0' by reading back the Flags2 Register (0x0B), or by setting HWEN to '0', or by setting the SW RESET bit to a '1', or by removing power to the AW3644.

**THERMAL SHUTDOWN (TSD)**

When the AW3644 die temperature reaches 155°C, the thermal shutdown detection circuit trips, forcing the AW3644 into standby and writing a '1' to the Thermal Shutdown Fault flag of the Flags1 Register (0x0A) . The AW3644 is only allowed to restart after the Thermal Shutdown Fault flag is cleared. The Thermal Shutdown Faults can be reset to '0' by reading back the Flags1 Register (0x0A), or by setting HWEN to '0', or by setting the SW RESET bit to a '1', or by removing power to the AW3644. Upon restart, if the die temperature is still above 155°C, the AW3644 resets the Fault flag and re-enters standby.

**SOFTWARE RESET**

Writing "1" to the bit7 of Boost Configuration Register (register: 0x07) via I<sup>2</sup>C interface will reset the device, including all internal circuits and configuration registers. After the software reset command is input through I<sup>2</sup>C, it needs to wait at least 2ms before any other I<sup>2</sup>C command can be accepted.

## PROGRAMMING

### CONTROL TRUTH TABLE

| MODE1 | MODE0 | STROBE EN | TORCH EN | STROBE PIN | TORCH PIN | ACTION           |
|-------|-------|-----------|----------|------------|-----------|------------------|
| 0     | 0     | 0         | 0        | X          | X         | Standby          |
| 0     | 0     | 0         | 1        | X          | Pos edge  | Ext Torch        |
| 0     | 0     | 1         | 0        | Pos edge   | X         | Ext Flash        |
| 0     | 0     | 1         | 1        | 0          | Pos edge  | Standalone Torch |
| 0     | 0     | 1         | 1        | Pos edge   | 0         | Standalone Flash |
| 0     | 0     | 1         | 1        | Pos edge   | Pos edge  | Standalone Flash |
| 1     | 0     | X         | X        | X          | X         | Int Torch        |
| 1     | 1     | X         | X        | X          | X         | Int Flash        |
| 0     | 1     | 0         | X        | X          | X         | IRLED Standby    |
| 0     | 1     | 1         | X        | 0          | X         | IRLED Standby    |
| 0     | 1     | 1         | X        | Pos edge   | X         | IRLED enabled    |

### I<sup>2</sup>C INTERFACE

#### Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

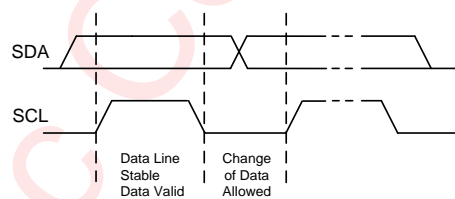


Fig 52 Data Validation Diagram

#### I<sup>2</sup>C Start/Stop

I<sup>2</sup>C start: SDA changes from high level to low level when SCL is high level.

I<sup>2</sup>C stop: SDA changes from low level to high level when SCL is high level.

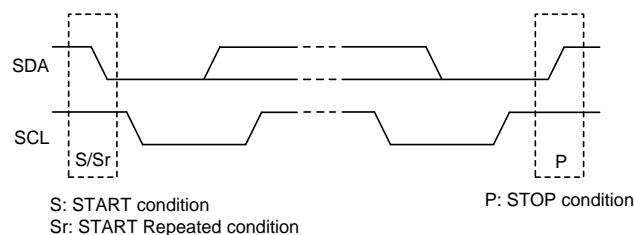


Fig 53 Start and Stop Conditions



### ACK (Acknowledgement)

ACK means the successful transfer of I<sup>2</sup>C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I<sup>2</sup>C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I<sup>2</sup>C stop.

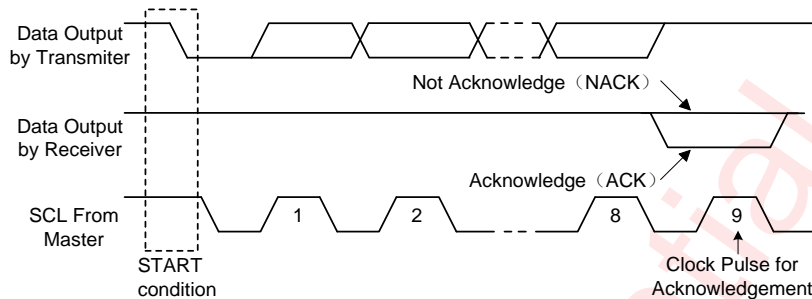


Fig 54 Acknowledgement Diagram

### Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

- Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
- Master device sends slave address (7-bit) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit)
- Slave sends acknowledge signal
- Master sends data byte to be written to the addressed register
- Slave sends acknowledge signal
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6, 7)
- Master generates STOP condition to indicate write cycle end



Fig 55 I<sup>2</sup>C Write Timing

### Read Cycle

In a read cycle, the following steps should be followed:

- a) Master device generates START condition
- b) Master device sends slave address (7-bit) and the data direction bit ( $r/w = 0$ ).
- c) Slave device sends acknowledge signal if the slave address is correct.
- d) Master sends control register address (8-bit)
- e) Slave sends acknowledge signal
- f) Master generates STOP condition followed with START condition or REPEAT START condition
- g) Master device sends slave address (7-bit) and the data direction bit ( $r/w = 1$ ).
- h) Slave device sends acknowledge signal if the slave address is correct.
- i) Slave sends data byte from addressed register.
- j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
- k) If the master device generates STOP condition, the read cycle is ended.

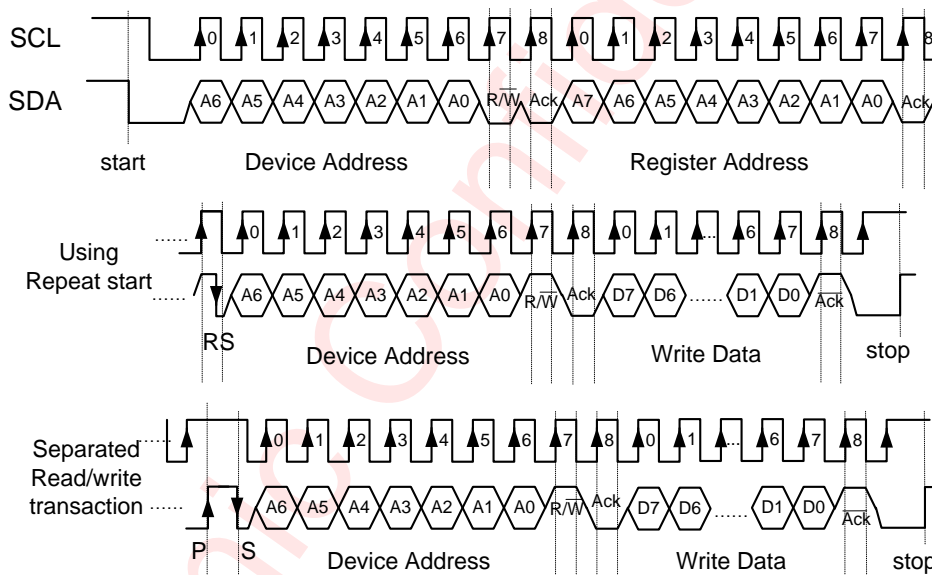


Fig 56 I<sup>2</sup>C Read Timing

## REGISTER CONFIGURATION

### REGISTER LIST

| Register name                  | Address(HEX) | Read/Write | Default Value |
|--------------------------------|--------------|------------|---------------|
| Chip ID Register               | 0x00         | Read       | 0x36          |
| Enable Register                | 0x01         | Read/Write | 0x80          |
| IVFM Register                  | 0x02         | Read/Write | 0x01          |
| LED1 Flash Brightness Register | 0x03         | Read/Write | 0xBF          |
| LED2 Flash Brightness Register | 0x04         | Read/Write | 0x3F          |
| LED1 Torch Brightness Register | 0x05         | Read/Write | 0xBF          |
| LED2 Torch Brightness Register | 0x06         | Read/Write | 0x3F          |
| Boost Configuration Register   | 0x07         | Read/Write | 0x09          |
| Timing Configuration Register  | 0x08         | Read/Write | 0x1A          |
| Temp Register                  | 0x09         | Read/Write | 0x08          |
| Flags1 Register                | 0x0A         | Read       | 0x00          |
| Flags2 Register                | 0x0B         | Read       | 0x00          |
| Device ID Register             | 0x0C         | Read       | 0x02          |
| Last Flash Register            | 0x0D         | Read       | 0x00          |

### REGISTER DETAILED DESCRIPTION

#### ◇ Chip ID Register (0x00)

| Bit 7               | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| Chip ID: "00110110" |       |       |       |       |       |       |       |

#### ◇ Enable Register (0x01)

| Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3   | Bit 2 | Bit 1  | Bit 0  |
|--|--|--|--|---|-------|--|--|
| <b>TX Pin Enable</b><br>0=Disabled<br>1=Enabled<br>(Default) | <b>Strobe Type</b><br>0=Level<br>Triggered<br>(Default)<br>1=Edge<br>Triggered | <b>Strobe Enable</b><br>0=Disabled<br>(Default)<br>1=Enabled | <b>Torch/Temp Pin Enable</b><br>0=Disabled<br>(Default)<br>1=Enabled | <b>Mode Bits: M1, M0</b><br>00=Standby (Default)<br>01=IR Drive<br>10=Torch<br>11=Flash |       | <b>LED2 Enable</b><br>0=OFF<br>(Default)<br>1=ON | <b>LED1 Enable</b><br>0=OFF<br>(Default)<br>1=ON |

#### Note:

In Edge or Level Strobe Mode, it is recommended that the trigger pulse width be set greater than 1ms to ensure proper turn-on of the device.

◇ **IVFM Register (0x02)**

| Bit 7 | Bit 6  | Bit 5  | Bit 4 | Bit 3 | Bit 2   | Bit 1   | Bit 0 |
|-------|--|--|-------|-------|---|---|-------|
| RFU   | <b>UVLO Circuitry</b><br>0=Disabled (Default)<br>1=Enabled | <b>IVFM Levels</b><br>000=2.9 V (Default)<br>001=3.0 V<br>010=3.1 V<br>011=3.2 V<br>100=3.3 V<br>101=3.4 V<br>110=3.5 V<br>111=3.6 V |       |       | <b>IVFM Hysteresis</b><br>0=0 mV (Default)<br>1=50 mV | <b>IVFM Mode Selection</b><br>00=Disabled<br>01=Stop and Hold Mode (Default)<br>10=Down Mode<br>11=Up and Down Mode |       |

◇ **LED1 Flash Brightness Register (0x03)**

| Bit 7  | Bit 6 | Bit 5  | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------|--|-------|-------|-------|-------|-------|
| <b>LED2 Flash Current Override</b><br>0=LED2 Flash Current is not set to LED1 Flash Current<br>1=LED2 Flash Current is set to LED1 Flash Current (Default) |       | <b>LED1 Flash Brightness Levels</b><br>$I_{FLASH}(mA) \approx (\text{Brightness Code} * 11.72mA) + 11.35mA$<br>0000000=11.35 mA<br>.....<br>0111111=746.9 mA (Default)<br>.....<br>1111111=1.5 A |       |       |       |       |       |

◇ **LED2 Flash Brightness Register (0x04)**

| Bit 7 | Bit 6  | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--|-------|-------|-------|-------|-------|-------|
| RFU   | <b>LED2 Flash Brightness Levels</b><br>$I_{FLASH}(mA) \approx (\text{Brightness Code} * 11.72mA) + 11.35mA$<br>0000000=11.35 mA<br>.....<br>0111111=746.9 mA (Default)<br>.....<br>1111111=1.5 A |       |       |       |       |       |       |

◇ **LED1 Torch Brightness Register (0x05)**

| Bit 7  | Bit 6 | Bit 5  | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------|--|-------|-------|-------|-------|-------|
| <b>LED2 Torch Current Override</b><br>0=LED2 Torch Current is not set to LED1 Torch Current<br>1=LED2 Torch Current is set to LED1 Torch Current (Default) |       | <b>LED1 Torch Brightness Levels</b><br>$I_{TORCH}(mA) \approx (\text{Brightness Code} * 2.91mA) + 2.55mA$<br>0000000=2.55 mA<br>.....<br>0111111=186 mA (Default)<br>.....<br>1111111=372 mA |       |       |       |       |       |

◇ **LED2 Torch Brightness Register (0x06)**

| Bit 7 | Bit 6  | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--|-------|-------|-------|-------|-------|-------|
| RFU   | <b>LED2 Torch Brightness Levels</b><br>$I_{TORCH}(mA) \approx (\text{Brightness Code} * 2.91mA) + 2.55mA$<br>0000000=2.55 mA<br>.....<br>0111111=186 mA (Default)<br>.....<br>1111111=372 mA |       |       |       |       |       |       |

◇ **Boost Configuration Register (0x07)**

| Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3   | Bit 2   | Bit 1  | Bit 0   |
|--|-------|-------|-------|---|---|--|---|
| <b>Software Reset Bit</b><br>0=Not Reset<br>(Default)<br>1=Reset | RFU   | RFU   | RFU   | <b>LED Pin Short Fault Detect</b><br>0=Disabled<br>1=Enabled<br>(Default) | <b>Boost Mode</b><br>0=Normal<br>(Default)<br>1=Pass Mode<br>Only | <b>Boost Frequency Select</b><br>0=2 MHz<br>(Default)<br>1=4 MHz | <b>Boost Current Limit</b><br>0=1.9A<br>1=2.8A<br>(Default) |

◇ **Timing Configuration Register (0x08)**

| Bit 7 | Bit 6  | Bit 5 | Bit 4 | Bit 3  | Bit 2 | Bit 1 | Bit 0 |
|-------|--|-------|-------|--|-------|-------|-------|
| RFU   | <b>Torch Current Ramp time</b><br>000=No Ramp<br>001=1 ms (Default)<br>010=32 ms<br>011=64 ms<br>100=128 ms<br>101=256 ms<br>110=512 ms<br>111=1024 ms |       |       | <b>Flash Time-out Duration</b><br>0000=40 ms<br>0001=80 ms<br>0010=120 ms<br>0011=160 ms<br>0100=200 ms<br>0101=240 ms<br>0110=280 ms<br>0111=320 ms<br>1000=360 ms<br>1001=400 ms<br>1010=600 ms (Default)<br>1011=800 ms<br>1100=1000 ms<br>1101=1200 ms<br>1110=1400 ms<br>1111=1600 ms |       |       |       |

◇ **Temp Register (0x09)**

| Bit 7 | Bit 6  | Bit 5  | Bit 4   | Bit 3   | Bit 2 | Bit 1 | Bit 0   |
|-------|--|--|---|---|-------|-------|---|
| RFU   | <b>TORCH Polarity</b><br>0=Active High<br>(Default)<br>(Pull-down Resistor Enabled)<br>1=Active Low<br>(Pull-down Resistor Disabled) | <b>NTC Open Fault Enable</b><br>0=Disabled<br>(Default)<br>1=Enabled | <b>NTC Short Fault Enable</b><br>0=Disabled<br>(Default)<br>1=Enabled | <b>TEMP Detect Voltage Thresholds</b><br>000=200 mV<br>001=300 mV<br>010=400 mV<br>011=500 mV<br>100=600 mV (Default)<br>101=700 mV<br>110=800 mV<br>111=900 mV |       |       | <b>TORCH/TEMP Function Select</b><br>0=TORCH<br>(Default)<br>1=TEMP |

◇ **Flags1 Register (0x0A)**

| Bit 7          | Bit 6                              | Bit 5                   | Bit 4                   | Bit 3                     | Bit 2                               | Bit 1             | Bit 0                      |
|----------------|------------------------------------|-------------------------|-------------------------|---------------------------|-------------------------------------|-------------------|----------------------------|
| <b>TX Flag</b> | <b>V<sub>OUT</sub> Short Fault</b> | <b>LED1 Short Fault</b> | <b>LED2 Short Fault</b> | <b>Current Limit Flag</b> | <b>Thermal Shutdown (TSD) Fault</b> | <b>UVLO Fault</b> | <b>Flash Time-Out Flag</b> |

◇ **Flags2 Register (0x0B)**

| Bit 7 | Bit 6 | Bit 5 | Bit 4                  | Bit 3                 | Bit 2                 | Bit 1            | Bit 0                  |
|-------|-------|-------|------------------------|-----------------------|-----------------------|------------------|------------------------|
| RFU   | RFU   | RFU   | <b>NTC Short Fault</b> | <b>NTC Open Fault</b> | <b>IVFM Trip Flag</b> | <b>OVP Fault</b> | <b>TEMP Trip Fault</b> |

◇ **Device ID Register (0x0C)**

| Bit 7 | Bit 6 | Bit 5              | Bit 4 | Bit 3 | Bit 2                          | Bit 1 | Bit 0 |
|-------|-------|--------------------|-------|-------|--------------------------------|-------|-------|
| RFU   | RFU   | Device ID<br>"000" |       |       | Silicon Revision Bits<br>"010" |       |       |

◇ **Last Flash Register (0x0D)**

| Bit 7 | Bit 6  | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--|-------|-------|-------|-------|-------|-------|
| RFU   | The value stored is always the last current value the IVFM detection block set $I_{LED}=I_{FLASH-TARGET}*((code+1)/128)$ |       |       |       |       |       |       |

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## APPLICATION INFORMATION

The AW3644 can drive two flash LEDs at currents up to 1.5 A per LED. The 2MHz/4MHz DC-DC boost regulator allows for the use of small value discrete external components. Below are some peripheral selection guidelines.

### OUTPUT CAPACITOR SELECTION

The AW3644 is designed to operate with a 10μF ceramic output capacitor. When the boost converter is running, the output capacitor supplies the load current during the boost converter on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

Larger capacitors such as a 22μF or capacitors in parallel can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge ( $\Delta V_Q$ ) and the ripple due to the capacitors ESR ( $\Delta V_{ESR}$ ) use the following equations:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{(V_{OUT} - V_{IN}) \times I_{LED}}{V_{OUT} \times f \times C_{OUT}}$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left( \frac{V_{OUT} \times I_{LED}}{V_{IN}} + \frac{\Delta I_L}{2} \right) \quad \text{Where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f \times L}$$

In ceramic capacitors the ESR is very low so the assumption is that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. Table 1 lists different manufacturers for various output capacitors and their case sizes suitable for use with the AW3644.

### INPUT CAPACITOR SELECTION

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the AW3644 boost converter and reduce noise on the boost converter's input pin that can feed through and disrupt internal analog signals. In the typical application circuit a 10-μF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the AW3644 input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. Table 1 lists various input capacitors recommended for use with the AW3644.

Table 1 Recommended Input/ Output Capacitors (X5R/X7R Dielectric)

| MANUFACTURER | PART NUMBER       | VALUE | CASE | VOLTAGE RATING |
|--------------|-------------------|-------|------|----------------|
| TDK          | C1608JB0J106M     | 10μF  | 0603 | 6.3V           |
| TDK          | C2012JB1A106M     | 10μF  | 0805 | 10V            |
| Murata       | GRM188R60J106M    | 10μF  | 0603 | 6.3V           |
| Murata       | GRM21BR61A106KE19 | 10μF  | 0805 | 10V            |

## INDUCTOR SELECTION

The AW3644 is designed to use a 0.47μH or 1μH inductor. When the device is boosting ( $V_{OUT} > V_{IN}$ ) the inductor is typically the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the AW3644. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the AW3644 are greater than  $I_{PEAK}$  in the following calculation:

$$I_{PEAK} = \frac{I_{LED} \times V_{OUT}}{\eta \times V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

And  $f_{SW}$  =2 or 4MHz.

Table 2 lists various inductors and their manufacturers that work well with the AW3644.

**Table 2 Recommended Inductors**

| MANUFACTURER | L      | PART NO.         | SIZE                     | IsAT | R <sub>Dc</sub> |
|--------------|--------|------------------|--------------------------|------|-----------------|
| TOKO         | 1μH    | DFE201610P-1R0M  | 2.0 mm x 1.6 mm x 1.0 mm | 3.7A | 58mΩ            |
| TOKO         | 0.47μH | DFE201610P-R470M | 2.0 mm x 1.6 mm x 1.0 mm | 4.1A | 32mΩ            |
| Sunlord      | 1μH    | WPN252012H1R0MT  | 2.5mm x 2.0mm x1.2mm     | 3.4A | 48mΩ            |



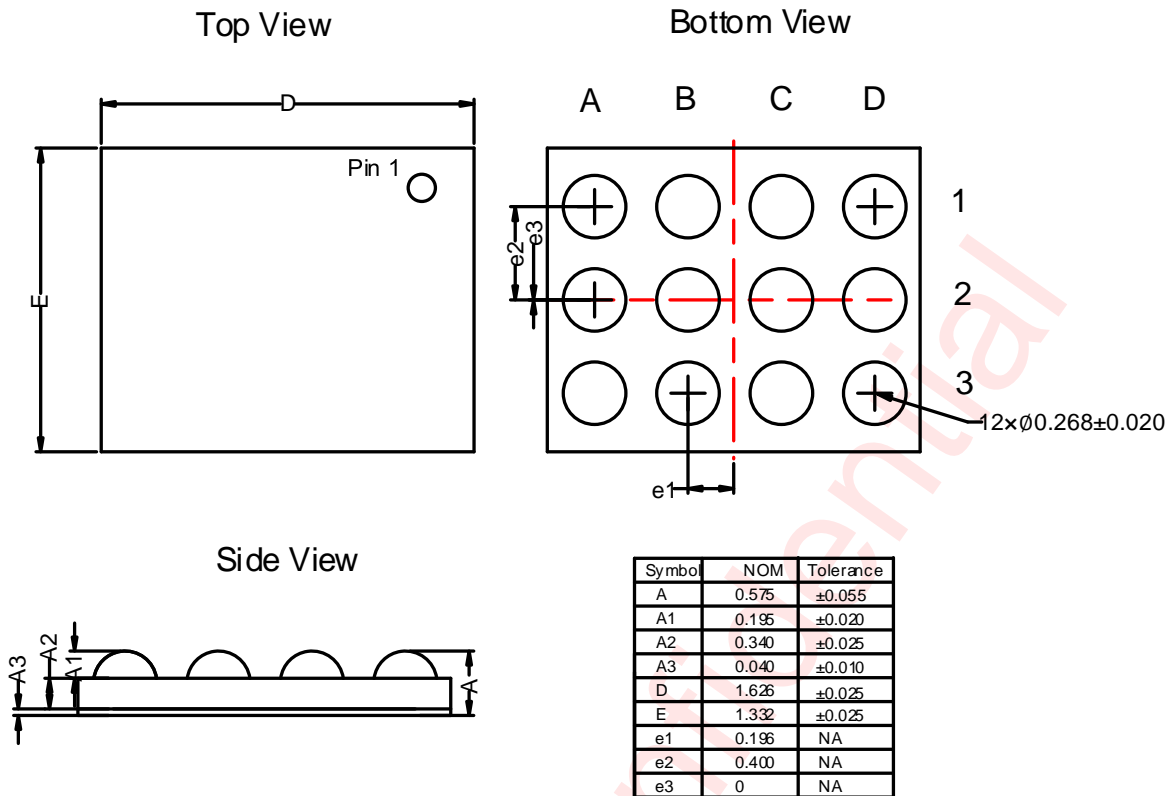
## PCB LAYOUT

### LAYOUT GUIDELINES

The high switching frequency and large switching currents of the AW3644 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

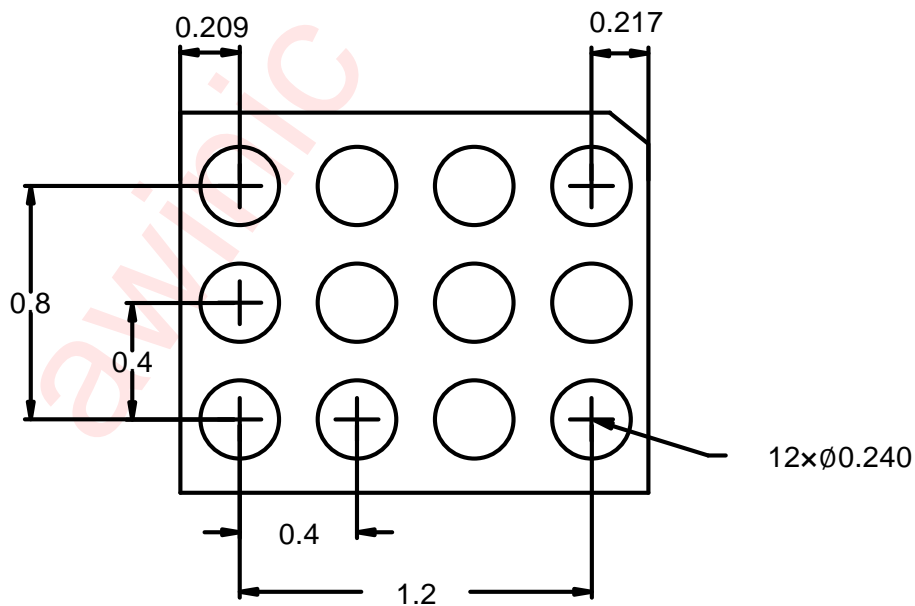
1. Place  $C_{IN}$  on the top layer (same layer as the AW3644) and as close to the device as possible. The input capacitor conducts the driver currents during the low-side MOSFET turn-on and turn-off and can detect current spikes over 1 A in amplitude. Connecting the input capacitor through short, wide traces to both the IN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the  $V_{IN}$  line.
2. Place  $C_{OUT}$  on the top layer (same layer as the AW3644) and as close as possible to the OUT and GND pin. The returns for both  $C_{IN}$  and  $C_{OUT}$  should come together at one point, as close to the GND pin as possible. Connecting  $C_{OUT}$  through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the  $V_{OUT}$  and GND lines and cause excessive noise in the device and surrounding circuitry.
3. Connect the inductor on the top layer close to the SW pin. There should be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node should be small so as to reduce the capacitive coupling of the high  $dV/dT$  present at SW that can couple into nearby traces.
4. Avoid routing logic traces near the SW node so as to avoid any capacitive coupling from SW onto any high-impedance logic lines such as TORCH/TEMP, STROBE, HWEN, SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
5. Terminate the Flash LED cathodes directly to the GND pin of the AW3644. If possible, route the LED returns with a dedicated path so as to keep the high amplitude LED currents out of the GND plane. For Flash LEDs that are routed relatively far away from the AW3644, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current paths.

## PACKAGE DESCRIPTION



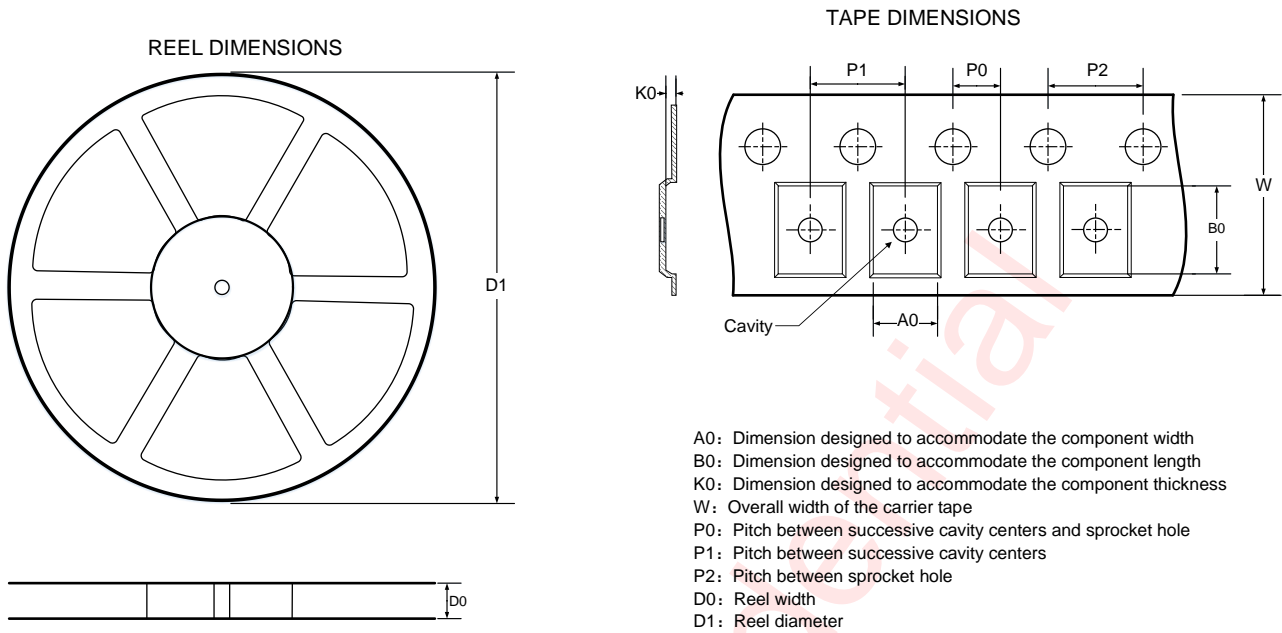
Note: All dimensions are in millimeter(mm).

## LAND PATTERN DATA

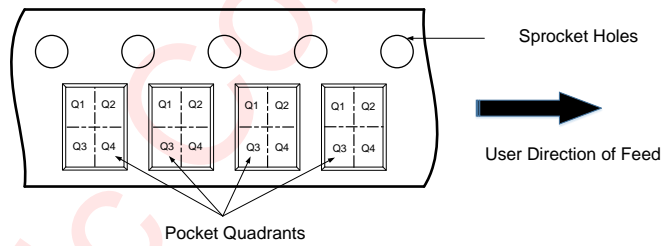


Note: All dimensions are in millimeter(mm).

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal

| D1<br>(mm) | D0<br>(mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P0<br>(mm) | P1<br>(mm) | P2<br>(mm) | W<br>(mm) | Pin1 Quadrant |
|------------|------------|------------|------------|------------|------------|------------|------------|-----------|---------------|
| 179        | 9          | 1.5        | 1.78       | 0.78       | 2          | 4          | 4          | 8         | Q1            |

## REVISION HISTORY

| Vision | Date       | Change Record   |
|--------|------------|---|
| V1.0   | April 2016 | Product Datasheet V1.0 Released   |
| V1.1   | Sep 2016   | Added ESD CDM Information<br>Changed LED1 Flash Brightness Level 0111111 to 746.9mA --page27<br>Changed LED2 Flash Brightness Level 0111111 to 746.9mA --page27 |
| V1.2   | Jan 2017   | Added Awinic Flash Led Driver Series --page3  |
| V1.3   | May 2017   | Added HWEN & I <sup>2</sup> C Interface Description --page17  |
| V1.4   | Jan 2018   | Add Moisture Sensitivity Level and Environmental Information. --page3   |
| V1.5   | July 2018  | 1. Updated Absolute Maximum Ratings --page5<br>2. Updated Tape and Reel Information --page35  |
| V1.6   | Sep 2018   | 1. Updated Feature Description --page 17  |
| V1.7   | June 2019  | 1. Added SOFT RESET description --page 18<br>2. Added the Software Reset definition --page23  |
| V1.8   | July 2021  | 1. Update the torch mode description --page18   |

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