Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

FEATURES

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- Ultra low current=7.8mA;
- Ultra low noise figure(NF)=0.9dB;
- High power gain=18.9dB;
- High input 1dB-compression point=-10.5dBm;
- GPS L1 requires only one input matching inductor;
- RF output internally matched to 50 ohm for GPS L1;
- Supply voltage: 1.5V to 3.3V;
- Operating frequencies: 1550~1615MHz; 1164~1215MHz;
- DFN 1.1 mmX0.9 mmX0.45 mm-6L package
- ±3kV HBM ESD protection (including RFIN and RFOUT pin)

APPLICATIONS

- Smart Phones, Feature Phones;
- Tablet PCs;
- Personal Navigation Devices;
- Digital Still Cameras, Digital Video Cameras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

GENERAL DESCRIPTION

The AW15245DNR is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, Beidou, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW15245DNR can be close to the antenna, requires only one external input matching inductor for GPS L1, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.

The AW15245DNR with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.3V. All these features make AW15245DNR an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provide better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.

The AW15245DNR is available in a small lead-free, RoHS-Compliant, DFN 1.1 mm X 0.9 mm X 0.45 mm-6L package.

TYPICAL APPLICATION CIRCUIT

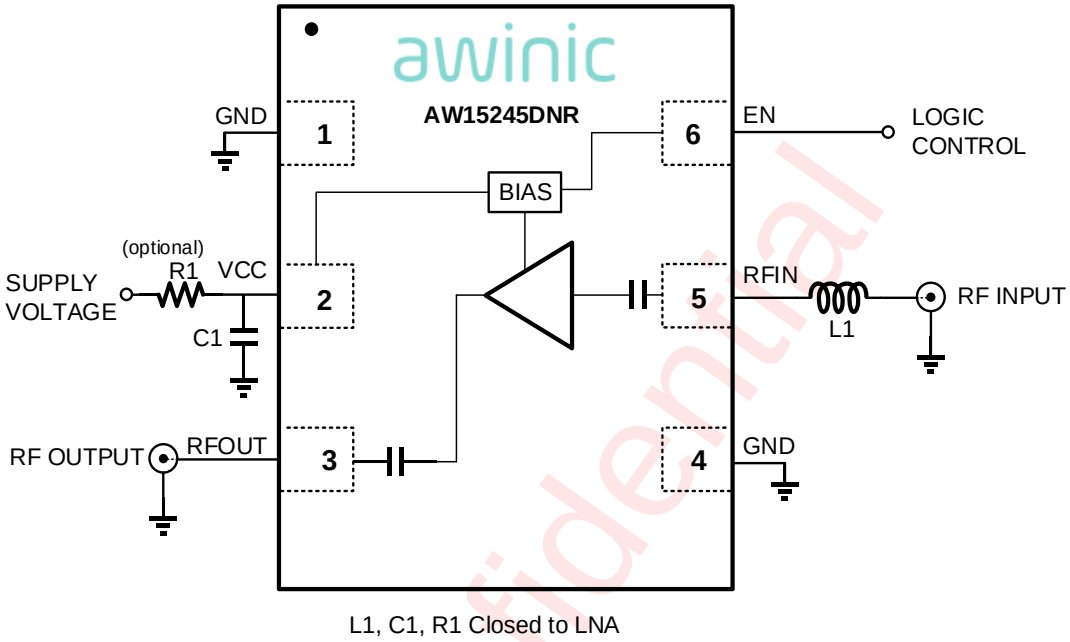


Figure 1(a) Typical Application Circuit of AW15245DNR for GPS L1

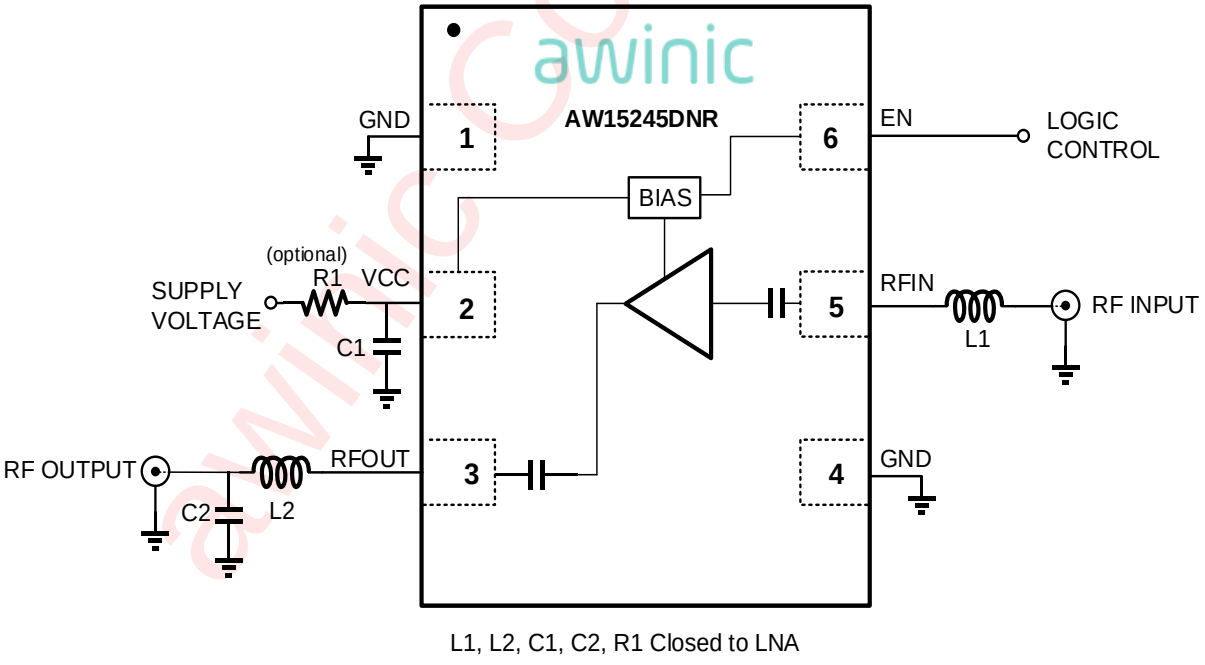


Figure 1(b) Typical Application Circuit of AW15245DNR for GPS L5

RECOMMENDED COMPONENTS LIST

Table1 and talble2 list the recommended inductor types and values; Table 3 lists the recommended capacitor types and values.

Table1: list of inductor for GPS L1

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	10	25	250	Murata	0402
L1	SDWL1005C	10	24	250	Sunlord	0402

Table2: list of inductor for GPS L5

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	18	25	250	Murata	0402
L2	LQW15A	8.7	25	250	Murata	0402

Table2: list of capacitor

Component	Part Number	Capacitance	Rated Voltage	Supplier	Size
	Units	pF	V		
C1	GRM155	1000	50	Murata	0402
C2	GRM155	1.5	50	Murata	0402

PIN CONFIGURATION AND TOP MARK

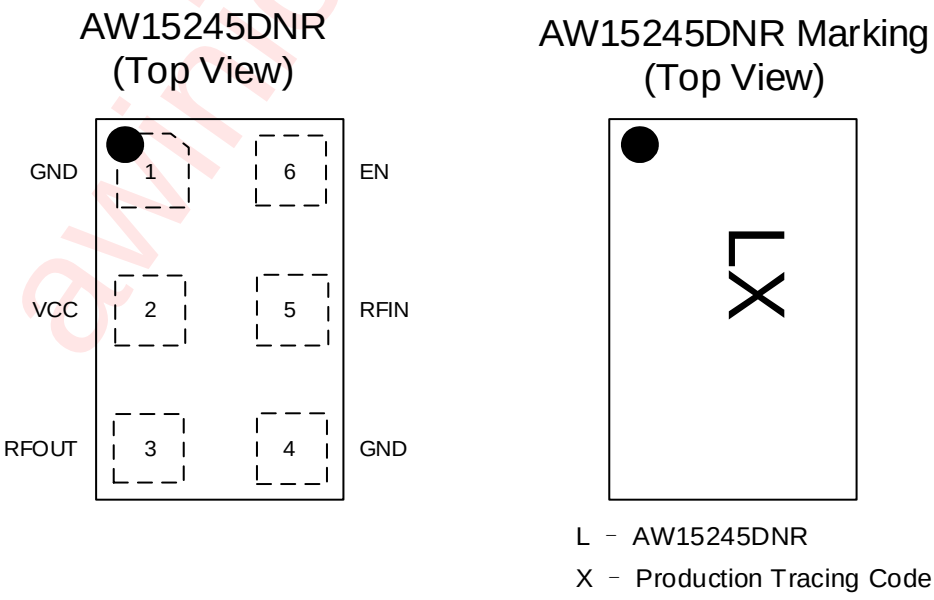


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	DC Supply
3	RFOUT	LNA output
4	GND	Ground
5	RFIN	LNA input
6	EN	Logic control

FUNCTIONAL BLOCK DIAGRAM

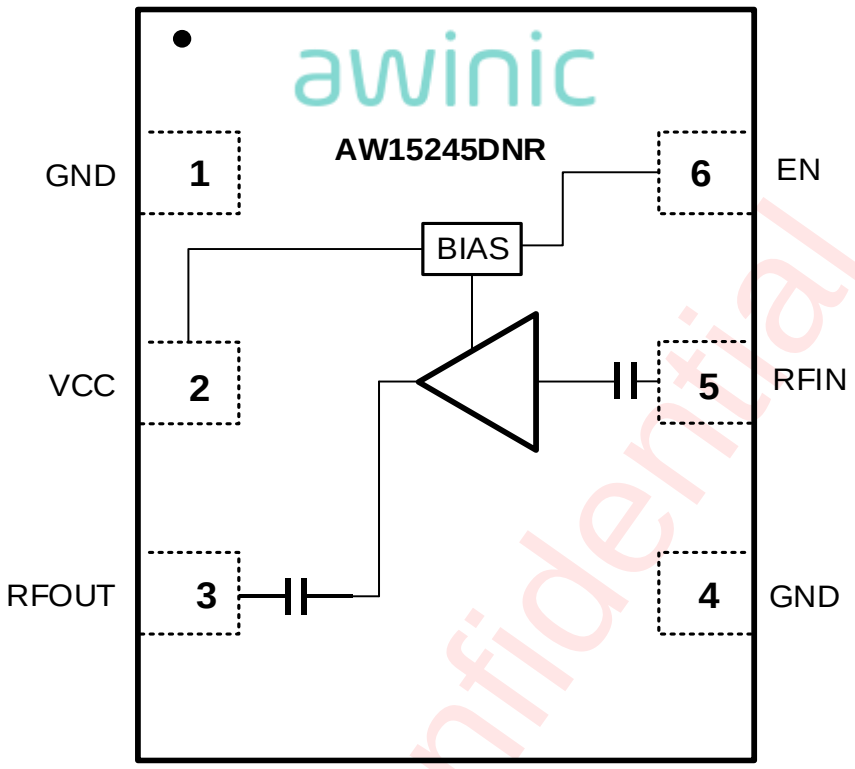


Figure 3 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15245DNR	-40°C ~ 85°C	DFN 1.1mmx0.9mm-6L	L	MSL1	ROHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETERS	SYMBOL	MIN	TYP	MAX	Unit
Supply Voltage at pin VCC	VCC	-0.3	-	3.6	V
Voltage at pin EN [2]	VEN	-0.3	-	3.6	V
RF input power [3]	PIN	-	-	10	dBm
Storage temperature range	T_{STG}	-65	-	150	℃
Ambient temperature range	T_{amb}	-40	-	85	℃
Solder temperature(10s)		-	260	-	℃
ESD RANGE					
HBM [4]		±3000			V
CDM [4]		±2000			V
LATCH-UP					
Test condition: JESD78E		+IT: +200 -IT: -200			mA mA

***Note1**: Stresses beyond those listed under "absolute maximum ratings" Nov cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods Nov affect device reliability.*

***Note2:** Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 3.6V in order to avoid excess current.*

***Note3**: The RF input and RF output are AC coupled through internal DC blocking capacitor.*

***Note4**: HBM standard: ESDA/JEDEC JS-001-2017. CDM standard: ESDA/JEDEC JS-002-2018.*

ELECTRICAL CHARACTERISTICS

(AW15245DNR EVB[1]; Typical values are at VCC=V_{EN}=2.8V and TA=+25°C, f=1575.42MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High		7.8	12	mA
V_{EN}	Digital Input-Logic High		1.0		Vcc	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		17.5	18.9	20.5	dB
RL_{in}	Input Return Loss		8	10		dB
RL_{out}	Output Return Loss		10	16		dB
ISL	Reverse Isolation		20	27		dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer		0.9	1.2	dB
Kf	Stability factor	f=20MHz…10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-12	-10.5		dBm

$IIP3_{ib}$	Inband input
	3^{rd}-order intercept point
		f1=1574.42MHz;
		f2=1575.42MHz;
		Pin=-25dBm;
			-5	-2		dBm

$IIP3_{oob}$	Out-of-band input
	3^{rd}-order intercept point[3]
		f1=1713MHz;
		f2=1851MHz;
		Pin_f1=-20dBm;
		Pin_f2=-65dBm;
			-3	-1		dBm

H2-input referred	Out-of-band input 2^{nd}-ord intercept point	f=787.76MHz Pin=-25dBm		-63		dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain			2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain			1	μs

Note1: *input matched to 50 ohm using a high quality-factor 10nH inductor.*

Note2: *PCB losses are subtracted.*

Note3: *IP3=P1+(P2+$Gain_{1575MHZ}$-IM3)/2*

(AW15245DNR EVB[1]; Typical values are at VCC=V_{EN}=1.8V and TA=+25°C, f=1575.42MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High		6.7	10	mA
V_{EN}	Digital Input-Logic High		1.0		Vcc	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		17	18.4	20	dB
RL_{in}	Input Return Loss		8	9.5		dB
RL_{out}	Output Return Loss		10	16		dB
ISL	Reverse Isolation		20	27		dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer		0.9	1.2	dB
Kf	Stability factor	f=20MHz…10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-14	-12.5		dBm

$IIP3_{ib}$	Inband input
	3^{rd}-order intercept point
		f1=1574.42MHz;
		f2=1575.42MHz;
		Pin=-25dBm;
			-5.5	-3.5		dBm

$IIP3_{oob}$	Out-of-band input
	3^{rd}-order intercept point[3]
		f1=1713MHz;
		f2=1851MHz;
		Pin_f1=-20dBm;
		Pin_f2=-65dBm;
			-5	-3		dBm

H2-input referred	Out-of-band input 2^{nd}-ord intercept point	f=787.76MHz Pin=-25dBm		-63		dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain			2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain			1	μs

***Note1**: input matched to 50 ohm using a high quality-factor 10nH inductor.*

***Note2**: PCB losses are subtracted.*

***Note3**: IP3=P1+(P2+$Gain_{1575MHZ}$-IM3)/2.*

(AW15245DNR EVB[1]; Typical values are at VCC=V_{EN}=2.8V and TA=+25°C, f=1176.45MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High		7.8	12	mA
V_{EN}	Digital Input-Logic High		1.0		Vcc	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		17.5	18.5	20	dB
RL_{in}	Input Return Loss		7	9		dB
RL_{out}	Output Return Loss		10	18		dB
ISL	Reverse Isolation		20	29.5		dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer		0.9	1.2	dB
Kf	Stability factor	f=20MHz…10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-15	-13.1		dBm

$IIP3_{ib}$	Inband input
	3^{rd}-order intercept point
		f1=1176.45MHz;
		f2=1177.45MHz;
		Pin=-30dBm;
			-5.6	-3.6		dBm

$IIP3_{oob}$	Out-of-band input
	3^{rd}-order intercept point
		f1=1800MHz;
		f2=2400MHz;
		Pin_f1=-30dBm;
			-9	-7.3		dBm

ton	turn-on time	time from VEN ON to 90% of the final gain			2	μs
toff	turn-off time	time from VEN OFF to 10% of the gain			1	μs

***Note1**: input matched to 50 ohm using a high quality-factor 18nH inductor. Output matching using 9.1nH inductor and 1.5pF capacitor.*
***Note2**: PCB losses are subtracted.*

(AW15245DNR EVB[1]; Typical values are at VCC=V_{EN}=1.8V and TA=+25°C, f=1176.45MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High		6.7	10	mA
V_{EN}	Digital Input-Logic High		1.0		Vcc	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		17	17.7	20	dB
RL_{in}	Input Return Loss		6.5	8.5		dB
RL_{out}	Output Return Loss		10	18		dB
ISL	Reverse Isolation		20	29		dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer		0.9	1.2	dB
Kf	Stability factor	f=20MHz…10GHz	1			
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-16	-14.3		dBm

$IIP3_{ib}$	Inband input
	3^{rd}-order intercept point
		f1=1176.45MHz;
		f2=1177.45MHz;
		Pin=-30dBm;
			-7.2	-5.2		dBm

$IIP3_{oob}$	Out-of-band input
	3^{rd}-order intercept point
		f1=1800MHz;
		f2=2400MHz;
		Pin_f1=-30dBm;
			-11	-9		dBm

ton	turn-on time	time from VEN ON to 90% of the final gain			2	μs
toff	turn-off time	time from VEN OFF to 10% of the gain			1	μs

***Note1**: input matched to 50 ohm using a high quality-factor 18nH inductor. Output matching using 9.1nH inductor and 1.5pF capacitor.*
***Note2**: PCB losses are subtracted.*

TEST CIRCUITS

DC Characteristics

The following is the test bench for power supply, pin voltage, supply current, standby current

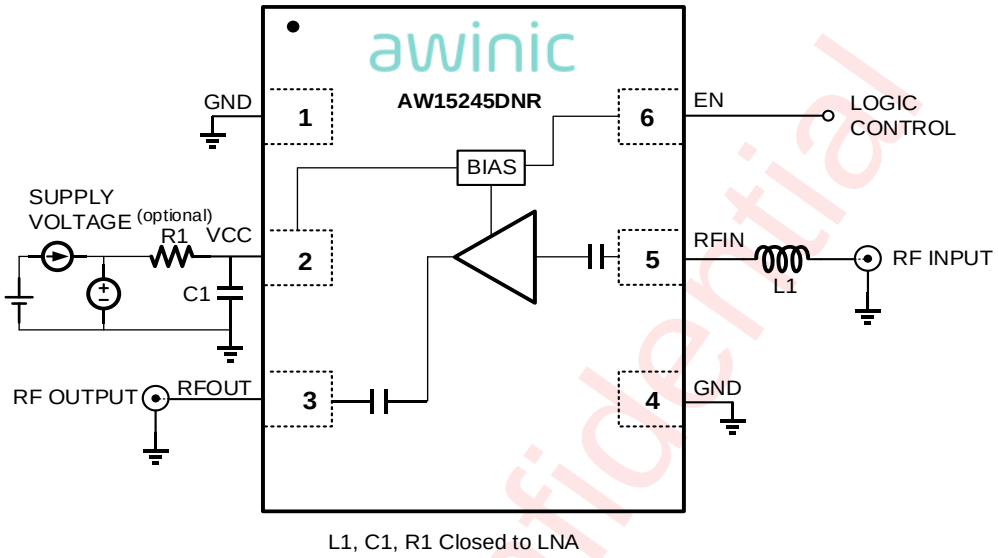


Figure 4 Test Circuits

S Parameter

The following is the test bench for input return loss, output return loss, reverse isolation, forward gain, and 1dB gain compression.

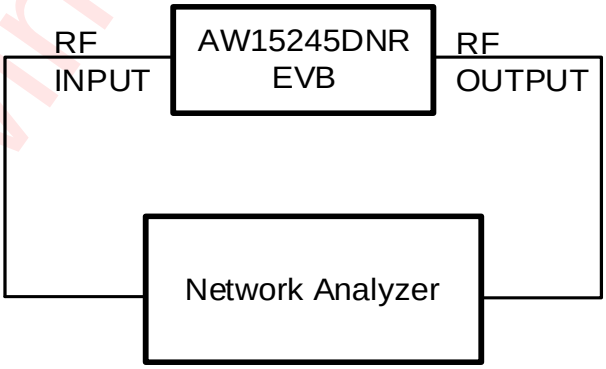


Figure 5 S Parameter Test Bench

Noise Figure

The following is the test bench for noise figure, power gain.

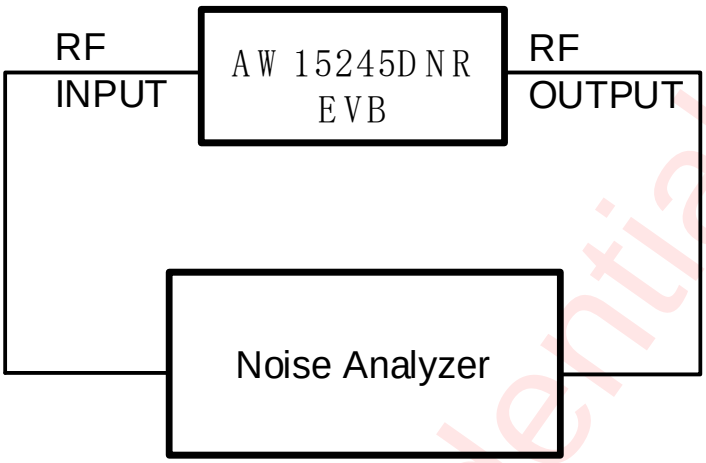


Figure 6 Noise Figure Test Bench

Intermodulation distortion

The following is the test bench for third-order intercept point and second-order intercept point.

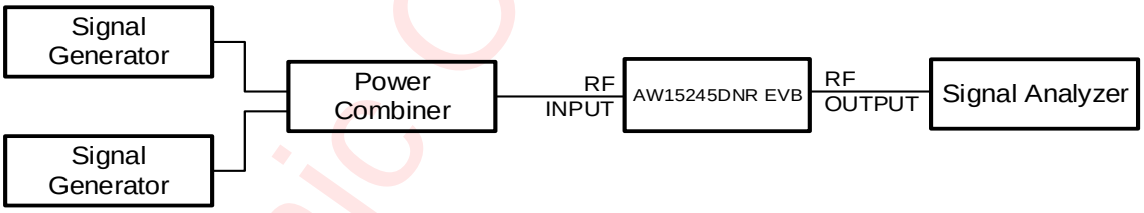
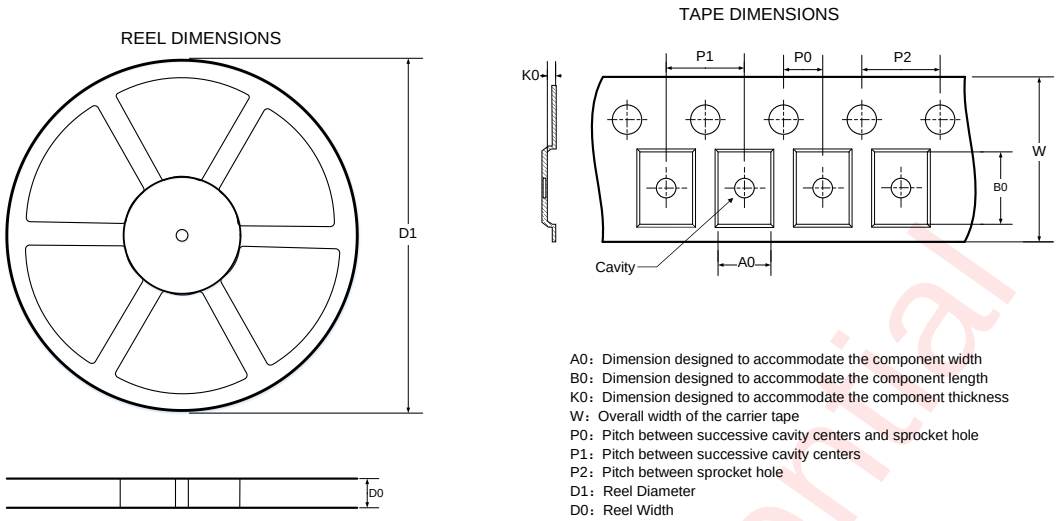
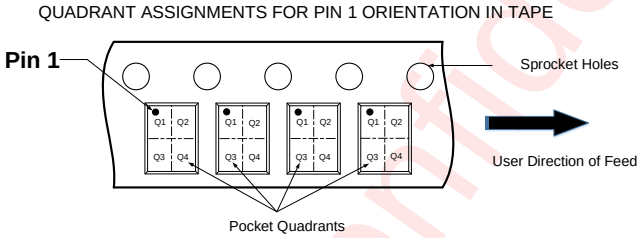


Figure 7 IIP3 Test Bench

TAPE & REEL DESCRIPTION



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.02	1.22	0.6	2	4	4	8	Q1

All dimensions are nominal

Figure 8 Tape & Reel Description

Package Description

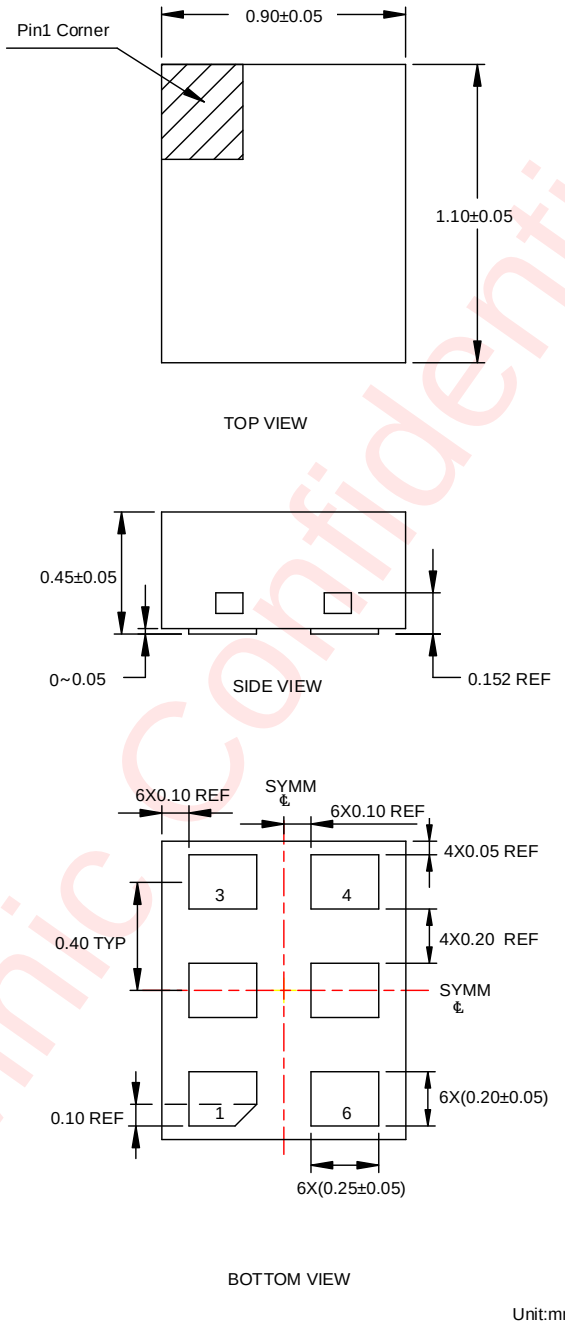
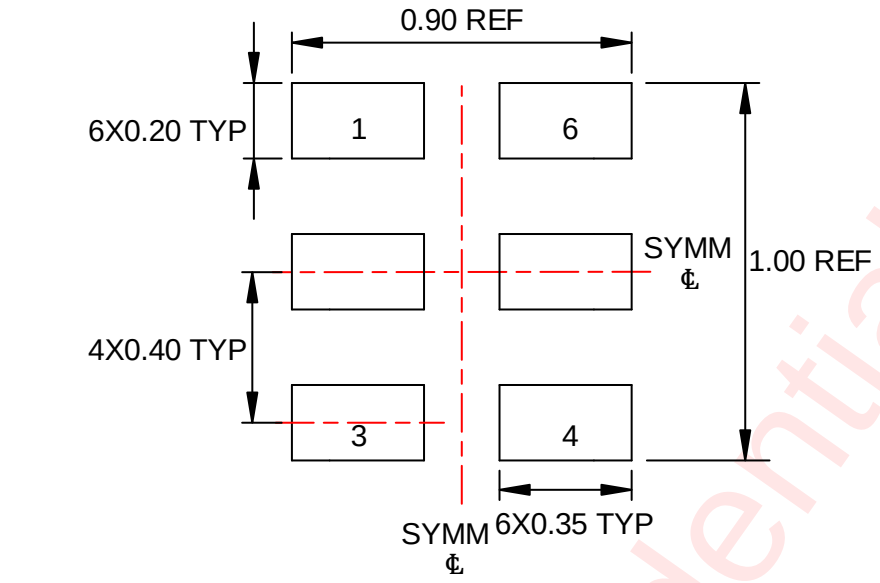
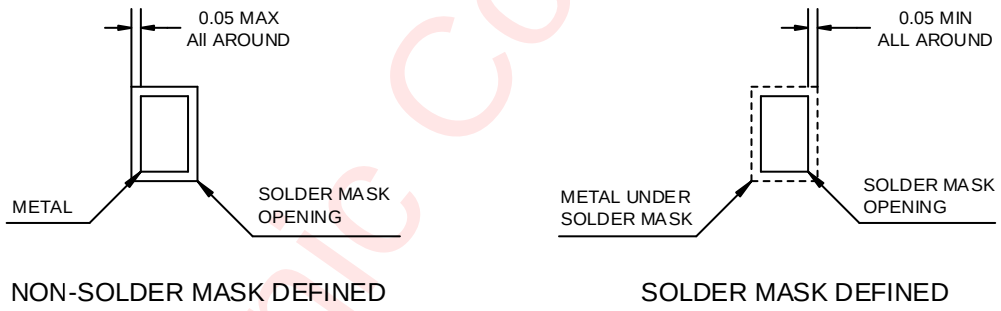


Figure 9 Package Outline

LAND PATTERN





Unit: mm

Figure 10 Land Pattern

REVISION HISTORY

Version	Date	Change Record
V1.0	Nov. 2020	Officially Released
V1.1	Nov. 2020	Added P1dB/ $IIP3_{ib}$ / $IIP3_{oob}$ OF L5 BAND
V1.2	Mar. 2021	Added H2-input referred
V1.3	Feb. 2022	1. The input and output matching inductance of L5 is modified 2. The typical value of NF is modified 3. Some formats have been modified
V1.4	May. 2023	Delete the IMD3 in the EC table

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