# I²S/TDM Input, High Efficiency, 6.25V BOOST Digital Smart K Audio Amplifier with SKTune Algorithm

## FEATURES

- **Integrates SKTune Algorithm**
  - **Bass Booster**
  - **Parametric Equalizer**
  - **Dynamic Range Control**
  - **Anti-clip Voltage Limiter**
  - **Speaker Membrane Excursion and Temperature Protection**
- **Smart BOOST with total efficiency up to 86%**
- **High RF noise suppression, eliminate the TDD noise**
- **Low noise: 10μV**
- **THD+N: 0.006%**
- Supports 4Ω Speaker
- Extensive Pop-Click Suppression
- Volume control (from -96dB to 0dB)
- I²S/TDM interface:
  - I²S, Left-Justified and Right-Justified
  - Supports 1/2/4/6/8 slots TDM
  - Input Sample Rates from 8kHz to 96kHz
  - Data Width: 16, 20, 24, 32 Bits
- Ultrasonic support via TDM/I²S running at 96kHz
- I²C-bus control interface(≤1MHz)
- Power Supplies:
  - VBAT: 3.0V~5.5V
  - DVDD: 1.65V~1.95V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- FCQFN 2.0mmX2.5mmX0.55mm-22L Package

## APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

## DESCRIPTION

The AW88166 is an I²S/TDM input, high efficiency digital Smart K audio amplifier with an integrated 6.25V smart boost converter, sound quality enhancement algorithm and speaker protection. Due to its 10μV noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 2.1W output power into an 8Ω speaker at 1% THD+N.

The AW88166 integrates SKTune algorithm that include parametric audio path equalizer, dynamic range control, anti-clip voltage limiter and speaker protection. The SKTune algorithm maximizes speaker performance while maintaining safe speaker conditions.

The AW88166 integrates a high-efficiency smart boost converter as the Class-D amplifier supply rail. The output voltage of boost converter can be adjusted smartly according to the input amplitude, which extremely improves the efficiency without clipping distortion.

The AW88166 features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface. General settings are communicated via an I²C-bus interface, and the device address is configurable.

The AW88166 offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

AW88166 is available in a FCQFN Package, body size is 2.0mmX2.5mmX0.55mm-22L.



## PIN CONFIGURATION AND TOP MARK

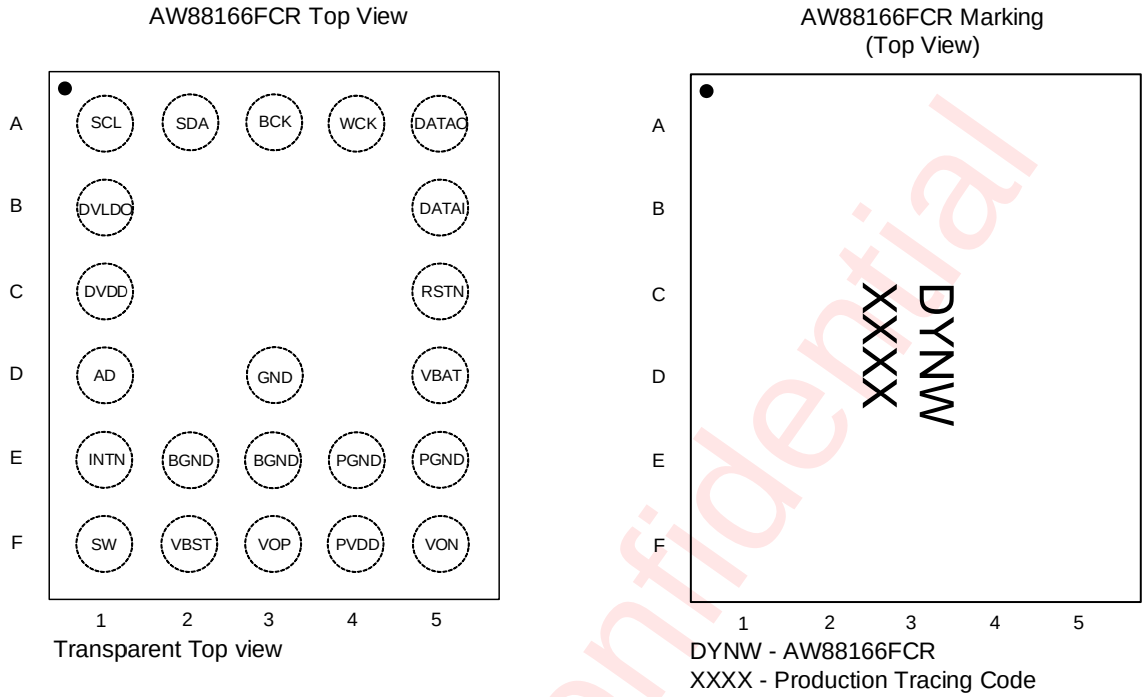



**Figure 1 AW88166FCR pin diagram top view and device marking**

## PIN DESCRIPTION

| Pin No | Pin Name | Description |
|---|---|---|
| A1 | SCL | I²C clock input |
| A2 | SDA | I²C data IO |
| A3 | BCK | I²S/TDM bit clock input |
| A4 | WCK | I²S word select input / TDM frame sync signal |
| A5 | DATAO | I²S/TDM data out |
| B1 | DVLDO | Digital core voltage regulator output |
| B5 | DATAI | I²S/TDM data input |
| C1 | DVDD | Digital power supply |
| C5 | RSTN | Active low hardware reset |
| D1 | AD | I²C device address selection |
| D3 | GND | GND |
| D5 | VBAT | Battery power supply |
| E1 | INTN | Interrupt output |



| | | |
|---|---|---|
| E2,E3 | BGND | Boost GND |
| E4,E5 | PGND | Power GND |
| F1 | SW | Boost switch pin |
| F2 | VBST | Boost output |
| F3 | VOP | Non-inverting Class-D output |
| F4 | PVDD | Class-D power supply voltage |
| F5 | VON | Inverting Class-D output |



## FUNCTIONAL BLOCK DIAGRAM

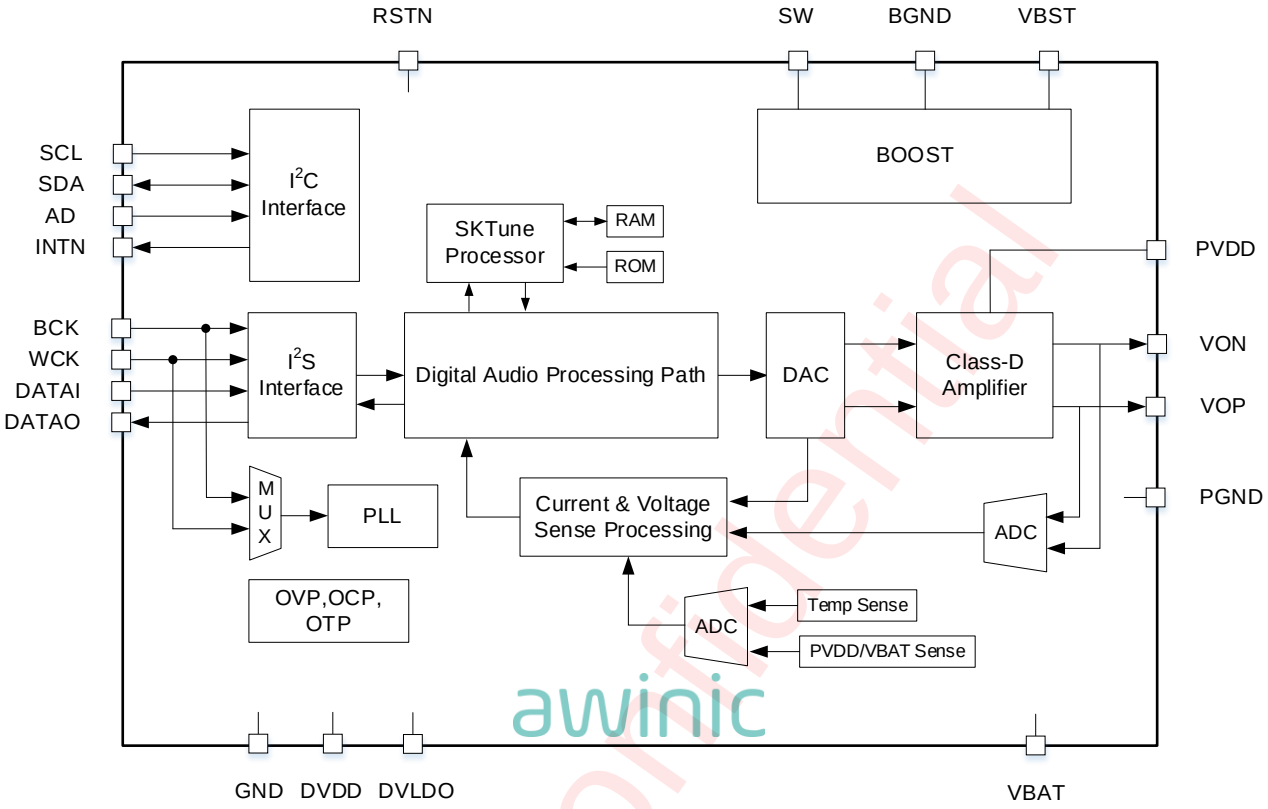



**Figure 2 FUNCTIONAL BLOCK DIAGRAM**



## APPLICATION DIAGRAM

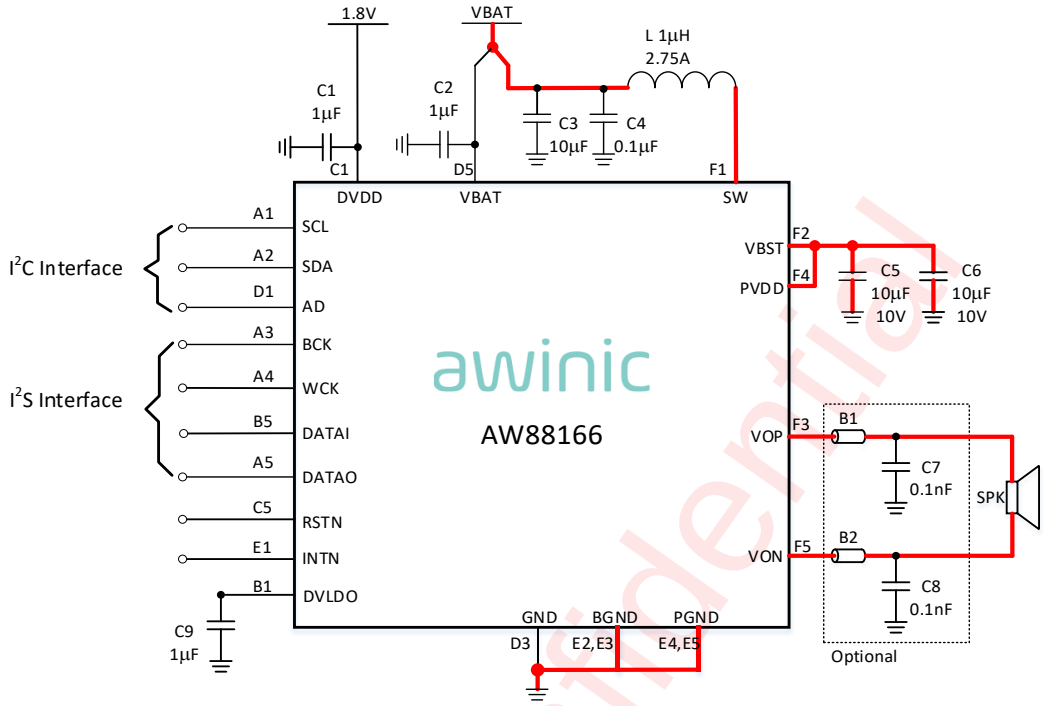



**Figure 3 AW88166 Application Circuit**

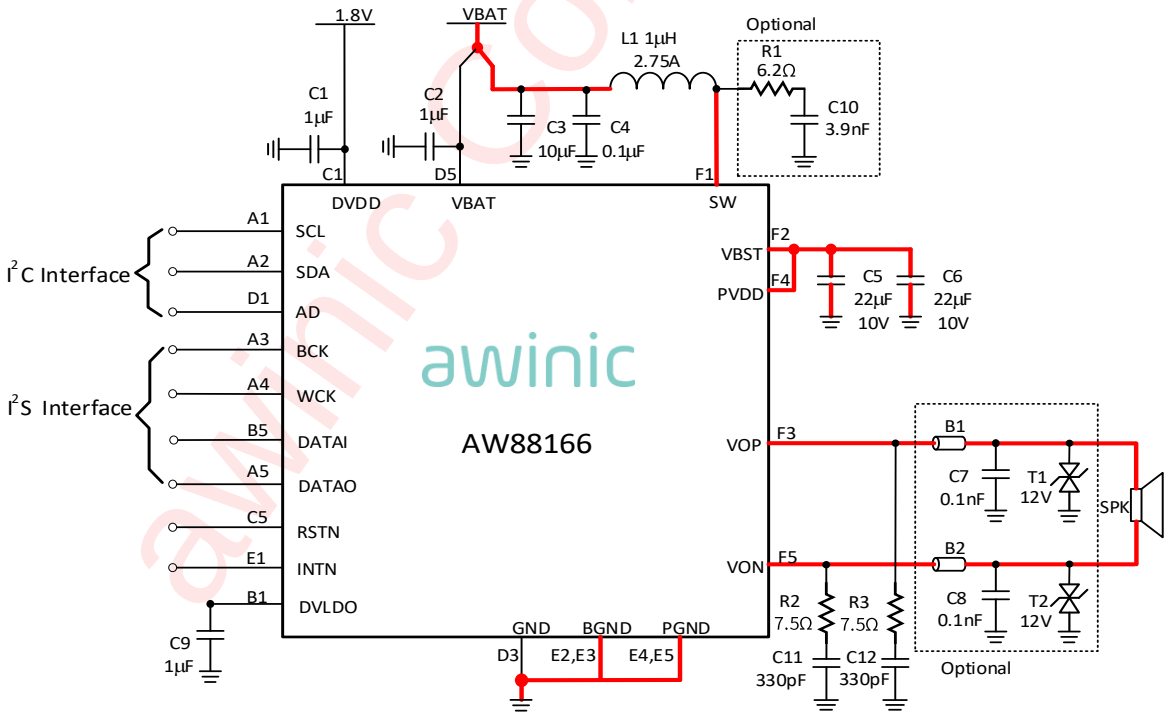



**Figure 4 AW88166 Application Circuit (4Ω Load application)**

Note: Traces carry high current are marked in red in the above figure



## ORDERING INFORMATION

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|---|---|---|---|---|---|---|
| AW88166FCR | -40℃～85℃ | FCQFN 2mmX2.5mmX 0.55mm-22L | DYNW | MSL1 | ROHS+HF | 6000 units/ Tape and Reel |



## ABSOLUTE MAXIMUM RATING[NOTE1]

| Parameter | Range |
|---|---|
| Battery Supply Voltage $V_{BAT}$ | -0.3V to 6V |
| Digital Supply Voltage $V_{DVDD}$ | -0.3V to 1.95V |
| Boost output voltage $V_{PVDD}$ | -0.3 to 6.75V |
| Boost SW pin voltage | -0.3 to $V_{PVDD}$+2V |
| Minimum load resistance $R_L$ | 3.2Ω [Note 2] |
| Package Thermal Resistance $\theta_{JA}$ | 55.1°C/W |
| Ambient Temperature Range | -40°C to 85°C |
| Maximum Junction Temperature $T_{JMAX}$ | 165°C |
| Storage Temperature Range $T_{STG}$ | -65°C to 150°C |
| Lead Temperature (Soldering 10 Seconds) | 260°C |
| ESD Rating[Note 3,4] | |
| HBM (Human Body Model) | ±2000V |
| CDM (Charge Device Model) | ±1500V |
| Latch-up | |
| Test Condition: JESD78E | +IT: 450mA<br>-IT: -450mA |

***Note 1***: *Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

***Note 2:*** *Only supports Micro Speaker when the load resistance $R_L$ is less than 5Ω.*

***Note 3:*** *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017*

***Note 4:*** *Test method: ESDA/JEDEC JS-002-2018*



# ELECTRICAL CHARACTERISTICS

## CHARACTERISTICS

Test condition: $T_A$=25°C, $V_{BAT}$=3.6V, DVDD=1.8V, PVDD=6.25V, $R_L$=8Ω+33μH, f=1kHz (unless otherwise noted)

| Symbol | Description | Test Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | Battery supply voltage | On pin VBAT | 3.0 | | 5.5Note1 | V |
| $V_{DVDD}$ | Digital supply voltage | On pin DVDD | 1.65 | 1.8 | 1.95 | V |
| $I_{VBAT}$ | Battery supply current | Operating mode, Po=0.5W | | 170 | | mA |
| | | Operating mode, I²S signal input digital zero, Noise Gate Off | | 3.2 | | mA |
| | | Operating mode, I²S signal input digital zero, Noise Gate On | | 1.9 | | mA |
| | | Power down mode | | 0.1 | 2 | μA |
| | | Standby mode | | 4.3 | | μA |
| $I_{DVDD}$ | Digital supply current | Operating mode with SKTune Algorithm activated, I²S signal input 0dBFS | | 13 | | mA |
| | | Operating mode with SKTune Algorithm bypassed, I²S signal input 0dBFS | | 3.2 | | mA |
| | | Operating mode with SKTune Algorithm activated, I²S signal input digital zero | | 4.4 | | mA |
| | | Operating mode with SKTune Algorithm bypassed, I²S signal input digital zero | | 2.9 | | mA |
| | | Power down mode | | 0.3 | | μA |
| | | Standby mode | | 4.3 | | μA |
| **Boost** | | | | | | |
| $V_{PVDD}$ | Boost output voltage | | | 6.25Note2 | | V |
| $V_{OVP}$ | Over-voltage threshold | | | $V_{PVDD}$+0.5 | | V |
| | OVP hysteresis voltage | | | 400 | | mV |
| $I_{L\_PEAK}$ | Inductor peak current limit | | | 2Note2 | | A |
| $F_{BST}$ | Operating Frequency | fs = 48kHz | | 2 | | MHz |
| **Class-D** | | | | | | |
| $R_{dson}$ | Drain-Source on-state resistance | High side MOS + Low side MOS | | 280 | | mΩ |
| Po | Speaker Output Power | THD+N=1%, $R_L$=8Ω+33μH, $V_{BAT}$=4.2V, PVDD=6.25V | | 2.1 | | W |



| Symbol | Description | Test Conditions | | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|---|
| | | THD+N=10%, $R_L$=8Ω+33μH, $V_{BAT}$=4.2V, PVDD=6.25V | | | 2.4 | | W |
| | | THD+N=1%, $R_L$=6Ω+33μH, $V_{BAT}$=4.2V, PVDD=6.25V | | | 2.8 | | W |
| | | THD+N=10%, $R_L$=6Ω+33μH, $V_{BAT}$=4.2V, PVDD=6.25V | | | 3.2 | | W |
| | | THD+N=1%, $R_L$=4Ω+33μH, $V_{BAT}$=4.2V, PVDD=6.25V | | | 3 | | W |
| | | THD+N=1%, $R_L$=4Ω+33μH, $V_{BAT}$=5V, Pass-through mode | | | 2.4 | | W |
| | | THD+N=10%, $R_L$=4Ω+33μH, $V_{BAT}$=5V, Pass-through mode | | | 3 | | W |
| $V_{OS}$ | Output offset voltage | $I^2S$ signal input digital zero | | -3 | 0 | 3 | mV |
| $F_{PWM}$ | PWM Switching frequency | Typical Sample Rate: 48kHz | | | 384 | | kHz |
| η | Total efficiency (Class-D) | $V_{BAT}$=4.2V, Po=0.45W, $R_L$=8Ω+33μH | | | 89 | | % |
| | Total efficiency (Smart Boost + Class-D) | $V_{BAT}$=4.2V, Po=1W, $R_L$=8Ω+33μH | | | 86 | | % |
| THD+N | Total harmonic distortion plus noise | $V_{BAT}$=4.2V, Po=1W, $R_L$=8Ω+33μH, f=1kHz,PVDD=6.25V | | | 0.006 | | % |
| $E_N$ | Speaker Mode Output noise | A-weighting | | | 10 | | μV |
| | Receiver Mode Output noise | A-weighting | | | 10 | | μV |
| $FR_{amp}$ | Frequency response flatness[Note3] | SPK(20Hz-20kHz), Po=1W | | | 0.2 | | dB |
| | | SPK(20Hz-40kHz), Po=1W | | | 0.5 | | dB |
| | | RCV(20Hz-20kHz), Po=1W | | | 0.2 | | dB |
| | | RCV(20Hz-40kHz), Po=1W | | | 0.5 | | dB |
| SNR | Signal-to-noise ratio | $V_{BAT}$=4.2V, PVDD=6.25V Po=2.1W, $R_L$=8Ω+33μH, A-weighting | | | 112 | | dB |
| DNR | Dynamic Range | -60dBFS Method, A-weighting | | | 109 | | dB |
| PSRR | Power supply rejection ratio | Receiver Mode, $V_{BAT}$=4.2V, $V_{p\text{-}p\_sin}$=200mV | 217Hz | | 88 | | dB |
| | | | 1kHz | | 78 | | dB |
| **Current Sense** | | | | | | | |
| $I_{SNS\_FS}$ | Current sense full scale | | | | 3.4667 | | A |
| SNR | Signal-to-noise ratio | Po=2W, $R_L$=8Ω+33μH, A-weighting | | | 60 | | dB |



| Symbol | Description | Test Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| THD+N | Total harmonic distortion plus noise | Po=1W, $R_L$=8Ω+33μH | | 0.3 | | % |
| $\Delta I_{SNS}$ | Current sense accuracy | Po=1W, $R_L$=8Ω+33μH | | 2 | | % |
| **Digital Logical Interface** | | | | | | |
| $V_{IL}$ | Logic input low level | BCK, WCK, DATAI Pin | | | 0.3 x $V_{DVDD}$ | V |
| $V_{IH}$ | Logic input high level | | 0.7 x $V_{DVDD}$ | | $V_{DVDD}$ | V |
| $V_{IL}$ | Logic input low level | RSTN, SCL, SDA, AD Pin | | | 0.3 x $V_{DVDD}$ | V |
| $V_{IH}$ | Logic input high level | | 0.7 x $V_{DVDD}$ | | 3.6 | V |
| $V_{OL}$ | Logic output low level | $I_{OUT}$=2mA | | | 0.45 | V |
| $V_{OH}$ | Logic output high level | $I_{OUT}$=-2mA | $V_{DVDD}$ - 0.45 | | $V_{DVDD}$ | V |
| **Protection** | | | | | | |
| $T_{SD}$ | Over temperature protection threshold | | | 150 | | °C |
| $T_{SDR}$ | Over temperature protection recovery threshold | | | 130 | | °C |
| UVP | Under-voltage protection voltage | | | 2.6 | | V |
| | Under-voltage protection hysteresis voltage | | | 100 | | mV |

***Note 1***: *When the voltage of VBAT is higher than 5V, DC-DC converter should be worked in Pass-through mode. At the same time, set SET_GAIN no less than 5.6AV and disable EN_MPD.*

***Note 2***: *Registers are adjustable; Refer to the list of registers.*

***Note 3***: *FS=96kHz when the amplitude response variation is 20Hz - 40kHz.*



## I²C INTERFACE TIMING

| Parameter | | | Fast mode | | | Fast mode Plus | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| No. | Sym | Name | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $f_{SCL}$ | SCL Clock frequency | | | 400 | | | 1000 | KHz |
| 2 | $t_{LOW}$ | SCL Low level Duration | 1.3 | | | 0.5 | | | μs |
| 3 | $t_{HIGH}$ | SCL High level Duration | 0.6 | | | 0.26 | | | μs |
| 4 | $t_{RISE}$ | SCL, SDA rise time | | | 0.3 | | | 0.12 | μs |
| 5 | $t_{FALL}$ | SCL, SDA fall time | | | 0.3 | | | 0.12 | μs |
| 6 | $t_{SU:STA}$ | Setup time SCL to START state | 0.6 | | | 0.26 | | | μs |
| 7 | $t_{HD:STA}$ | (Repeat-start) Start condition hold time | 0.6 | | | 0.26 | | | μs |
| 8 | $t_{SU:STO}$ | Stop condition setup time | 0.6 | | | 0.26 | | | μs |
| 9 | $t_{BUF}$ | the Bus idle time START state to STOP state | 1.3 | | | 0.5 | | | μs |
| 10 | $t_{SU:DAT}$ | SDA setup time | 0.1 | | | 0.05 | | | μs |
| 11 | $t_{HD:DAT}$ | SDA hold time | 10 | | | 10 | | | ns |

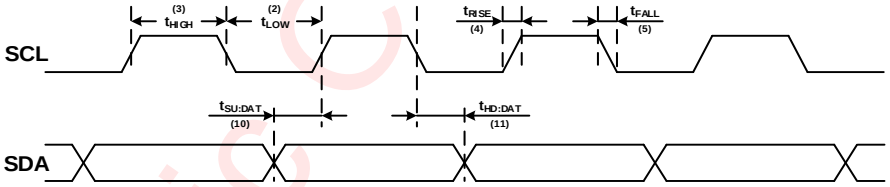



**Figure 5 SCL and SDA timing relationships in the data transmission process**

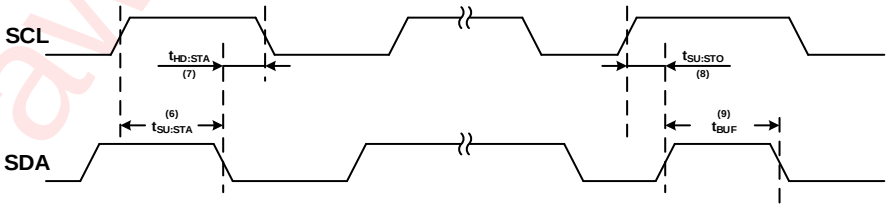



**Figure 6 The timing relationship between START and STOP state**



## DIGITAL AUDIO INTERFACE TIMING

| Parameter Name | | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| $f_s$ | sampling frequency, on pin WCK | 8 | | 96 | kHz |
| $f_{bck}$ | Bit clock frequency, on pin BCK | 16*fs | | 12.288 | MHz |
| $t_{su}$ | WCK, DATAI Setup time to BCK | 10 | | | ns |
| $t_h$ | WCK, DATAI hold time to BCK | 10 | | | ns |
| $t_d$ | DATAO output delay time to BCK | | | 50 | ns |

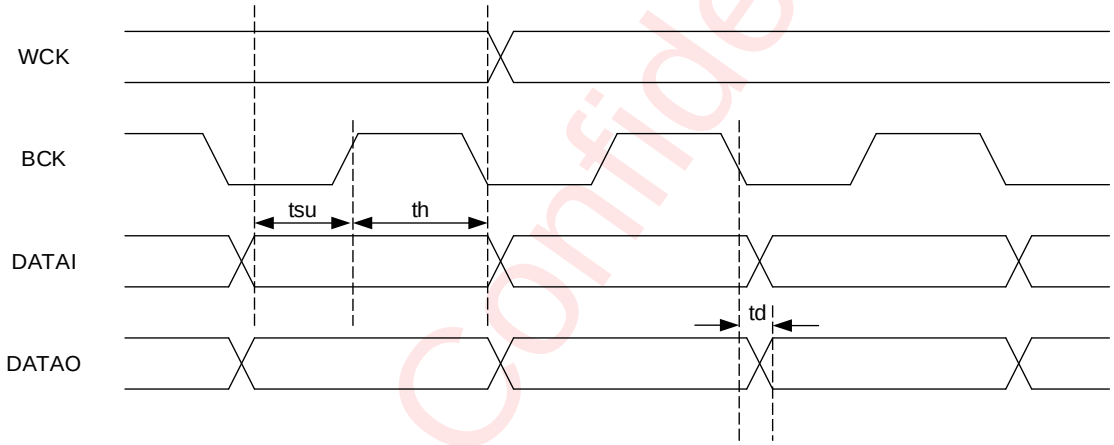


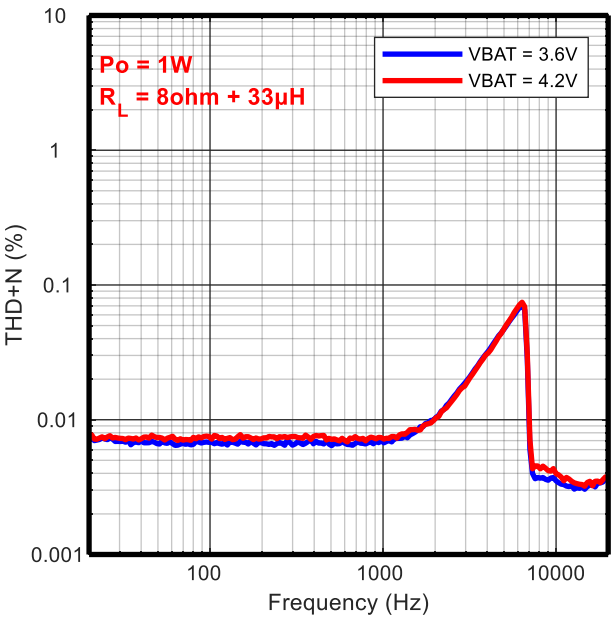

**Figure 7 Digital Audio Interface Timing**



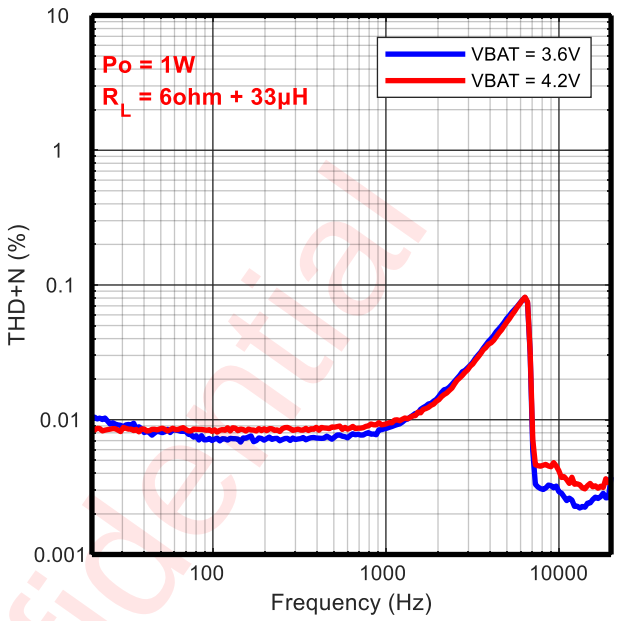
 

## TYPICAL CHARACTERISTIC CURVES

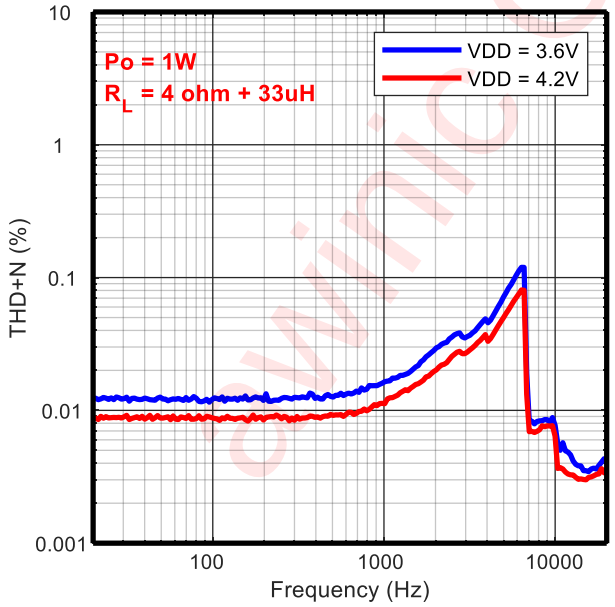
THD+N VS. FREQUENCY



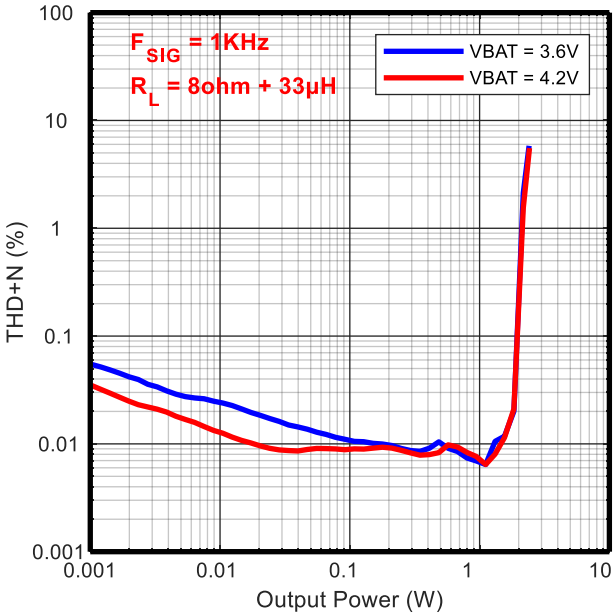

THD+N VS. FREQUENCY




THD+N VS. FREQUENCY



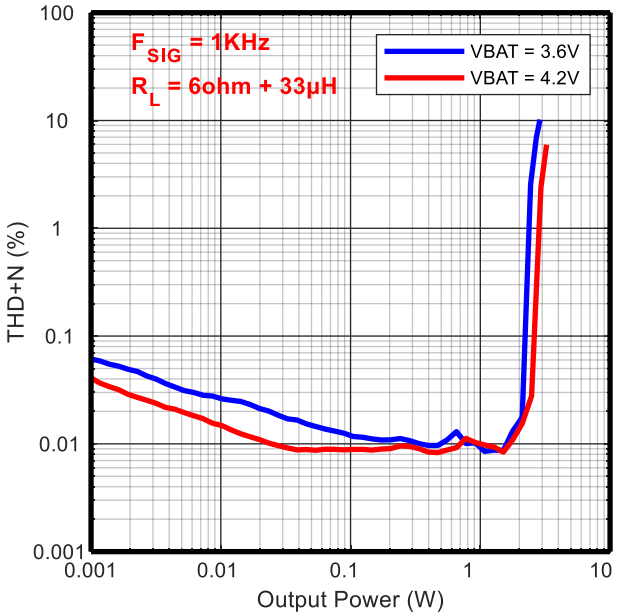

THD+N VS. OUTPUT POWER



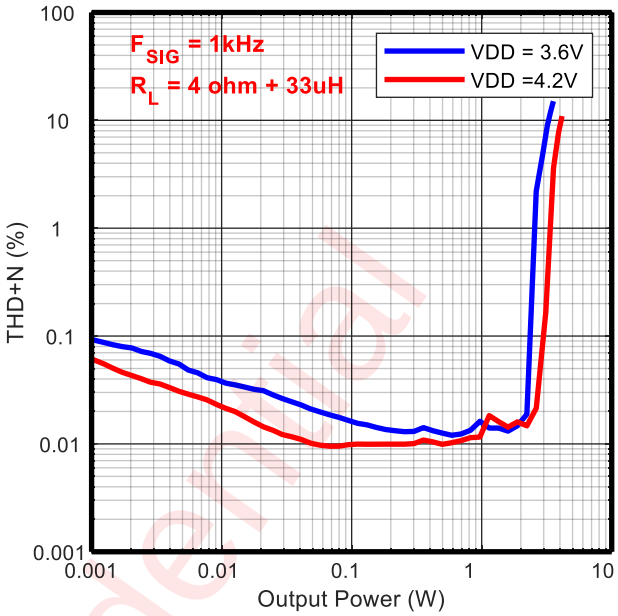


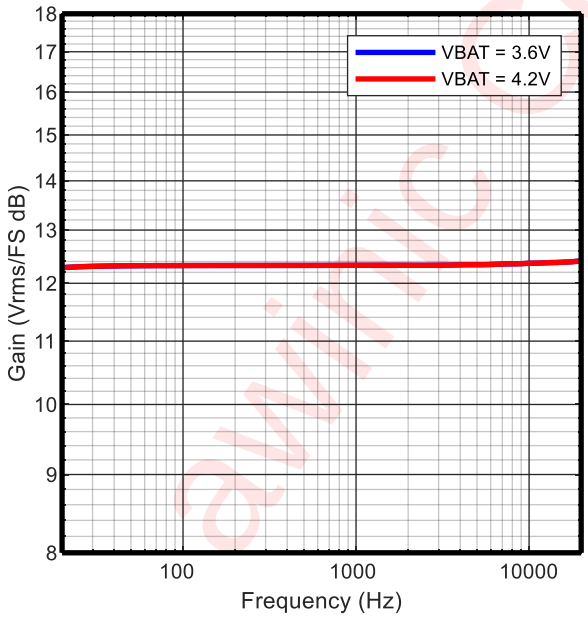
### THD+N VS. OUTPUT POWER



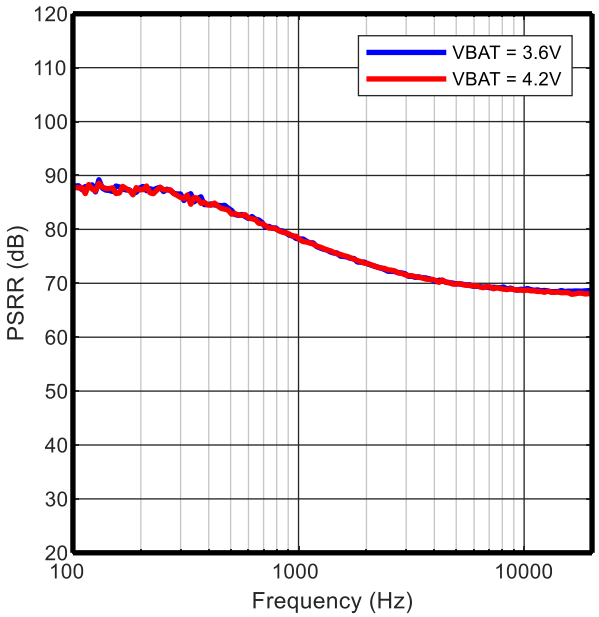

### THD+N VS. OUTPUT POWER




### GAIN VS. FREQUENCY



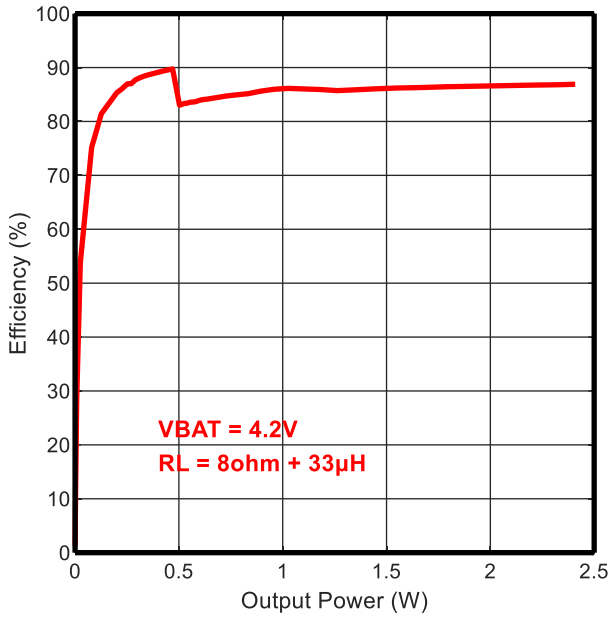

### RECEIVER PSRR VS. FREQUENCY



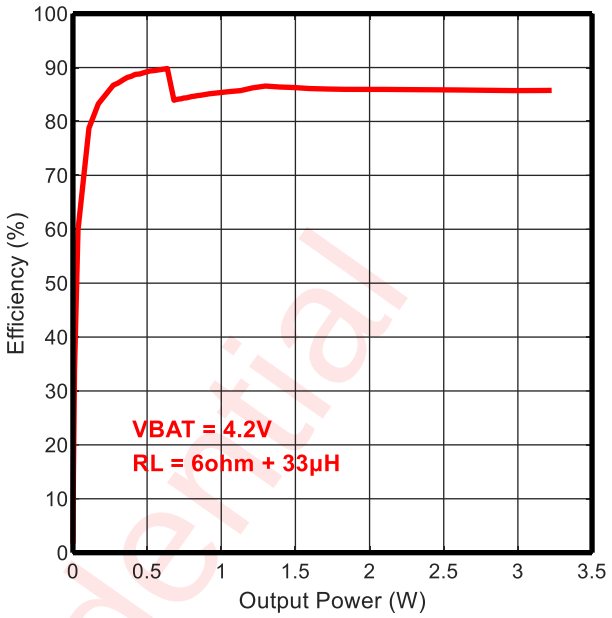


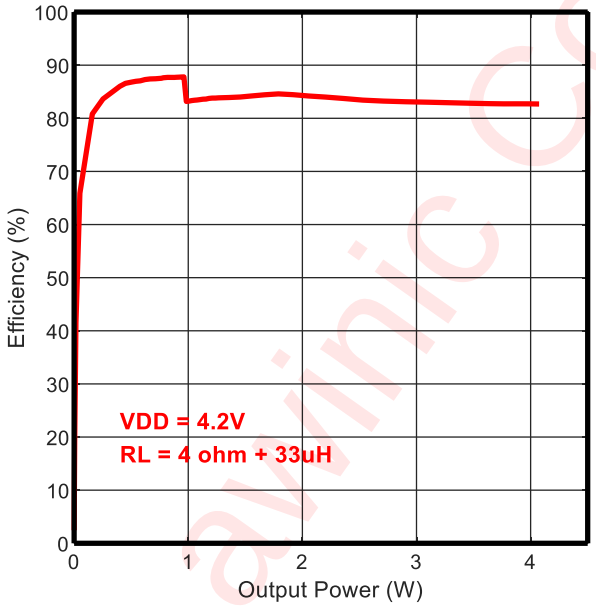
**EFFICIENCY VS. OUTPUT POWER**




**EFFICIENCY VS. OUTPUT POWER**




**EFFICIENCY VS. OUTPUT POWER**





# DETAIL FUNCTIONAL DESCRIPTION

## POWER ON RESET

The device provides a power-on reset feature that is controlled by VBAT and DVDD supply voltage. When the VBAT supply voltage raises from 0V to 2.1V, or DVDD supply voltage raises from 0V to 1.1V. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

## OPERATION MODE

The device supports 4 operation modes.

**Table 1 Operating Mode**

| Mode | Condition | Description |
|---|---|---|
| Power-Down | $V_{BAT}$ < 2.1V<br>$V_{DVDD}$ < 1.1V | Power supply is not ready, chipset is power down. |
| Stand-By | $V_{BAT}$ > 3.0V<br>$V_{DVDD}$ > 1.65V | Power supply is ready, most parts of the device are power down for low power consumption except I²C interface |
| Configuring | PWDN = 0 | Device is biased while boost and class-D output is floating. System configuration carried out in this mode |
| Operating | AMPPD = 0 | Amplifier is fully operating |

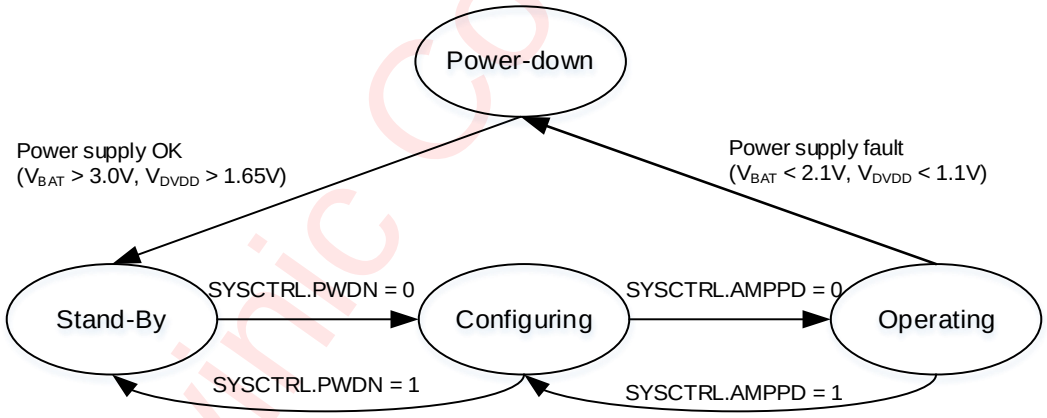



**Figure 8 Device operating modes transition**

### *POWER-DOWN MODE*

The device switches to power-down mode when any of the following events occurred:

- $V_{DVDD}$ < 1.1 V
- $V_{BAT}$ < 2.1 V
- RSTN pin goes LOW

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:



$V_{DVDD}$ > 1.65 V and $V_{BAT}$ > 3.0 V
And RSTN goes HIGH.

### *STAND-BY MODE*

The device switches stand-by mode when the power supply voltages are OK and RSTN pin is HIGH. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

### *CONFIG MODE*

The device switches to OFF mode when:

- SYSCTRL.PWDN = 0
- SYSCTRL.AMPPD = 1

In this mode the internal bias, OSC, PLL will start to work.

### *OPERATING MODE*

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.
This device power up sequence is illustrated in the following figure:

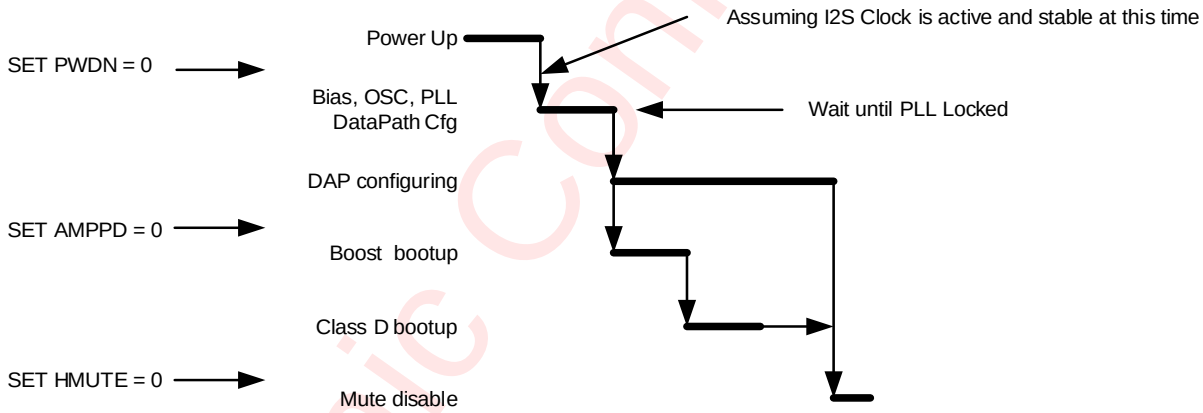



**Figure 9 Power up sequence**

Detail description for each step is listed in the following table.

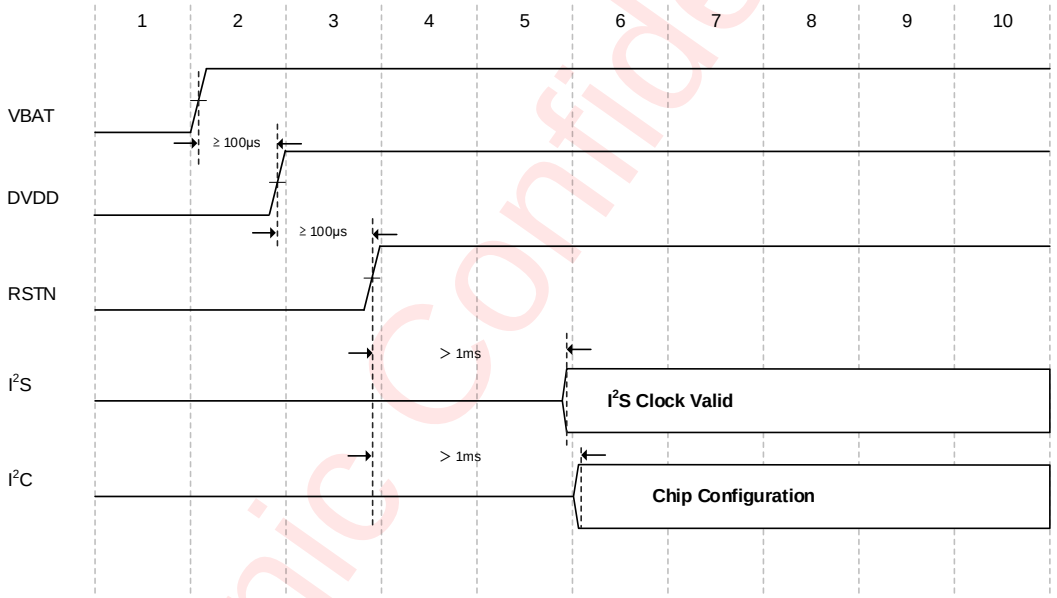


**Table 2 Detail Description of Power up sequence**

| Index | Description | Mode |
|---|---|---|
| **1** | Wait for VBAT, DVDD supply power up | Power-Down |
| **2** | I²S + Data Path Configuration | Stand-By |
| **3.1** | Enable system (SYSCTRL.PWDN = 0) | Configuring |
| **3.2** | Bias, OSC, PLL active | |
| **3.3** | Waiting for PLL to be locked | |
| **4.1** | Enable Boost and amplifier (SYSCTRL.AMPPD =0)<br>Boost and Amplifier boot up | Operating |
| **4.2** | Waiting for SYSST.SWS =1 | |
| **5** | Release Hard-Mute<br>Data Path active | |

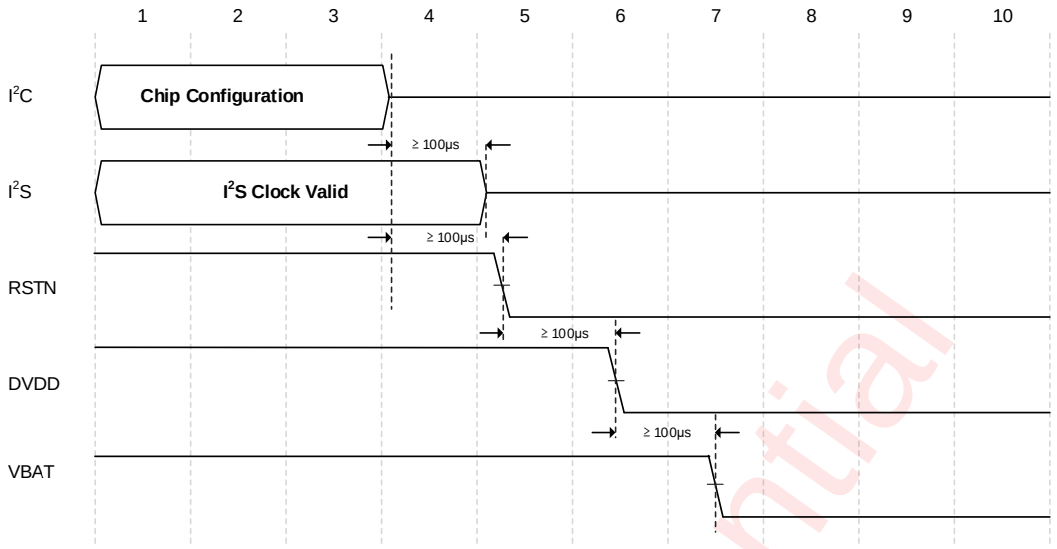
Power up sequence considering I²S, I²C timing shows as below:




Power down sequence considering I²S, I²C timing shows as below:






## SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

## DIGITAL I/O STATUS

Each digital input and IO's state is shown in below table. The input signal pin BCK, WCK and DATAI are set to high impedance by default after power on. If I2STXEN is enabled, DATAO is actively driven when outputting data otherwise it is high impedance by default.

| Digital I/O | Type | Description ( Default state) |
|---|---|---|
| RSTN | Input | Weak pull down |
| SCL | Input | Hi-Z |
| SDA | Inout | Hi-Z |
| INTN | Output | Hi-Z |
| AD | Input | Weak pull down (RSTN = High) |
| BCK | Input | Hi-Z |
| WCK | Input | Hi-Z |
| DATAI | Input | Hi-Z |
| DATAO | Output | Hi-Z |

## DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK
- DATAI
- DATAO



Two-slot I²S and 1/2/4/6/8 slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL1.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL1.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz and 96kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL1.I2SBCK. The frequency of BCK can be calculated according to the following equation:

*BCK frequency* = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

**SampleRate**: Sample rate for this digital audio interface

**SlotLength**: The length of one audio slot in unit of BCK clock

**SlotNumber**: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 1/2/4/6/8-slot supported in TDM mode

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL1.CHSEL.

**Table 3 Supported I²S interface parameters**

| Interface format(MSB first) | Data width | BCK frequency |
|---|---|---|
| Standard I²S | 16b/20b/24b/32b | 32fs/48fs/64fs |
| Left-justified | 16b/20b/24b/32b | 32fs/48fs/64fs |
| Right-justified | 16b/20b/24b/32b | 32fs /48fs/64fs |

The output port DATAO, can be enabled or disabled via bit I2SCTRL1.I2STXEN. The unused slots can be set to Hi-z or normal working, which is controlled by SYSCTRL2.DOHZ.

***STANDARD I²S MODE***

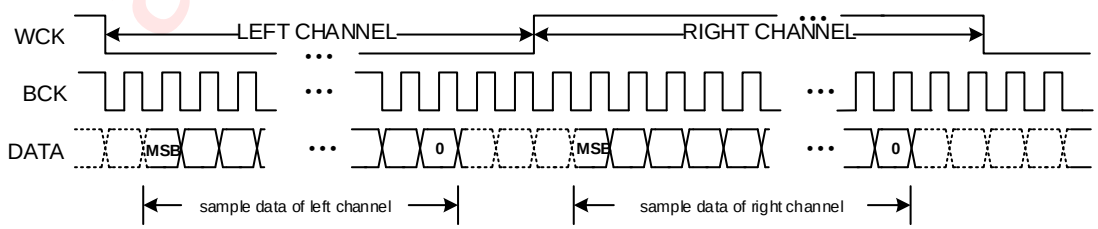



**Figure 10 I²S Timing for Standard I²S Mode**

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock

***LEFT-JUSTIFIED MODE***

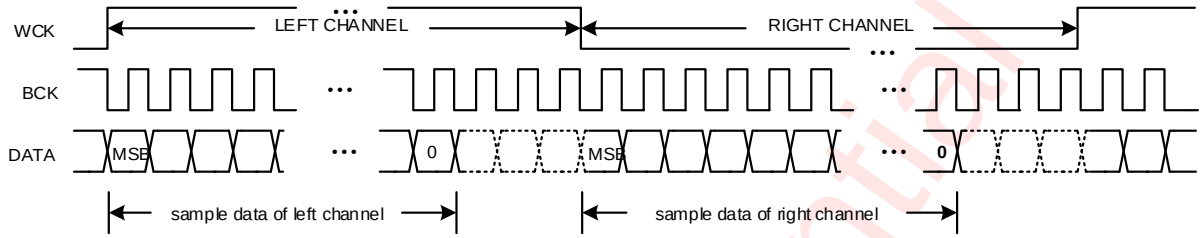



**Figure 11 I²S Timing for Left-Justified Mode**

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock

***RIGHT-JUSTIFIED MODE***

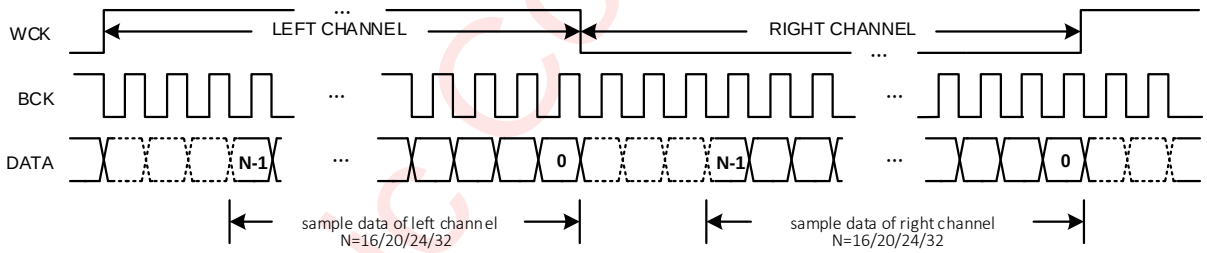



**Figure 12 I²S Timing for Right-Justified Mode**

- When WCK is high indicating the left channel data, and WCK=0 indicating the right channel data
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock

***TDM MODE***

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 1/2/4/6/8-slot is supported in TDM mode, while 2-slot is supported in I²S mode.



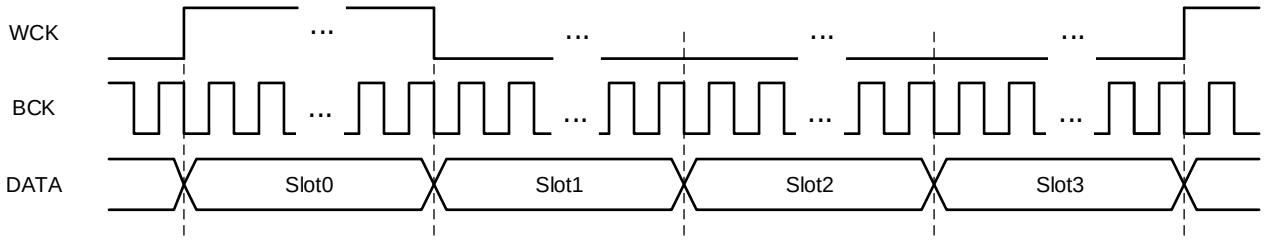



**Figure 13 TDM Timing**

Note: The high level pulse width of WCK signal can be one slot time or one period of BCK.

## DIGITAL AUDIO PROCESSING

This device incorporates one programmable Digital Audio Processor (DAP) block. It provides the algorithm for audio signal processing and speaker protection. The following functions are available in this module.

- HDCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the Digital Audio Processor (DAP) is illustrated in the following figure.

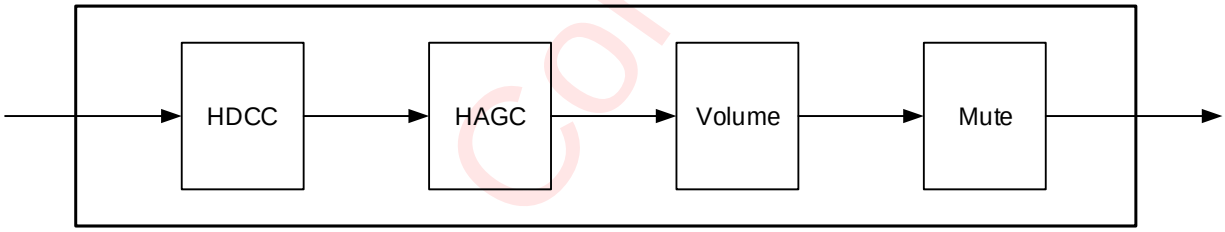



**Figure 14 Block Diagram of DAP**

***HDCC***

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

***HAGC***

System output power tends to be more than rated power of speaker in the actual audio application, such as the maximum undistorted power is about 2.1W in the 6.25V power supply for 8Ω speaker. However, many speakers' rated power is about 1W, the overload signal can cause damage to the speaker if there is no output power control. The audio power amplifier with HAGC can protect the speaker effectively. When the output power does not exceed the setting threshold, the HAGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the HAGC module will reduce the internal gain of amplifier and restrict the output power under the setting threshold.



### *VOLUME CONTROL*

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0dB to -96dB with 0.094dB/step.

### *MUTE*

This module performs mute control for the audio stream.

## SKTUNE ALOGRITHM

This device integrates SKTune algorithm that maximizes the speaker performance while maintaining safe speaker conditions. The following functions are available in this module.

- Bass Booster
- Parametric Audio Path Equalizer (EQ)
- Automatic Gain Control (AGC)
- Multi-Band Dynamic Range Compressor (MBDRC)
- Anti-clip Voltage Limiter
- Speaker Protection

The signal processing flow in the SKTune algorithm is illustrated in the following figure:

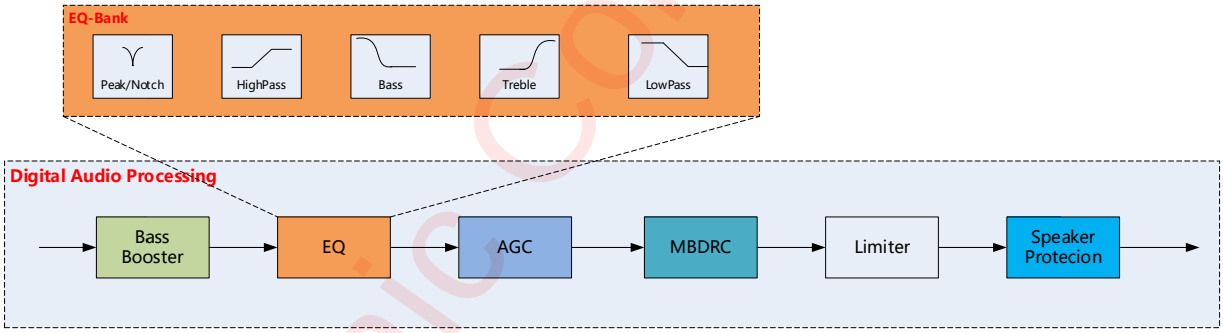



**Figure 15 Block Diagram of SKTune algorithm**

### *BASS BOOSTER*

Small loudspeakers have poor performance in display low frequency audio signal, which can't meet people's demand for high quality sound. BASS BOOSTER uses psychoacoustic technology to highly elevate the low frequency performance in small loudspeaker.

### *PARAMETRIC AUDIO PATH EQUALIZER*

Ten Parametric Audio Path Equalizers (EQ) are available and each of the equalizer can be fully programmable. It's possible to be implemented as any type of filter (high-pass, low-pass, peak, notch, bass, treble etc.) with different design methodologies to achieve the required frequency response.



### *AUTOMATIC GAIN CONTROL*

Automatic Gain Control (AGC) adjust the signal to an appropriate range by applying different gain to achieve the best output effect of the speaker. As the input signal amplitude changes, gain changes automatically. It attenuates big signals and amplifies small signals.

### *MULTI-BAND DYNAMIC RANGE CONTROL*

A highly configurable and scalable MBDRC is available to improve audio performance. A block diagram of the MBDRC is illustrated in the following figure:

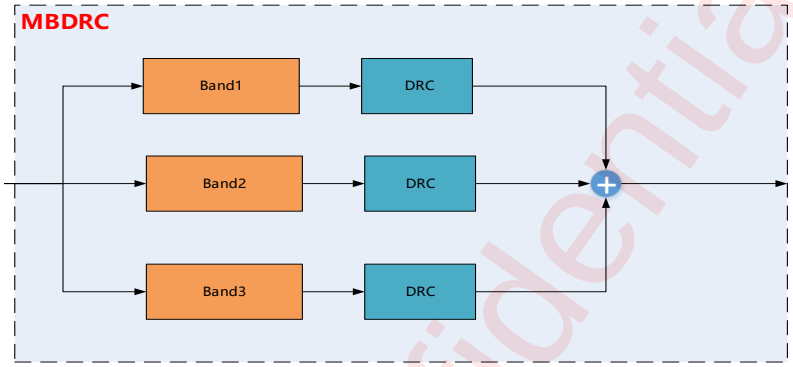



**Figure 16 Simplified MBDRC block diagram**

Three sub-band DRCs are supported. The audio input can be processed with individually configurable band-limited DRCs.

### *ANTI-CLIP VOLTAGE LIMITER*

The anti-clip voltage limiter is used to protect the output signal from exceeding the amplifier clip level. When signal is over the amplifier clip level it will be attenuated automatically and limited below the threshold without clipping.

### *SPEAKER PROTECTION*

This device has integrated three protection schemes for the speaker

- **Membrane excursion control:** avoiding speaker membrane over-excursion
- **Programmable Power Control**: avoiding speaker voice coil over-power
- **Coil temperature control**: avoiding speaker voice coil over-temperature

**Membrane excursion control**

The speaker membrane excursion is proportional to the amplitude of input signal. This device controls the membrane excursion by control the signal amplitude. It predicted the speaker membrane excursion according to the input signal at first. Then it'll attenuate the amplitude of the input signal automatically once the predicted excursion over the threshold.

**Programmable Power Control**

The power controller limits the maximum output power in amplifier mode when necessary. The power of output signal will be attenuated and limited below the programmable threshold in given attack time when the amplitude



of input signal is above the threshold. While the attenuation will be released in given release time when the amplitude of input signal is below the threshold.

**Coil temperature control**

Speaker voice coil temperature is proportional to its impedance in general. This device continuously monitors the impedance of speaker voice coil with integrated ADCs, and the coil temperature could be calculated according to its impedance. When the coil temperature is near the threshold, it controls the amplitude of signal sending to speaker.

## DC-DC CONVERTER

This device using smart boost converter generates the amplifier supply rail, working in 2MHz. The DC-DC converter can work in different mode via BSTCTRL2.BST_MODE:

- **Pass-through mode**: the voltage of VBAT is transparently passed to output of converter PVDD
- **Force boost mode**: the output voltage is boosted to the programmed output voltage
- **Smart boost 1 mode**: the output voltage can be switch between VBAT and programmed output voltage according to the amplifier output's signal swing requirements
- **Smart boost 2 mode**: the output voltage can be dynamically adjusted according to the amplifier output's signal swing requirements in order to maximize efficiency of smart boost 2

### *PASS-THROUGH MODE*

The internal boost circuit is not working; the voltage of VBAT is passed to PVDD directly.

### *FORCE BOOST MODE*

The boost circuit is always working and converts the voltage of VBAT to the programmed output voltage. The output voltage is configured via BSTCTRL2.VOUT_VREFSET.

### *SMART BOOST 1 MODE*

Smart boost 1 mode can dynamically turn off the boost according to the amplifier output's signal swing requirements in order to maximize efficiency.

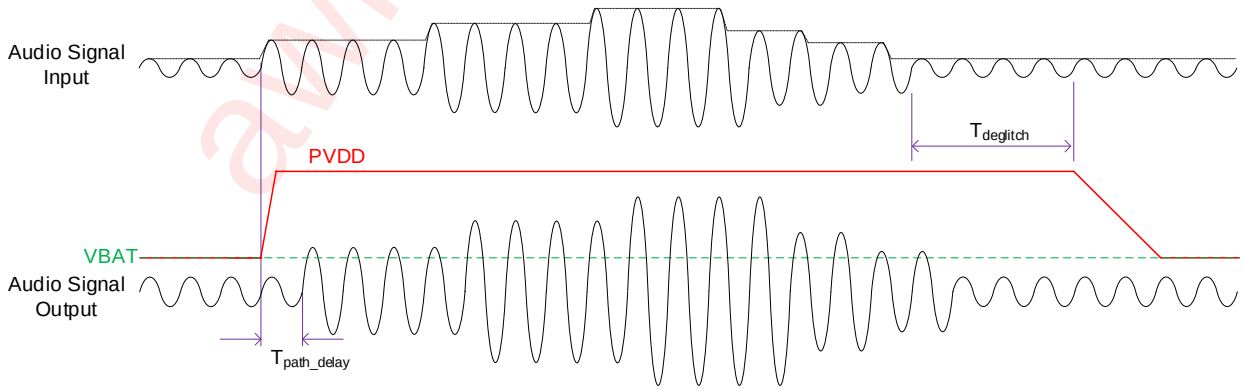



**Figure 17 Boost Circuit Behavior in Smart Boost 1 Mode**



### *SMART BOOST 2 MODE*

The boost circuit works dynamically according to the output audio level. When the level of output audio signal is below the setting threshold, the boost circuit will not be activated. Till the level of output audio signal is above the threshold, the boost circuit starts to work before the audio stream arriving at amplifier power stage. The output voltage PVDD is dynamically adjusted to meet the amplifier output's signal swing requirements.

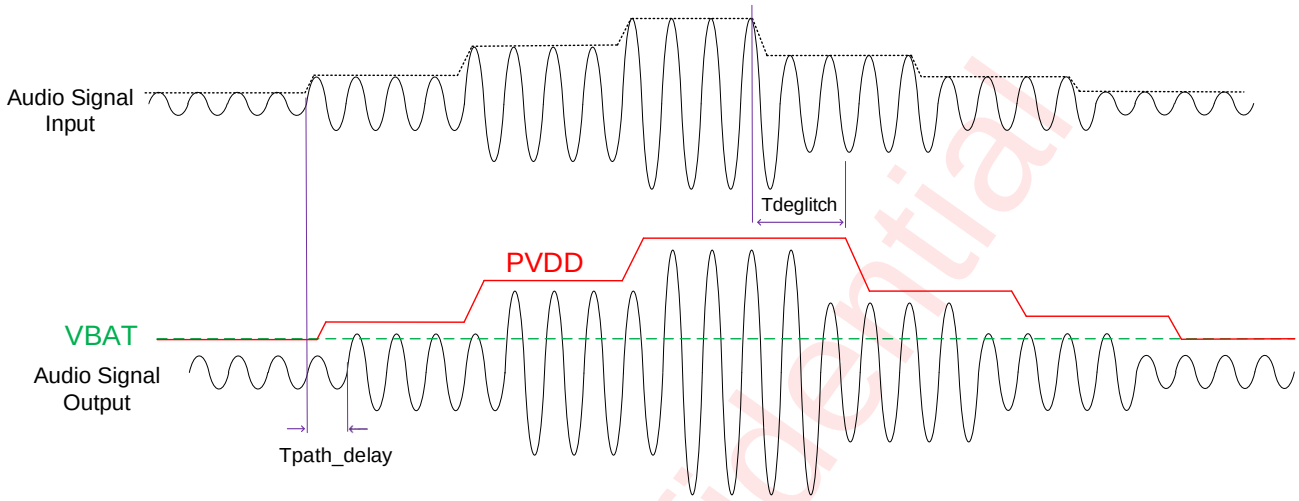



**Figure 18 Boost Circuit Behavior in Smart Boost 2 Mode**

**NOTE**: When the voltage of VBAT is higher than 5V, DC-DC converter should be worked in Pass-through mode.



## PROTECTION MECHANISMS

### Over Voltage Protection (OVP)

The boost circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the boost circuits will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

### Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again.

### Over Current (short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to PVDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

### Under Voltage Detection (UVL)

The interrupt bit SYSINT.UVLI will be set to 1 when VBAT under voltage occurs, and SYSINT.UVLDI will be set to 1 when DVDD under voltage occurs. Both interrupt bits will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI and SYSINT.UVLDI bit can be used to check whether an unexpected under-voltage event has taken place.

## BATTERY VOLTAGE MONITORING

The device monitors the voltage on the VBAT pin, which is most commonly the battery for the system. The battery voltage level is available via bits VBAT_DET in the Battery Supply Voltage register VBAT. Status bits VBAT_DET can be used to calculate the battery voltage. The battery voltage level $V_{BAT}$ is:

$$V_{BAT} = \frac{VBAT\_DET}{2^{10} - 1} \times 6.025V$$

For example, if VBAT_DET = 1001100011, the battery voltage level $V_{BAT}$ is equal to 3.6V.

## PVDD VOLTAGE MONITORING

The device monitors the voltage on the PVDD pin, which is most commonly the PVDD voltage level for the system. The PVDD pin voltage level is available via bits PVDD_DET in the Power Supply Voltage monitor register PVDD. Status bits PVDD_DET can be used to calculate the PVDD voltage. The PVDD voltage level $V_{PVDD}$ is:

$$V_{PVDD} = \frac{PVDD\_DET}{2^{10} - 1} \times 7.25V$$

For example, if PVDD_DET = 1001100011, the PVDD voltage level $V_{PVDD}$ is equal to 4.3V.

## DIE TEMPERATURE MONITORING

The device monitors the die temperature and the result is available via bits TEMP_DET in the Temperature register TEMP. The TEMP_DET is a two's complement value. For example, if TEMP_DET = 00011001, the die



temperature is 25℃.

## CURRENT SENSING

The device provides speaker current sense for real time monitoring of loudspeaker behavior. Current sensing is not disturbed by capacitance (<1nF) on the output lines or on the long speaker tracks. The current sensing transfer function $I_{SNS}$ is:

$$I_{SNS} = \frac{D_{OUT}}{2^{15}-1} \times 3.4667A$$

$D_{OUT}$: the current sense I²S output stream.

## AMPLIFIER TRANSFER FUNCTION

The transfer function from the input to the amplifier PWM output (when no gain and attenuation is applied in digital signal domain) is:

$$V_o = AMP\_NORM\_V \times D_{in}$$

$D_{in}$: the level of input signal with a range from -1 to +1
AMP_NORM_V: the equivalent amplifier output voltage when $D_{in}$ is 1. In receiver mode the AMP_NORM_V is 4.5V, in speaker mode it's 6.75V.

## RECEIVER MODE

The device built-in Receiver mode is easy to realize the Speaker and Receiver combo applications, it saves the system cost and board space. If the receiver magnification is one times, the noise floor will be 10μV. Speaker and Receiver combo applications can be realized without changing any hardware.
When the device is set to receiver mode, the power supply of Class D driver stage is from VBAT directly without boost.

## I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 1MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

### *DEVICE ADDRESS*

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34 (7-bit) through 0x37 (7-bit).

**Table 4 Address Selection**

| AD | Address(7-bit) |
|---|---|
| GND | 0x34 |
| DVDD | 0x35 |
| SCL | 0x36 |
| SDA | 0x37 |



### *DATA VALIDATION*

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

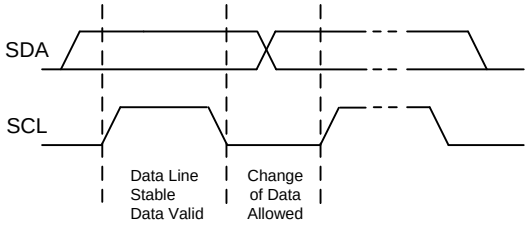



**Figure 19 Data Validation Diagram**

### *I²C START/STOP*

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

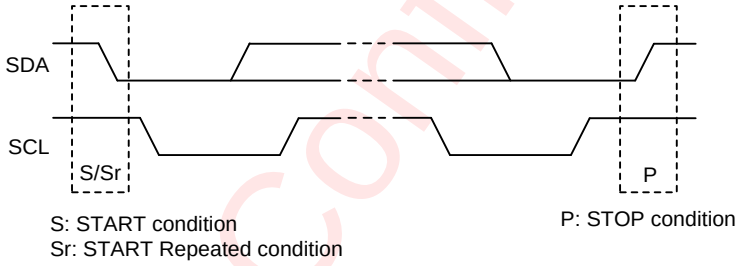



**Figure 20 I²C Start/Stop Condition Timing**

### *ACK (ACKNOWLEDGEMENT)*

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.



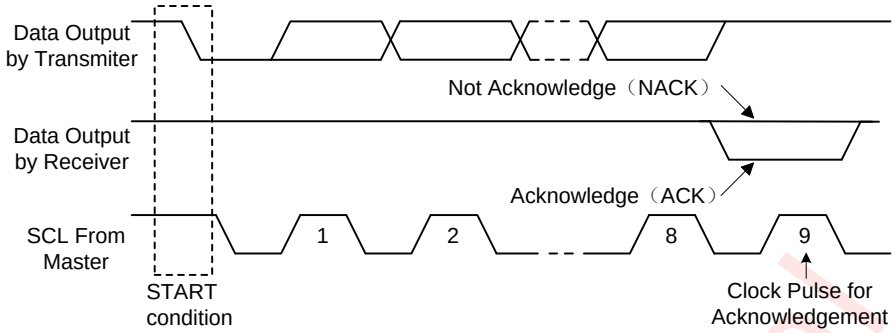



**Figure 21 I²C ACK Timing**

***WRITE CYCLE***

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends high data byte of 16-bit data to be written to the addressed register.

g) Slave sends acknowledge signal.

h) Master sends low data byte of 16-bit data to be written to the addressed register.

i) Slave sends acknowledge signal.

j) If master will send further 16-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g).

k) Master generates STOP condition to indicate write cycle end.



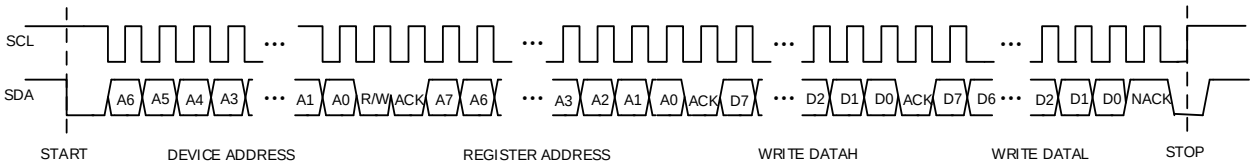



**Figure 22 I²C Write Byte Cycle**

***READ CYCLE***

In a read cycle, the following steps should be followed:

a) Master device generates START condition.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master generates STOP condition followed with START condition or REPEAT START condition.

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.



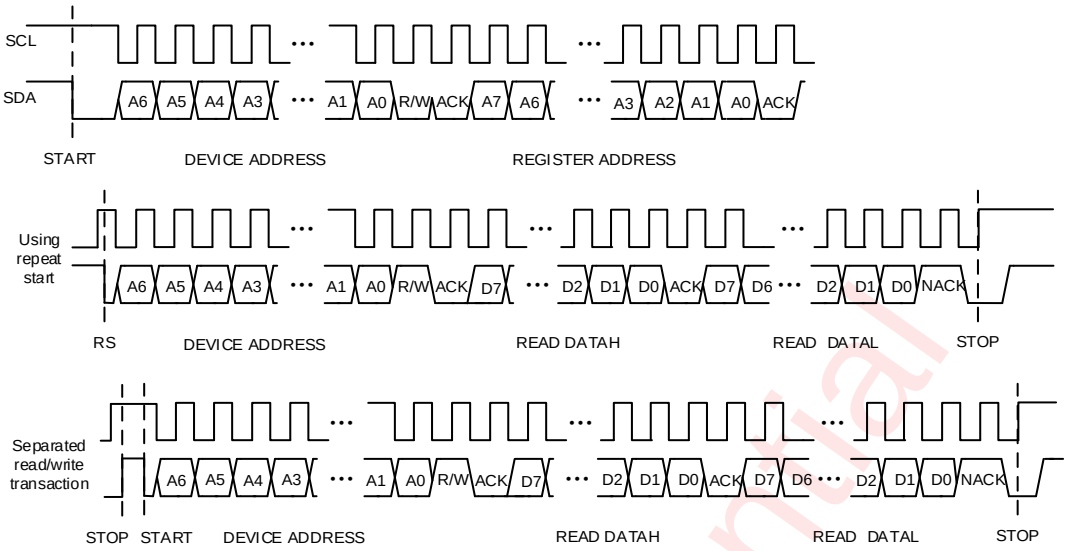



**Figure 23 I²C Read Byte Cycle**



# REGISTER MAP

## REGISTER DESCRIPTION

### *REGISTER LIST*

| ADDR | NAME | R/W | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | ID | *RO* | IDCODE | | | | | | | | | | | | | | | |
| 0x01 | SYSST | *RO* | | UVLS | ADPS | | BSTOCS | OVPS | BSTS | SWS | | WDS | NOCLKS | CLKS | OCDS | UVL_DVDDS | OTHS | PLLS |
| 0x02 | SYSINT | *RC* | | UVLI | ADPI | | BSTOCI | OVPI | BSTI | SWI | | WDI | NOCLKI | CLKI | OCDI | UVL_DVDDI | OTHI | PLLI |
| 0x03 | SYSINTM | *RW* | | UVLM | ADPM | | BSTOCM | OVPM | BSTM | SWM | | WDM | NOCLKM | CLKM | OCDM | UVL_DVDDM | OTHM | PLLM |
| 0x04 | SYSCTRL | *RW* | | SET_GAIN | | | RMSE | HAGCE | HDCCE | HMUTE | | I2SEN | WSINV | BCKINV | IPLL | DSPBY | AMPPD | PWDN |
| 0x05 | SYSCTRL2 | *RW* | EN_MPD | | | | INTMODE | INTN | VOL | | | | | | | | | |
| 0x06 | I2SCTRL1 | *RW* | | CFSEL | | | CHSEL | | I2SMD | | I2SFS | | I2SBCK | | I2SSR | | | |
| 0x07 | I2SCTRL2 | *RW* | FSYNC_TYPE | SLOT_NUM | | | I2S_TX_SLOTVLD | | | | I2S_RXR_SLOTVLD | | | | I2S_RXL_SLOTVLD | | | |
| 0x08 | I2SCTRL3 | *RW* | IV2CH | I2SDOSEL | DOHZ | I2SCHS | DRVSTREN | I2SRXEN | I2STXEN | | ULS_MODE | ULS_EN | LPBK | | | | | |
| 0x09 | DACCFG1 | *RW* | RVTH | | | | | | | | AVTH | | | | | | | |
| 0x0A | DACCFG2 | *RW* | ATTH | | | | | | | | | | | | | | | |
| 0x0B | DACCFG3 | *RW* | RTTH | | | | | | | | | | | | | | | |
| 0x0C | DACCFG4 | *RW* | | | | | | | | | HOLDTH | | | | | | | |
| 0x16 | PWMCTRL3 | *RW* | | | NOISE_GATE_EN | | | | | | | | | | | | | |
| 0x21 | VBAT | *RO* | | | | | VBAT_DET | | | | | | | | | | | |
| 0x22 | TEMP | *RO* | | | | | TEMP_DET | | | | | | | | | | | |
| 0x23 | PVDD | *RO* | | | | | PVDD_DET | | | | | | | | | | | |
| 0x60 | BSTCTRL1 | *RW* | | | BST_RTH | | | | | | | BST_ATH | | | | | | |
| 0x61 | BSTCTRL2 | *RW* | BST_IPEAK | | | | BST_TDEG | | | | | BST_MODE | | BST_VOUT_SET | | | | |



REGISTER DEFAULT

| ADDR | NAME | R/W | Reset Value |
|---|---|---|---|
| 0x00 | ID | *RO* | 0x2066 |
| 0x01 | SYSST | *RO* | 0x0000 |
| 0x02 | SYSINT | *RC* | 0x0000 |
| 0x03 | SYSINTM | *RW* | 0xFFFF |
| 0x04 | SYSCTRL | *RW* | 0xD307 |
| 0x05 | SYSCTRL2 | *RW* | 0x8000 |
| 0x06 | I2SCTRL1 | *RW* | 0x04E8 |
| 0x07 | I2SCTRL2 | *RW* | 0x0010 |
| 0x08 | I2SCTRL3 | *RW* | 0x2C08 |
| 0x09 | DACCFG1 | *RW* | 0x3940 |
| 0x0A | DACCFG2 | *RW* | 0x0030 |
| 0x0B | DACCFG3 | *RW* | 0x01ED |
| 0x0C | DACCFG4 | *RW* | 0x1C64 |
| 0x15 | PWMCTRL2 | *RW* | 0x02BA |
| 0x21 | VBAT | *RO* | 0x02EB |
| 0x22 | TEMP | *RO* | 0x0019 |
| 0x23 | PVDD | *RO* | 0x02A0 |
| 0x60 | BSTCTRL1 | *RW* | 0x0402 |
| 0x61 | BSTCTRL2 | *RW* | 0x5B6C |



## DETAILED REGISTER DESCRIPTION

| ID: (Address 00h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:0 | IDCODE | RO | Chip ID will be returned after read<br>All configuration registers will be reset to default value after 0x55aa is written | 0x2066 |

| SYSST: (Address 01h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15 | Reserved | RO | Not used | 0x0 |
| 14 | UVLS | RO | VBAT under voltage indicator<br>0: Normal<br>1: UVLO | 0x0 |
| 13 | ADPS | RO | Boost Adaptive status<br>0: Pass Through<br>1: Boost | 0x0 |
| 12 | Reserved | RO | Not used | 0x0 |
| 11 | BSTOCS | RO | Boost over current indicator<br>0: Normal<br>1: Over Current | 0x0 |
| 10 | OVPS | RO | Boost OVP status indicator<br>0: Normal<br>1: OVP | 0x0 |
| 9 | BSTS | RO | Boost start up finished indicator<br>0: Not finished<br>1: Finished | 0x0 |
| 8 | SWS | RO | Amplifier switching status indicator<br>0: Not switching<br>1: Switching | 0x0 |
| 7 | Reserved | RO | Not used | 0x0 |
| 6 | WDS | RO | DSP watch-dog status<br>0: Normal<br>1: Abnormal | 0x0 |
| 5 | NOCLKS | RO | The reference clock of PLL status indicator<br>0: Clock Ok<br>1: No Clock | 0x0 |
| 4 | CLKS | RO | Internal clocks status flag<br>0: At least one clocks are unstable<br>1: Stable | 0x0 |
| 3 | OCDS | RO | Over current status in amplifier<br>0: Normal<br>1: OC | 0x0 |
| 2 | UVL_DVDDS | RO | DVDD UVLO status indicator<br>0: Normal<br>1: DVDD_UVLO | 0x0 |
| 1 | OTHS | RO | OT indicator, Die Temperature is higher than 150 degrees or not<br>0: Normal<br>1: OT | 0x0 |



| | | | | |
|---|---|---|---|---|
| 0 | PLLS | RO | PLL locked status indicator<br>0: Unlocked<br>1: Locked | 0x0 |

SYSINT: (Address 02h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | RC | Not used | 0x0 |
| 14 | UVLI | RC | Interrupt indicator for VBAT Power On and UVLS | 0x0 |
| 13 | ADPI | RC | Interrupt indicator for ADPS | 0x0 |
| 12 | Reserved | RC | Not used | 0x0 |
| 11 | BSTOCI | RC | Interrupt indicator for BSTOCS | 0x0 |
| 10 | OVPI | RC | Interrupt indicator for OVPS | 0x0 |
| 9 | BSTI | RC | Interrupt indicator for BSTS | 0x0 |
| 8 | SWI | RC | Interrupt indicator for SWS | 0x0 |
| 7 | Reserved | RC | Not used | 0x0 |
| 6 | WDI | RC | Interrupt indicator for WDS | 0x0 |
| 5 | NOCLKI | RC | Interrupt indicator for NOCLKS | 0x0 |
| 4 | CLKI | RC | Interrupt indicator for CLKS | 0x0 |
| 3 | OCDI | RC | Interrupt indicator for OCDS | 0x0 |
| 2 | UVLDI | RC | Interrupt indicator for UVLDS | 0x0 |
| 1 | OTHI | RC | Interrupt indicator for OTHS | 0x0 |
| 0 | PLLI | RC | Interrupt indicator for PLLS | 0x0 |

Note: It will be set to '1' once corresponding status bit changed, and all the interrupt bits will be cleared after reading 0x02 via IIC bus.

SYSINTM: (Address 03h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | RW | Not used | 0x1 |
| 14 | UVLM | RW | Interrupt mask for UVLI | 0x1 |
| 13 | ADPM | RW | Interrupt mask for ADPI | 0x1 |
| 12 | Reserved | RW | Not used | 0x1 |
| 11 | BSTOCM | RW | Interrupt mask for BSTOCI | 0x1 |
| 10 | OVPM | RW | Interrupt mask for OVPI | 0x1 |
| 9 | BSTM | RW | Interrupt mask for BSTI | 0x1 |
| 8 | SWM | RW | Interrupt indicator for SWI | 0x1 |
| 7 | Reserved | RW | Not used | 0x1 |
| 6 | WDM | RW | Interrupt mask for WDS | 0x1 |
| 5 | NOCLKM | RW | Interrupt mask for NOCLKI | 0x1 |
| 4 | CLKM | RW | Interrupt mask for CLKI | 0x1 |
| 3 | OCDM | RW | Interrupt mask for OCDI | 0x1 |



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|---|---|---|---|---|
| 2 | UVLDM | RW | Interrupt mask for UVLDI | 0x1 |
| 1 | OTHM | RW | Interrupt mask for OTHI | 0x1 |
| 0 | PLLM | RW | Interrupt mask for PLLI | 0x1 |
| Note: All the mask bits are high-active. The interrupt will be masked when its corresponding mask bit is set to "1", then this interrupt will not be sent to INTN pin. | | | | |

SYSCTRL: (Address 04h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | RW | Not used | 0x1 |
| 14:12 | SET_GAIN | RW | Amplifier gain setting<br>001: 4.2 AV<br>010: 4.5 AV<br>011: 5.6 AV<br>100: 6.3 AV<br>101: 6.75 AV<br>Others: Reserved | 0x5 |
| 11 | RMSE | RW | Hardware HAGC mode selection<br>0: Peak AGC<br>1: RMS AGC | 0x0 |
| 10 | HAGCE | RW | Disable/Enable Hardware AGC<br>0: Disable<br>1: Enable | 0x0 |
| 9 | HDCCE | RW | Disable/Enable Hardware DC Canceling module<br>0: Disable<br>1: Enable | 0x1 |
| 8 | HMUTE | RW | Disable/Enable Hardware mute module<br>0: Disable<br>1: Enable | 0x1 |
| 7 | Reserved | RW | Not used | 0x0 |
| 6 | I2SEN | RW | Disable/Enable whole $I^2S$ interface module<br>0: Disable<br>1: Enable | 0x0 |
| 5 | WSINV | RW | $I^2S$ Left/Right channel switch control<br>0: Not switch<br>1: Switch | 0x0 |
| 4 | BCKINV | RW | $I^2S$ bit clock invert control<br>0: Not invert<br>1: Inverted | 0x0 |
| 3 | IPLL | RW | PLL reference clock selection<br>0: BCK<br>1: WCK | 0x0 |
| 2 | DSPBY | RW | DSP bypass control bit<br>0: Working<br>1: Bypass | 0x1 |
| 1 | AMPPD | RW | Amplifier power down control bit, Power Down until system configuration is finished<br>0: Working<br>1: Power Down | 0x1 |
| 0 | PWDN | RW | System power down control bit<br>0: Working<br>1: Power Down | 0x1 |



| SYSCTRL2: (Address 05h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15 | EN_MPD | RW | Disable/Enable MPD multi stage power mode, Gain will be automatically adjusted only when EN_MPD is high.<br>0: Disable<br>1: Enable | 0x1 |
| 14:12 | Reserved | RW | Not used | 0x0 |
| 11 | INTMODE | RW | Interrupt pad INTN output mode selection<br>0: Open-drain<br>1: Push-Pull | 0x0 |
| 10 | INTN | RW | Interrupt pad INTN pin-source selection<br>0: SYSINT<br>1: SYSST | 0x0 |
| 9:0 | VOL | RW | Volume control, from 0 to-96dB, in unit of-6.02/64dB | 0x0 |

| I2SCTRL1: (Address 06h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15 | Reserved | RW | Not used | 0x0 |
| 14:12 | CFSEL | RW | I2S legacy path output data selection<br>000: HAGC<br>100: IV<br>101: IVBT<br>Others: Reserved | 0x0 |
| 11:10 | CHSEL | RW | Left/right channel selection for $I^2S$ input<br>00: Reserved<br>01: Left<br>10: Right<br>11: Mono | 0x1 |
| 9:8 | I2SMD | RW | $I^2S$ data format mode selection<br>00: Philip Standard<br>01: MSB justified<br>10: LSB justified<br>11: Reserved | 0x0 |
| 7:6 | I2SFS | RW | $I^2S$ data resolution selection<br>00: 16 bits<br>01: 20 bits<br>10: 24 bits<br>11: 32 bits | 0x3 |
| 5:4 | I2SBCK | RW | $I^2S$ BCK mode<br>00: 32*fs<br>01: 48*fs<br>10: 64*fs<br>11: Reserved | 0x2 |
| 3:0 | I2SSR | RW | $I^2S$ interface sample rate configuration<br>0000: 8kHz<br>0001: 11.025kHz<br>0010: 12kHz<br>0011: 16kHz<br>0100: 22.05kHz<br>0101: 24kHz | 0x8 |



| | | | | |
|---|---|---|---|---|
| | | | 0110: 32kHz<br>0111: 44.1kHz<br>1000: 48kHz<br>1001: 96kHz<br>Others: Reserved | |

I2SCTRL2: (Address 07h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15 | FSYNC_TYPE | RW | Audio Frame synchronization signal (WCK) pulse width configuration<br>0: One-slot<br>1: One-bck | 0x0 |
| 14:12 | SLOT_NUM | RW | $I^2S$ interface mode control (support max to 8 slots)<br>000: $I^2S$ mode<br>001: TDM1s<br>010: TDM2s<br>011: TDM4s<br>100: TDM6s<br>101: TDM8s<br>Others: Reserved | 0x0 |
| 11:8 | I2S_TX_SLOTVLD | RW | TX slot selection, data will be sent to one of the 8 slots<br>0000: Slot 0<br>0001: Slot 1<br>0010: Slot 2<br>0011: Slot 3<br>0100: Slot 4<br>0101: Slot 5<br>0110: Slot 6<br>0111: Slot 7<br>Others: Reserved | 0x0 |
| 7:4 | I2S_RXR_SLOTVLD | RW | RX right channel slot selection<br>0000: Slot 0<br>0001: Slot 1<br>0010: Slot 2<br>0011: Slot 3<br>0100: Slot 4<br>0101: Slot 5<br>0110: Slot 6<br>0111: Slot 7<br>Others: Reserved | 0x1 |
| 3:0 | I2S_RXL_SLOTVLD | RW | RX left channel slot selection<br>0000: Slot 0<br>0001: Slot 1<br>0010: Slot 2<br>0011: Slot 3<br>0100: Slot 4<br>0101: Slot 5<br>0110: Slot 6<br>0111: Slot 7<br>Others: Reserved | 0x0 |



| I2SCTRL3: (Address 08h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15 | IV2CH | RW | I2S TX channel data packing mode control<br>When I2SBCK is set to 32*fs mode, Current & Voltage data could be transmitted to I2S Left & Right channels by Using Special Mode<br>0: Legacy<br>1: Special | 0x0 |
| 14 | I2SDOSEL | RW | I2S unused channel data selection<br>0: Zeros<br>1: TXData | 0x0 |
| 13 | DOHZ | RW | Unused channel Data control, When it is set to 0, all Channels are available. Otherwise Unused channel is set to be HiZ<br>0: All<br>1: HiZ | 0x1 |
| 12 | I2SCHS | RW | I2S Tx Channel selection<br>0: Left<br>1: Right | 0x0 |
| 11 | DRVSTREN | RW | I2S_DATAO PAD driving strength setting<br>0: 4mA<br>1: 12mA | 0x1 |
| 10 | I2SRXEN | RW | Disable/Enable I2S receiver module<br>0: Disable<br>1: Enable | 0x1 |
| 9 | I2STXEN | RW | Disable/Enable I2S transmitter module<br>0: Disable<br>1: Enable | 0x0 |
| 8 | Reserved | RW | Not used | 0x0 |
| 7 | ULS_MODE | RW | Ultrasonic mode control<br>0: LowPass<br>1: TDM | 0x0 |
| 6 | ULS_EN | RW | Ultrasonic mode enable<br>0: Disable<br>1: Enable | 0x0 |
| 5:4 | LPBK | RW | I2S data Loopback control bits<br>00: Disable<br>01: Far-Back<br>10: Near-Back<br>11: Reserved | 0x0 |
| 3:0 | Reserved | RW | Not used | 0x8 |

| DACCFG1: (Address 09h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:8 | RVTH | RW | Release Amplitude threshold, which is 90% of the AVTH register value<br>RVTH = round( AVTH * 0.9) | 0x39 |
| 7:0 | AVTH | RW | Attack Amplitude threshold, in percent of signal full scale<br>RMSE = 0 (Peak AGC) : P0= ((i/256*Gain)**2)/$R_{Load}$/2<br>RMSE = 1 (RMS AGC) : P0=(i/256)*(Gain**2)/$R_{Load}$<br>i is the register value<br>Gain is the Amplifier Gain, default 6.7<br>$R_{Load}$ is 8Ω/6Ω/4Ω for different application, default 8Ω | 0x40 |



| DACCFG2: (Address 0ah) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:0 | ATTH | RW | HAGC Attack time threshold, in unit of 20.8μs<br>0: Reserved<br>n: n*20.8us | 0x0030 |

| DACCFG3: (Address 0bh) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:0 | RTTH | RW | HAGC Release time threshold, in unit of 20.8μs<br>0: Reserved<br>n: n*20.8μs | 0x01E0 |

| DACCFG4: (Address 0ch) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:8 | Reserved | RW | Not used | 0x0 |
| 7:0 | HOLDTH | RW | HAGC Hold time before release, in unit of 1.33ms<br>0: Reserved<br>n: n*1.33ms | 0x64 |

| PWMCTRL3: (Address 16h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:14 | Reserved | RW | Not used | 0x2 |
| 13 | NOISE_GATE_EN | RW | Enable/Disable of noise gate function<br>0: Disable<br>1: Enable | 0x0 |
| 12:0 | Reserved | RW | Not used | 0x2BA |

| VBAT: (Address 21h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:10 | Reserved | RO | Not used | 0x0 |
| 9:0 | VBAT_DET | RO | Detected Voltage of battery, and the full scale is 6.025V<br>VBAT=(VBAT_DET)/1023 * 6.025 | 0x2EB |

| TEMP: (Address 22h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:10 | Reserved | RO | Not used | 0x0 |
| 9:0 | TEMP_DET | RO | Detected Die Temperature (Two's Complement), typical values are as follows<br>0x3D8 :-40℃<br>0x000 : 0℃<br>0x019 : 25℃ | 0x019 |

| PVDD: (Address 23h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:10 | Reserved | RO | Not used | 0x0 |
| 9:0 | PVDD_DET | RO | Detected Voltage of PVDD, and the full scale is 7.25V<br>PVDD=(PVDD_DET)/1023 * 7.25 | 0x2A0 |

| BSTCTRL1: (Address 60h) | | | | |
|---|---|---|---|---|
| Bit | Symbol | R/W | Description | Default |
| 15:14 | Reserved | RW | Not used | 0x0 |
| 13:8 | BST_RTH | RW | Smart boost small signal release threshold setting, When the input signal is above the threshold, the voltage of PVDD will be raised up higher than | 0x4 |



| | | | | |
|---|---|---|---|---|
| | | | VBAT in smart boost mode<br>Release threshold = BST_RTH * 1/64 FullScale | |
| 7:6 | Reserved | RW | Not used | 0x0 |
| 5:0 | BST_ATH | RW | Smart boost small signal attack threshold setting. When the input signal is below the threshold, the voltage of PVDD will be equal to VBAT in smart boost mode<br>Attack threshold = BST_ATH * 1/64 FullScale | 0x2 |

BSTCTRL2: (Address 61h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:12 | BST_IPEAK | RW | Boost peak current limiter threshold<br>0000: 1.00A<br>0001: 1.20A<br>0010: 1.40A<br>0011: 1.60A<br>0100: 1.80A<br>0101: 2.00A<br>0110: 2.25A<br>0111: 2.50A<br>1000: 2.75A<br>1001: 3.00A<br>Others: Reserved | 0x5 |
| 11:8 | BST_TDEG | RW | Smart Boost small signal level detection deglitch time<br>0000: 0.50ms<br>0001: 1.00ms<br>0010: 2.00ms<br>0011: 4.00ms<br>0100: 8.00ms<br>0101: 10.7ms<br>0110: 13.3ms<br>0111: 16.0ms<br>1000: 18.6ms<br>1001: 21.3ms<br>1010: 24.0ms<br>1011: 32.0ms<br>1100: 64.0ms<br>1101: 128ms<br>1110: 256ms<br>1111: 1200ms | 0xB |
| 7 | Reserved | RW | Not used | 0x0 |
| 6:5 | BST_MODE | RW | BOOST mode selection<br>00: Transparent<br>01: Force Boost<br>10: Smart Boost 1<br>11: Smart Boost 2 | 0x3 |
| 4:0 | BST_VOUT_SET | RW | BOOST max output voltage control bits (0.125V/Step)<br>00111: 4V<br>01000: 4.125V<br>01001: 4.25V<br>01010: 4.375V<br>...<br>11000: 6.125V<br>11001: 6.25V<br>Others: Reserved | 0xB |



# APPLICATION INFORMATION

## EXTERNAL COMPONENTS

### *BOOST INDUCTOR SELECTION*

Inductance value is limited by the boost converter's internal loop compensation, a large $L_{SW}$ will reduce the phase margin of the DC-to-DC converter. Also, the inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency under all operating conditions, the recommended value of inductor is 1μH.

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, inductance value will decline since the magnetic core begins to saturate; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. The inductor saturation current rating could to be considered with the following equation:

$$I_{L\_PEAK} = \frac{2 * P_{Out}}{\eta * V_{BAT}} + \frac{V_{BAT} * (V_{PVDD} - V_{BAT})}{2 * L_{SW} * F_{BST} * V_{PVDD}}$$

Following is the inductor selection reference for typical speaker impedances.

| $V_{BAT}$ (V) | PVDD (V) | $R_L$ (Ω) | $I_{PEAK}$ (A) | Total Eff. η (%) | $P_{out}$ (W) | $I_{L\_PEAK}$ (A) | $I_{SAT\_min}$ (A) |
|---|---|---|---|---|---|---|---|
| 4.2 | 6.25 | 8 | 2.0 | 86 | 2.0 | 1.54 | 2.75 |
| 4.2 | 6.25 | 6 | 2.0 | 86 | 2.5 | 1.81 | 2.75 |
| 4.2 | 6.25 | 4 | 2.5 | 82 | 3.0 | 2.17 | 2.75 |

### *BOOST CAPACITOR SELECTION*

Boost output capacitor is usually within the range 0.1μF~47μF. The ceramic capacitors with low ESR are recommended for low ripple voltage which is determined as following equation:

$$\Delta V_{PVDD} = \frac{(V_{PVDD} - V_{BAT}) * I_{OUT}}{\eta * V_{PVDD} * F_{BST} * C_{OUT}} + \left(\frac{I_{OUT} * V_{PVDD}}{V_{BAT}} + \frac{V_{BAT} * (V_{PVDD} - V_{BAT})}{2 * L_{SW} * F_{BST} * V_{PVDD}}\right) * R_{C\_ESR}$$

Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the material, size, capacitor voltage, and capacitance values. It is suggested to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically $BaTiO_3$), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance.

Please notice the DC bias characteristics when selecting capacitors. For typical applications, it is necessary to ensure that the residual capacitance is higher than **3μF.** Take the following capacitances as the output capacitor of boost for example:

| Value | Material | Size ($mm^3$) | Rated Voltage | Quantity | Value@6.25V |
|---|---|---|---|---|---|
| 10μF | X5R | 1.00×0.50×0.50 (0402) | 10V | 2 | 3.2μF |
| 10μF | X5R | 2.00×0.80×0.85 (0805) | 16V | 1 | 3.5μF |



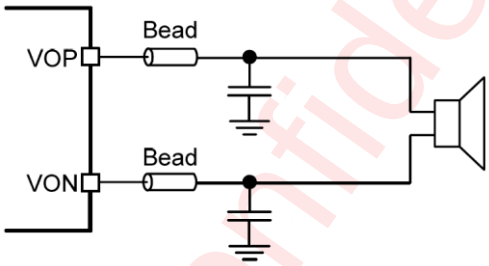
 

### *SUPPLY DECOUPLING CAPACITOR*

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A 0.1μF low equivalent-series-resistance (ESR) ceramic capacitor are recommended. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the DEVICE is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

### *FILTER FREE OPERATION AND FERRITE BEAD FILTERS*

If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 10V.




## LAYOUT CONSIDERATION

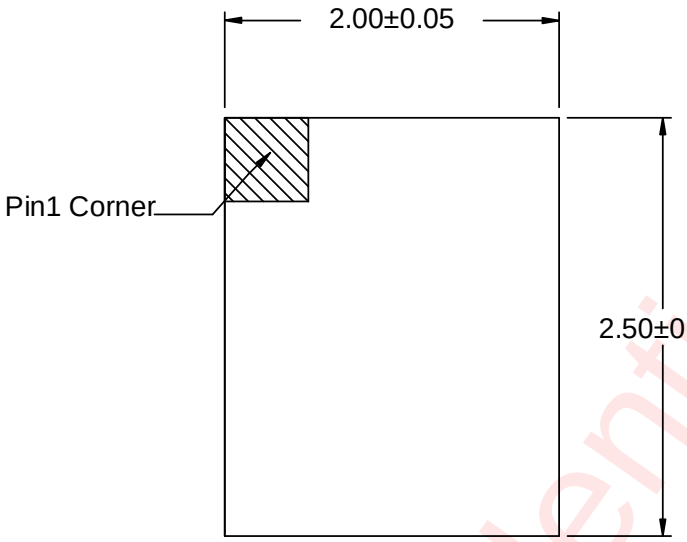
In order to obtain excellent performance of the PA, the below PCB layout guidelines should be followed:

1. All the filter capacitors should be placed close to the corresponding pins of the PA, including VBST, VBAT, DVDD.
2. The traces of SW pin should support currents up to the device over-current limit (peak current 2.75A).
3. It is recommended to provide a separate, short and thick power line to the PA, the copper width is recommended to be larger than 0.75mm.
4. The beads and capacitor should be placed close to the VON and VOP pin. The output line from PA to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.
5. The via numbers determine the current capability. Typically, the boost converter trace need four via to handle the current requirement around 2.5A.
6. The capacitance on the output lines or on the long speaker tracks should be less than 1nF.

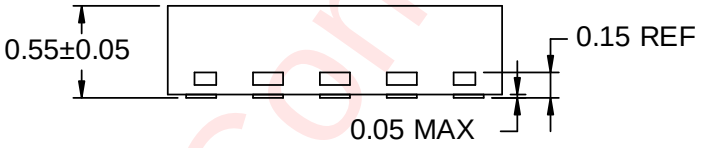


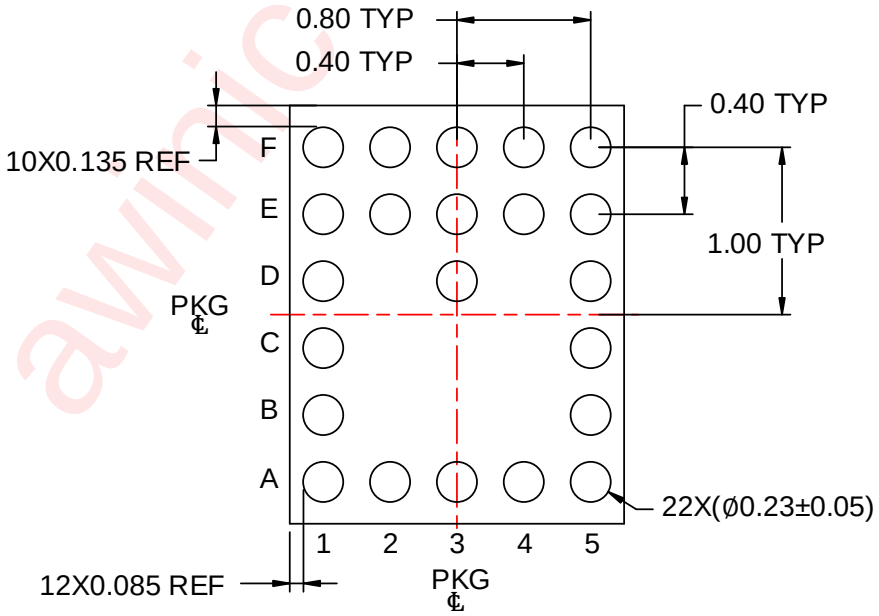
## PACKAGE DESCRIPTION




**Top View**




**Side View**



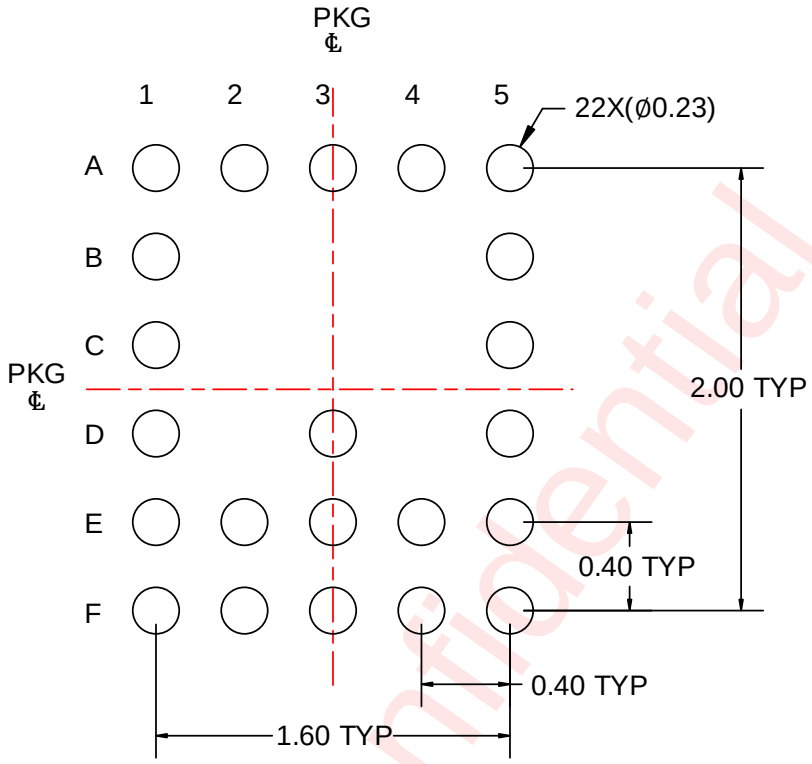

**Bottom View**

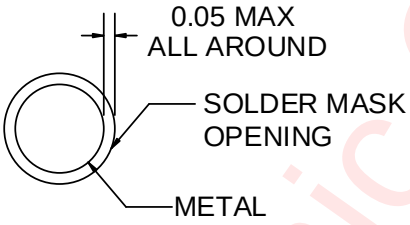
Unit:mm



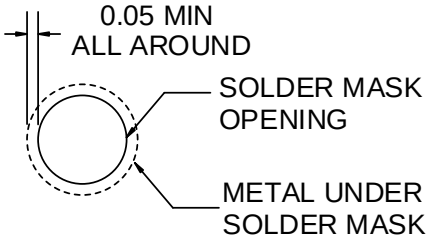
 

## LAND PATTERN DATA




NON SOLDER MASK DEFINED




SOLDER MASK DEFINED

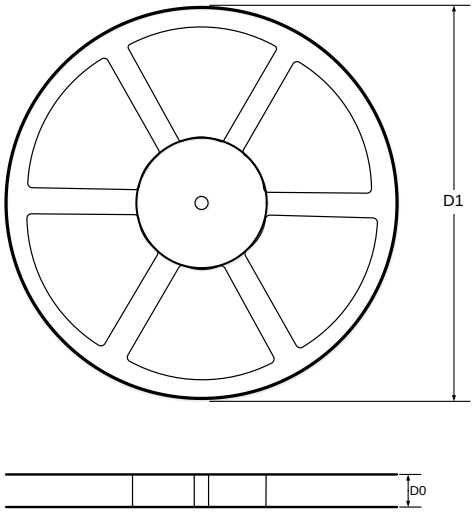
Unit: mm



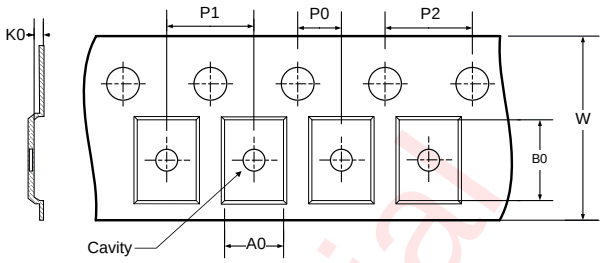
 

# TAPE AND REEL INFORMATION

REEL DIMENSIONS

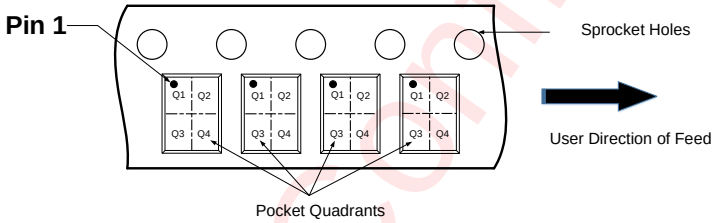



TAPE DIMENSIONS




A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| 330 | 12.40 | 2.20 | 2.67 | 0.83 | 2 | 8 | 4 | 12 | Q1 |

**All dimensions are nominal**



# REVISION HISTORY

| Version | Date | Change Record |
|---|---|---|
| V1.0 | Oct. 2022 | Officially Released |
| V1.1 | Apr.2023 | 1. Fix typo<br>2. Updated the register map<br>3. Updated the Block Diagram of SKTune algorithm<br>4.Modify package description and land pattern data |
| V1.2 | May.2023 | Add 4Ω application description |
| V1.3 | Nov.2023 | 1.Add typical characteristic curves about 4Ω application<br>2.Updated $I^2C$ interface timing<br>3.Add standby mode current |



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