Multi-Channel Half-Bridge Drivers with Advanced Diagnostics

Features

- Twelve half bridge power outputs
- Low power consumption in sleep mode
- 3.3/5V compatible inputs with hysteresis
- All outputs with overload and short circuit protection
- Independently diagnosable outputs (overcurrent)
- 16-bit Standard SPI interface with daisy chain and in-frame response capability for control and diagnosis
- Fast diagnosis with the global error flag
- PWM capable outputs for frequencies 80Hz, 100Hz and 200Hz, with 8-bit duty cycle resolution
- In the enhanced PWM can output the frequencies 400Hz, 800Hz, 2000Hz.
- Over-temperature pre-warning and protection
- Over and Under voltage lockout
- Cross current protection

Applications

- HVAC Flap DC motors
- Monostable and bistable Relays
- Side mirror x-y adjustment and mirror fold
- LED applications
- Multiple brushed DC motors and solenoids

General Description

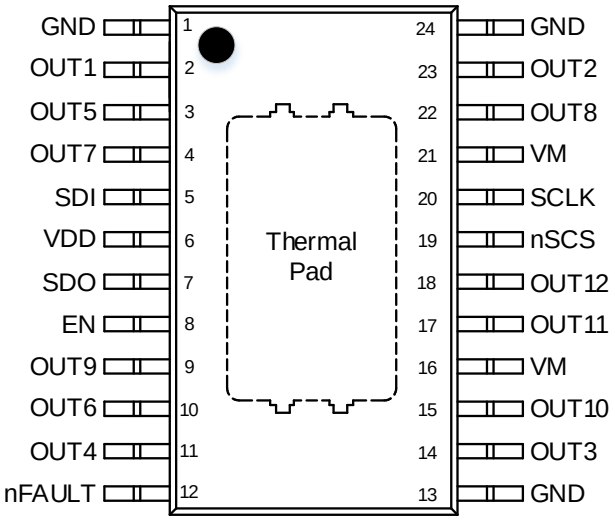
The AWD89XXTSR is a protected twelve-fold half-bridge driver designed especially for automotive motion control applications such as Heating, Ventilation and Air Conditioning (HVAC) flap DC motor control. It is part of a larger family offering half-bridge drivers from three outputs to twelve outputs with direct interface or SPI interface.

The half bridge drivers are designed to drive DC motor loads in sequential or parallel operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a 16-bit SPI interface. It offers diagnosis features such as short circuit, power supply failure and over temperature detection. In combination with its low quiescent current, this device is attractive among others for automotive applications. The small fine pitch exposed pad package, WBETSSOP-24L, provides good thermal performance.

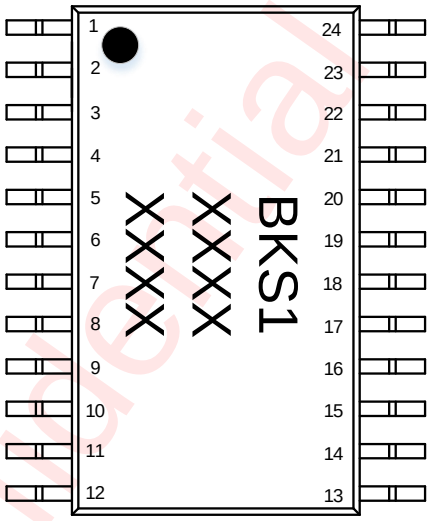
Pin Configuration And Top Mark

AWD8912TSR

AWD8912TSR
(Top view)



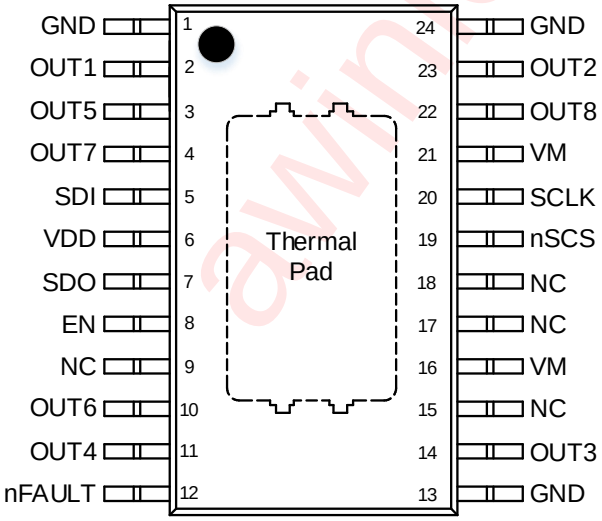
AWD8912TSR Marking
(Top View)



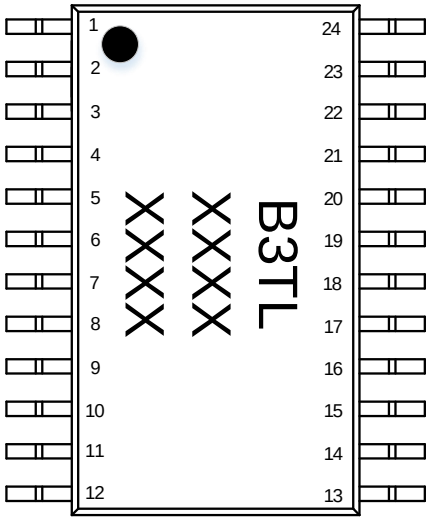
BKS1 - AWD8912TSR
XXXX/XXXX - Production Tracing Code

AWD8908TSR

AWD8908TSR
(Top view)



AWD8908TSR Marking
(Top View)



B3TL - AWD8908TSR
XXXX/XXXX - Production Tracing Code

Pin Definition

AWD8912TSR

PIN		TYPE	DESCRIPTION
NAME	No.		
GND	1	PWR	Device power ground. Connect the GND pin to the system ground.
GND	13	PWR	
GND	24	PWR	
OUT1	2	O	Power half-bridge 1 output
OUT5	3	O	Power half-bridge 5 output
OUT7	4	O	Power half-bridge 7 output
OUT9	9	O	Power half-bridge 9 output
OUT6	10	O	Power half-bridge 6 output
OUT4	11	O	Power half-bridge 4 output
OUT3	14	O	Power half-bridge 3 output
OUT10	15	O	Power half-bridge 10 output
OUT11	17	O	Power half-bridge 11 output
OUT12	18	O	Power half-bridge 12 output
OUT8	22	O	Power half-bridge 8 output
OUT2	23	O	Power half-bridge 2 output
VDD	6	PWR	Logic supply voltage. Connect a X5R or X7R, 0.1μF, VDD-rated ceramic capacitor.
nSCS	19	I	Serial chip select. Internal pull-up. A logic low on this pin enables serial interface communication.
SCLK	20	I	Serial clock input with internal pull down
SDI	5	I	Serial data input with internal pull-down. Data is captured on the falling edge of the SCLK pin.
SDO	7	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
nFAULT	12	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.
EN	8	I	Driver enable pin. Internal pull-down. When this pin is logically low, the device enters low power mode.
VM	16	PWR	Main supply voltage for power half bridge. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1μF, VM-rated ceramic capacitor and greater than or equal to 10μF bulk capacitance between the VM and GND pins.
VM	21	PWR	
	Thermal PAD		Connect to ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

AWD8908TSR

PIN		TYPE	DESCRIPTION
NAME	No.		
GND	1	PWR	Ground. All ground pins should be externally together.
GND	13	PWR	
GND	24	PWR	
NC	9	-	Not connected
NC	15	-	Not connected
NC	17	-	Not connected
NC	18	-	Not connected
OUT1	2	O	Power half-bridge 1 output
OUT5	3	O	Power half-bridge 5 output
OUT7	4	O	Power half-bridge 7 output
OUT6	10	O	Power half-bridge 6 output
OUT4	11	O	Power half-bridge 4 output
OUT3	14	O	Power half-bridge 3 output
OUT8	22	O	Power half-bridge 8 output
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VM	21	PWR	
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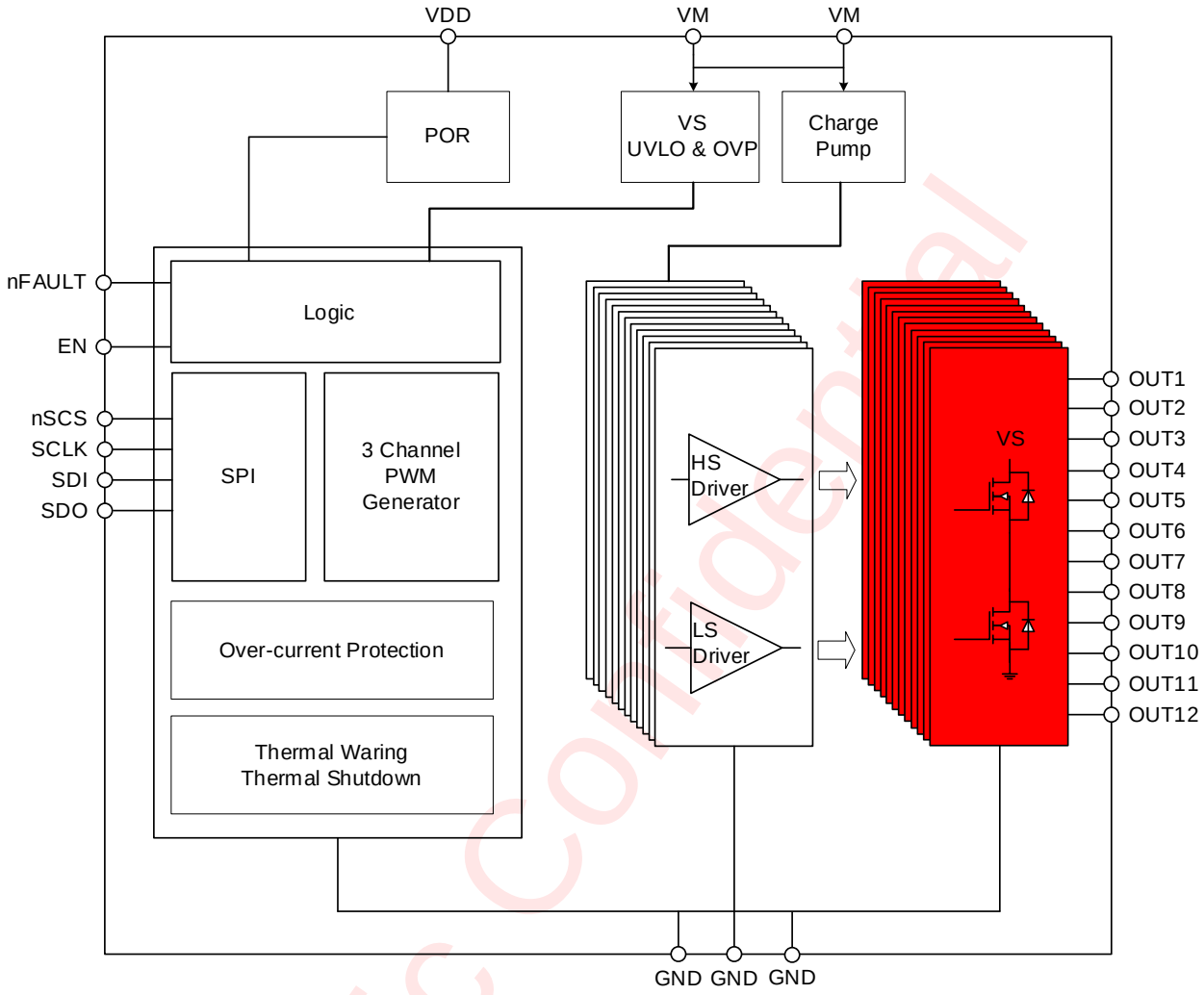
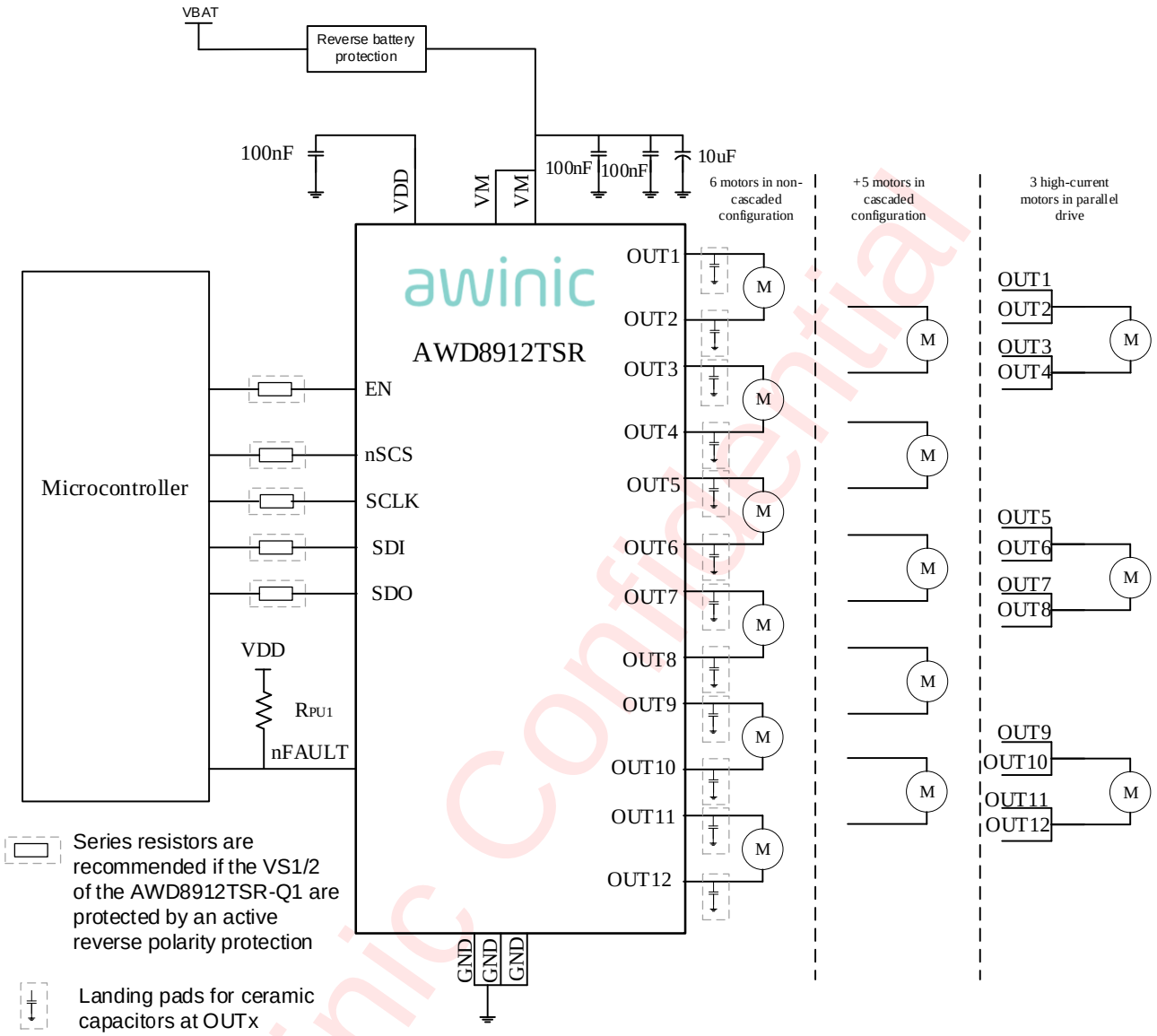
Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWD8912TSR	-40°C ~125°C	WBETSSOP-24L	BKS1	MSL3	ROHS+HF	3000 units/ Tape and Reel
AWD8908TSR	-40°C ~125°C	WBETSSOP-24L	B3TL	MSL3	ROHS+HF	3000 units/ Tape and Reel

Typical Application Circuits



Absolute Maximum RATINGS(NOTE1)

PARAMETERS	RANGE
Power supply voltage (VM)	-0.3V to 40V
Logic supply pin voltage (VDD)	-0.3V to 5.5V
Output pin voltage (OUTx)	-0.3V to VM
Logic pin input voltage (nSCS, EN, SCLK, SDI)	-0.3V to 5.5V
Logic pin output voltage (nFAULT, SDO)	-0.3V to 5.5V
Continuous supply current (VM pins combined)	0 to 6A
Peak drive current (OUTx)	Internally limited
Continuous sink current (GND pins combined)	0 to 6A
Junction-to-ambient thermal resistance θ_{JA}	30.2°C /W
Operating free-air temperature range	-40°C to 125°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature TSTG	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including HBM CDM)	
HBM(Human Body Model)	±2000V
CDM(Charge Device Model)	±1500V
Latch-Up	
Test Condition: JEDEC STANDARD NO.78F.01	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		Range	Unit
V_{VM}	Power supply voltage(VM)	4.5 to 32	V
V_{DD}	Logic supply voltage (VDD)	3 to 5.5	V
V_{IN}	Logic input voltage (nSCS, EN, SCLK, SDI)	0 to 5.5	V
V_{OD}	Open drain pullup voltage (nFAULT)	0 to 5.5	V
I_{OD}	Open drain pullup current (nFAULT)	0 to 5.0	mA
V_{OP}	Push-pull pullup voltage (SDO)	0 to 5.5	V
I_{OP}	Push-pull output current (SDO)	0 to 5.0	mA
T_A	Operating ambient temperature	-40 to 125	°C
T_J	Operating junction temperature	-40 to 150	°C

Electrical Characteristics

Electrical characteristics: VM=5.5V to 32V, VDD = 3.0V to 5.5V,

Typical values refer to VM=13.5V and VDD=3.3V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLIES(VM,VDD)						
I_{VMQ}	VM sleep mode current			0.9		μA
I_{VDDQ}	VDD sleep mode current			0.1		μA
I_{VMS}	VM standby mode current			0.03		mA
I_{VDDS}	VDD standby mode current			1.6		mA
I_{VM}	VM operating mode current			2		mA
I_{VDD}	VDD operating mode current			1.6		mA
t_{Wake}	Wake-up time	EN high to SPI ready		150		μs
LOGIC-LEVEL INPUTS (EN, SCLK, SDI)						
V_{IL}	Input logic low voltage				0.3*VDD	V
V_{IH}	Input logic high voltage		0.7*VDD			V
V_{HYS}	Input logic hysteresis			500		mV
I_{IL}	Input logic low current			0		μA
I_{IH}	Input logic high current			82.5		μA
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage				0.3*VDD	V
V_{IH}	Input logic high voltage		0.7*VDD			V
V_{HYS}	Input logic hysteresis			500		mV
I_{IL}	Input logic low current			66		μA
I_{IH}	IIH Input logic high current			0		μA
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{out} = 5mA			0.4	V
I_{OH}	Output logic high current				0.1	μA
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{SDOH}=1.6mA		0.2		V
V_{OH}	Output logic high voltage	I_{SDOH}=1.6mA		VDD-0.2		V
I_{SDOLK}	Tri-state leakage Current	$V_{CSN}=V_{DD}$,0V<V_{SDO}<V_{DD}	-1		1	μA
DRIVER OUTPUTS (OUTx)						
$R_{DS(ON)}$	High-side MOSFET on resistance	I_{OUT}=0.5A		750		Ω
	Low-side MOSFET on resistance	I_{OUT}=0.5A		750		Ω

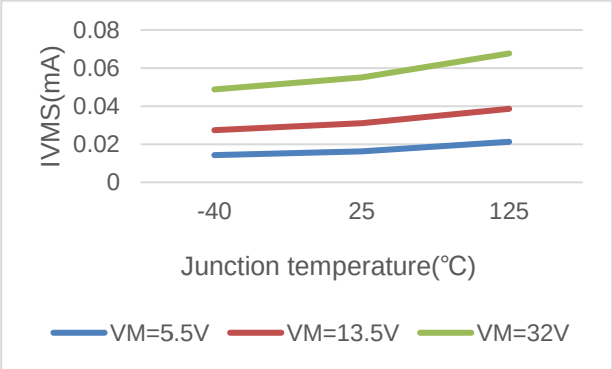
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SR	Output rise and fall time (high-side and low-side)	ENH_SR=0		0.45		V/μs
		ENH_SR=1		2.5		V/μs
t_{DEAD}	Output dead time (high to low / low to high)			120		μs
I_{LEAK}	Leakage current low-side				0.1	μA
	Leakage current high-side				0.1	μA
PWM MODE						
f_{PWM}	PWM switching frequency	PWM_FREQ=01, PWM_ENH_FREQ=0		80		Hz
		PWM_FREQ=10, PWM_ENH_FREQ=0		100		Hz
		PWM_FREQ=11, PWM_ENH_FREQ=0		200		Hz
		PWM_FREQ=01, PWM_ENH_FREQ=1		400		Hz
		PWM_FREQ=10, PWM_ENH_FREQ=1		800		Hz
		PWM_FREQ=11, PWM_ENH_FREQ=1		2000		Hz
OUTPUT SWITCHING TIMES						
t_{dONH}	Output delay time high side driver on	Resistive load=100Ω to GND		20		us
t_{dOFFH}	Output delay time high side driver off	Resistive load=100Ω to GND		45		us
t_{dONL}	Output delay time low side driver on	Resistive load=100Ω to VM		20		us
t_{dOFFL}	Output delay time low side driver off	Resistive load=100Ω to VM		45		us
t_{DHL}	Cross current protection time, high to low	Resistive load=100Ω		130		Us
t_{DLH}	Cross current protection time, low to high	Resistive load=100Ω		130		us
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising		4.7		V
		Supply falling		4.3		V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling theshold		400		mV
V_{OVP}	Supply overvoltage protection (OVP)	Supply rising, EXT_OVP=0		24		V
		Supply falling, EXT_OVP=0		23		V
		Supply rising, EXT_OVP=0		35		V
		Supply falling, EXT_OVP=0		33		V
V_{OVP_HYS}	Supply overvoltage protection			1		V

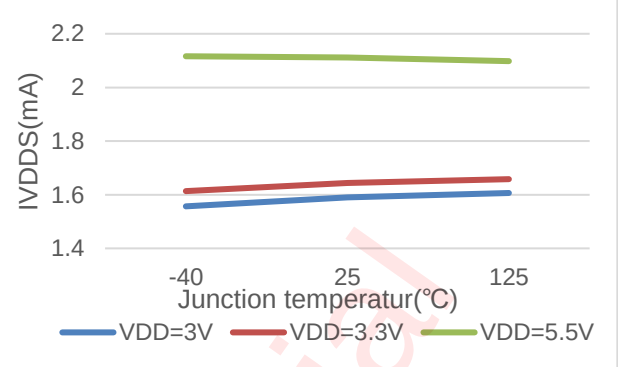
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{POR}	Logic undervoltage (POR)	Supply rising		2.7		V
		Supply falling		2.6		V
V_{POR_HYS}	Logic undervoltage hysteresis	Rising to falling theshold		100		mV
I_{OCP}	Overcurrent protection trip point			1.5		A
t_{OCP}	Overcurrent protection deglitch time			20		μs
T_{JW}	Thermal warning junction temperature			145		℃
T_{JSD}	Thermal shutdown junction temperature			175		℃

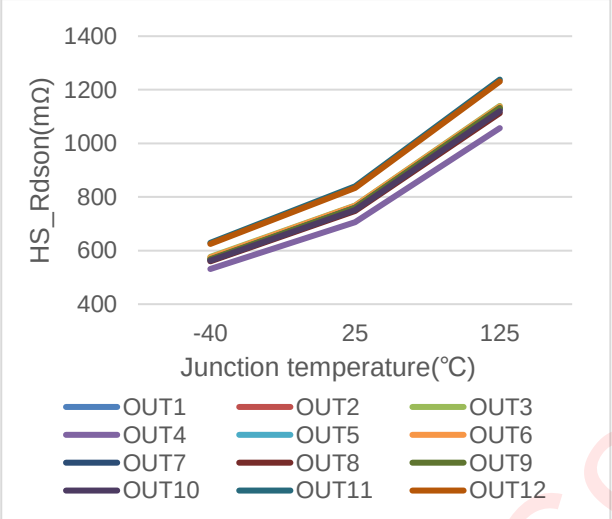
Timing Requirements

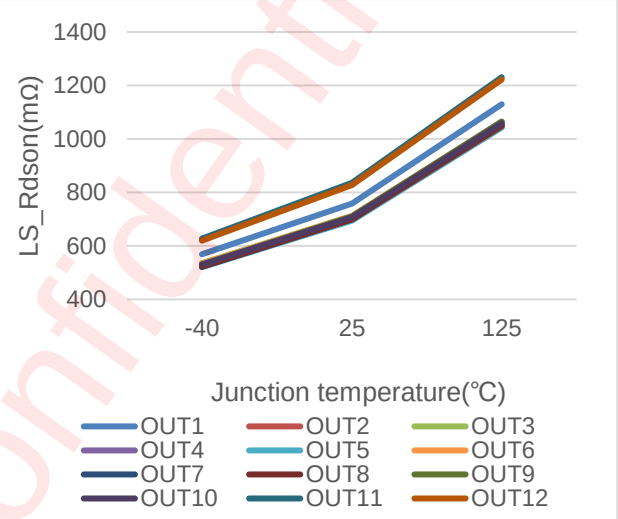
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SPI (nSCS, SCLK, SDI, SDO)						
t_{READY}	SPI ready after after enable	VDD = 3.3V		150		μs
t_{CLK}	SCLK minimum period	VDD = 3.3V	200			ns
t_{CLKH}	SCLK minimum high time	VDD = 3.3V	0.45*t_{pCLK}		0.45*t_{pCLK}	ns
t_{CLKL}	SCLK minimum low time	VDD = 3.3V	0.45*t_{pCLK}		0.45*t_{pCLK}	ns
t_{SU_SDI}	SDI input data setup time	VDD = 3.3V	30			ns
t_{HD_SDI}	SDI input data hold time	VDD = 3.3V	30			ns
t_{SU_nSCS}	nSCS input setup time	VDD = 3.3V	250			ns
t_{HD_nSCS}	nSCS input hold time	VDD = 3.3V	250			ns
t_{HI_nSCS}	nSCS minimum high time before active low	VDD = 3.3V	600			ns
t_{DIS_nSCS}	nSCS disable delay time	VDD = 3.3V		30		ns

Typical Characteristics









Detailed Functional Description

General Description

Power Supply

The AWD89XXTSR features two power supply inputs, VM and VDD. The half bridge outputs are powered by VM, which is connected to the high power supply rail. VDD is responsible for supplying the I/O buffers and internal voltage regulator of the device.

The separate VM and VDD supplies ensure the integrity of information stored in the logic block in the event of voltage dropouts or disturbances on VM. Consequently, the system can continue to operate once VM has recovered, without requiring retransmission of commands to the device.

A rising edge on VDD crossing VDD POR triggers an internal Power-On Reset (POR) to initialize the IC at power-on. This process involves the deletion of all internally stored data, and the switching off of outputs (high impedance).

It is recommended to place an electrolytic capacitor and a 100nF ceramic capacitor as close as possible to the VM supply pin of the device to enhance EMC performance in the high and low frequency bands. The electrolytic capacitor must be sized to prevent the VM voltage from exceeding the absolute maximum rating. Additionally, decoupling capacitors are advised for the VDD supply pin.

Reset Behavior

The reset of the AWD89XXTSR device includes VDD undervoltage reset and EN pin reset. After the chip is successfully reset, a reset event will be triggered, and the NPOR register will be set to 0. After reading the NPOR register status, NPOR will be set to 1.

VDD undervoltage reset:

When VDD falls below the undervoltage threshold , the SPI interface will stop working, the digital module will be disabled, the logic content will be cleared, and the output stage will be turned off. Once the VDD voltage level is higher than the undervoltage threshold, the VDD POR will be triggered, and the digital block will be initialized.

EN pin reset:

If the EN pin is pulled low, the logic content will be reset, and the device will enter sleep mode. When EN is pulled high and VDD is above the undervoltage threshold, AWD89XXTSR enters normal working mode.

Sleep Mode(EN = 0)

The AWD89XXTSR device enters sleep mode by setting the EN input Low. The EN input has an internal pull-down resistor. In sleep mode, all output transistors are turned off, the SPI register banks are reset, and the chip enters low power mode.

Operating Mode(EN = 1)

The AWD89XXTSR device enters Operating Mode by setting the EN input High. In Operating Mode, the charge pump is active and all output transistors can be configured via SPI.

Fault Mode

The AWD89XXTSR is protected against various faults, as listed in Table 1. The table provides a list of different fault conditions, the corresponding protection mechanisms, and recovery states. When a relevant fault occurs, the status register will change accordingly. Some faults can be indicated through the hardware output of the nFAULT pin.

Table 1 Fault Action and Response

FAULT	CONDITION	REPORT	HALF BRIDGE	LOGIC	RECOVERY
SPI Error	SPI communication abnormality	nFAULT Pin Pull down GLB_STAT SPI_ERR=1	Operating	Active	
VM Undervoltage (UVLO)	VM<V_{UVLO}	nFAULT Pin Pull down GLB_STAT VM_UV=1	High-Z	Reset	Automatic: VM> V_{UVLO} + V_{UVLO_HYS}
VM Overvoltage (OVP)	VM>V_{OVP}	nFAULT Pin Pull down GLB_STAT VM _OV=1	High-Z	Active	Automatic: VM< V_{OVP} - V_{OVP_HYS}
Temperature Shutdown (TSD)	T_J > T_{JSD} (Typ. 175°C)	nFAULT Pin Pull down GLB_STAT TSD=1	High-Z	Active	
Temperature Warning (TPW)	T_J > T_{JW} (Typ. 145°C)	nFAULT Pin Pull down GLB_STAT TPW=1	Operating	Active	
Overcurrent Protection (OCP)	I_{OUT} > I_{OCP}	nFAULT Pin Pull down HB_X_HS/LS_OC=1	High-Z	Active	

Half Bridge Drivers

The half-bridge drivers can be programmed to drive loads (motor, solenoids, LEDs) in 100% duty cycle with PWM or in chopping mode (with PWM) and in parallel operation for driving high current.

Half-bridge operation with PWM enabled

The AWD89XXTSR device has PWM capabilities for all of its half-bridge outputs. These outputs can be used to drive inductive loads, such as DC brush motors, or optionally resistive loads, such as LEDs. Each half-bridge output is allocated up to three PWM channels with individual duty cycle settings at 8-bit resolution. Each channel can be mapped to up to three PWM frequency options: 80Hz, 100Hz, and 200Hz, in the enhanced PWM can output the frequencies 400Hz, 800Hz, 2000Hz. This feature allows for highly flexible PWM operation when driving loads with different control profiles. Detailed parameter settings can be found in Table 2.

During PWM operation, the frequency and duty cycle can be changed as needed for the desired half-bridge output. The internal logic circuitry prevents glitches in the PWM output waveform that may occur due to on-demand changes in PWM operation.

When operating with motor loads, the device offers an active or passive free-wheeling configuration through SPI. This allows selection of the speed at which the inductive current can decay over the full-bridge circuit. The default setting is passive free-wheeling.

Table 2 PWM capability and frequency selection per half-bridge output

Control Register：HBx_MODE	PWM Frequency 80Hz Control Register :	PWM Frequency 100Hz Control Register:	PWM Frequency 200Hz Control Register:
PWM Channel 1 （HBx_MODE=01b）	PWM_CH1_FREQ=01b	PWM_CH1_FREQ=10b	PWM_CH1_FREQ=11b
PWM Channel 2 （HBx_MODE=10b）	PWM_CH2_FREQ=01b	PWM_CH2_FREQ=10b	PWM_CH2_FREQ=11b
PWM Channel 3 （HBx_MODE=11b）	PWM_CH3_FREQ=01b	PWM_CH3_FREQ=10b	PWM_CH3_FREQ=11b

Inductive Load

An illustration of a full bridge combination drive example is shown in Figure 1, with OUT1 and OUT2 driving a DC brush motor. In this configuration, HS1 is always driven, while LS2 is driven in PWM operation. HS2 is used to actively freewheel (FW) the motor current load, thereby reducing the power dissipation of the device.

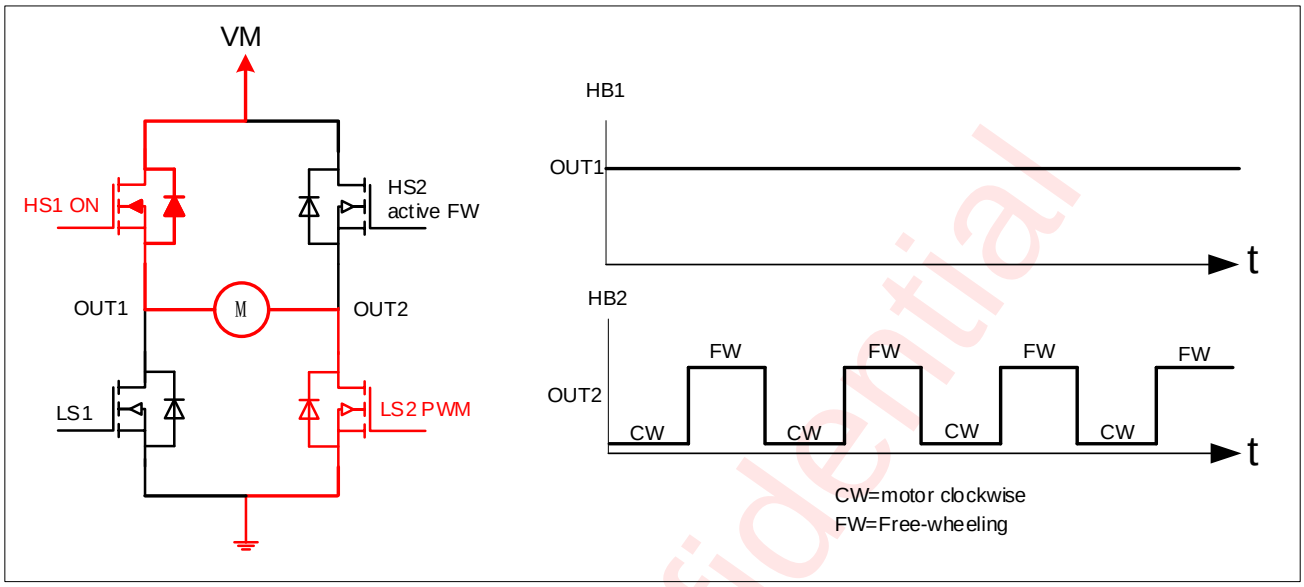


Figure 1 The considered output is not put in parallel with another one

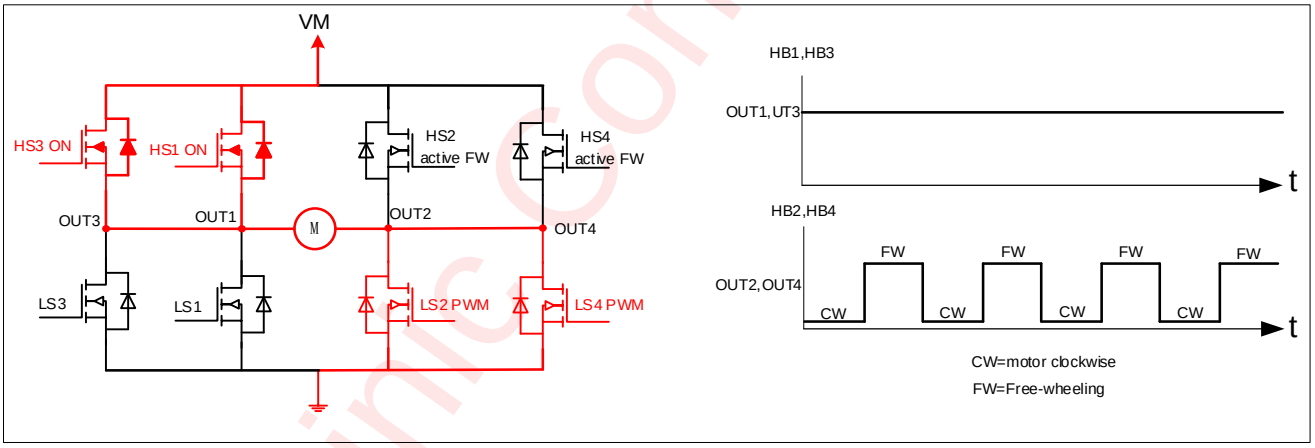


Figure 2 The considered output is put in parallel with another one

Assuming HBx Mode = 00 and considering HSx and LSx are in the off state (tri-state). Based on the two application scenarios of non-parallel output and parallel output, the device operation can be controlled by correctly configuring the register values through SPI.

Option 1: The considered output **is not put in parallel with another one**

1. Configure PWM_CHx_FREQ to 00 (PWM is stopped and off) for selected PWM channel.
2. Configure active or passive free-wheeling of the inductive decay current in FW_OL_CTRL and FW_CTRL register.
3. Assign an appropriate PWM channel for selected half-bridge output in HB_MODE_x_CTRL register.
4. Configure the duty cycle of the selected half-bridge output in PWMx_DC_CTRL register.
5. Select the PWM frequency in PWM_CHx_FREQ register to begin the PWM period.
6. Activate the channel to be driven in PWM operation: HBx_HS_EN or HBx_LS_EN in the HB_ACT_x_CTRL register.

Opton 2: Outputs controlled by different control registers are put paralleled. This sequence ensures that corresponding HS or LS are activated simultaneously

1. Configure PWM_CHx_FREQ to 00 (PWM is stopped and off) for selected PWM channel.
2. Configure active or passive free-wheeling of the inductive decay current in FW_1_CTRL and FW_2_CTRL register.
3. Assign an appropriate PWM channel for selected half-bridge output in HB_MODE_x_CTRL register.
4. Configure the duty cycle of the selected half-bridge output in PWMx_DC_CTRL register.
5. Activate the channel to be driven in PWM operation: HBx_HS_EN or HBx_LS_EN in the HB_ACT_x_CTRL register.
6. Select the PWM frequency in PWM_CHx_FREQ register to begin the PWM period.

Careful attention should be paid to the free-wheeling configuration of the half-bridge required to be driven in PWM operation. For example, in the event a high-side channel is activated and assigned a PWM channel, and active free-wheeling is selected, but a frequency mode of '00' (PWM is stopped and off) is configured in the PWM_FREQ_CTRL register, then the respective high-side channel will be configured low and the adjacent low-side channel within the half-bridge will be enabled. This is a result of enabling active free-wheeling.

Slew Rate

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy, and duration of diode recovery spikes and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in Figure 3 .

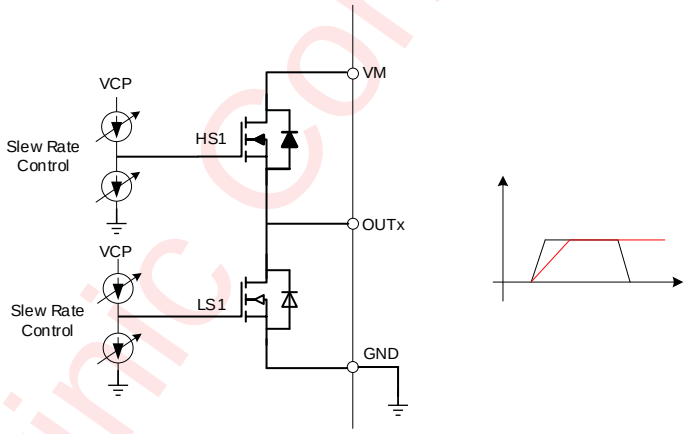


Figure 3 Slew Rate Circuit Implementation

The slew rate can be adjusted by HB_ENHSR bit in PWM_ENHSR_CTRL register. When the HB_HEHSR bit is set to 0, the slew rate of all half-bridge outputs is 0.45V/us. When the HB_HEHSR bit is set to 1, the slew rate of all half-bridge outputs is 2.5V/us.The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in Figure 4.

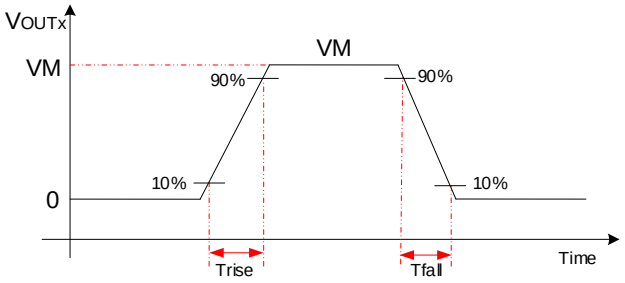


Figure 4 Slew Rate Timings

Protection Circuits

The AWD89XXTSR device is fully protected against undervoltage, overcurrent, over-temperature events.

VM Supply Undervoltage Lockout (UVLO)

When the chip is in operation, if the input supply voltage on the VM pin falls below the V_{UVLO} threshold, all of the half-bridges are disabled, and the nFAULT pin is driven low, as shown in Figure 5. In the global status register (GLB_STAT), the VM_UV bit is also latched high. Normal operation resumes (driver operation and nFAULT pin release) when the VM undervoltage condition is removed. The VM_UV bit in the status register (GLB_STAT) remains set until it is cleared by reading the VM_UV status register.

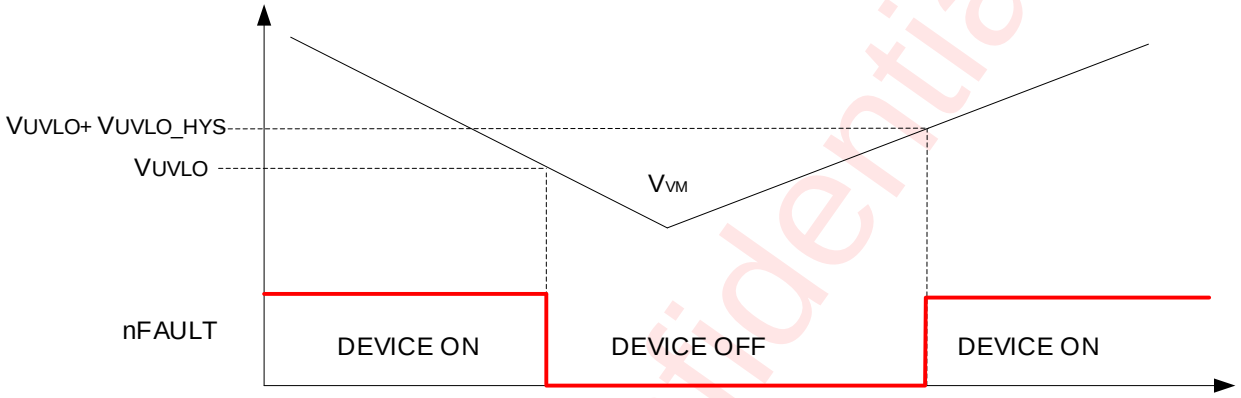


Figure 5 VM UVLO Operation

VM Supply Overvoltage Protection (OVP)

If at any time, the input supply voltage on the VM pin rises above the V_{OVP} threshold, all of the half-bridges will be disabled, the charge pump will be disabled, and the nFAULT pin will be driven low as shown in Figure 6. The VM_OV bit will also be set high in the global status register (GLB_STAT). Normal operation will resume (driver operation and the nFAULT pin will be released) when the VM overvoltage condition is removed. The VM_UV bit will remain set until cleared by reading the VM_OV status register.

In addition, this device also supports extended overvoltage operation for a higher over-voltage range up to 32V. This operation can be enabled by setting the EXT_OVP bit in the configuration (PWM_ENHSR_CTRL) register. The EXT_OVP bit is configured as 1 by default (34.5V), and when configured as 0, the OVP voltage is set to 22V.

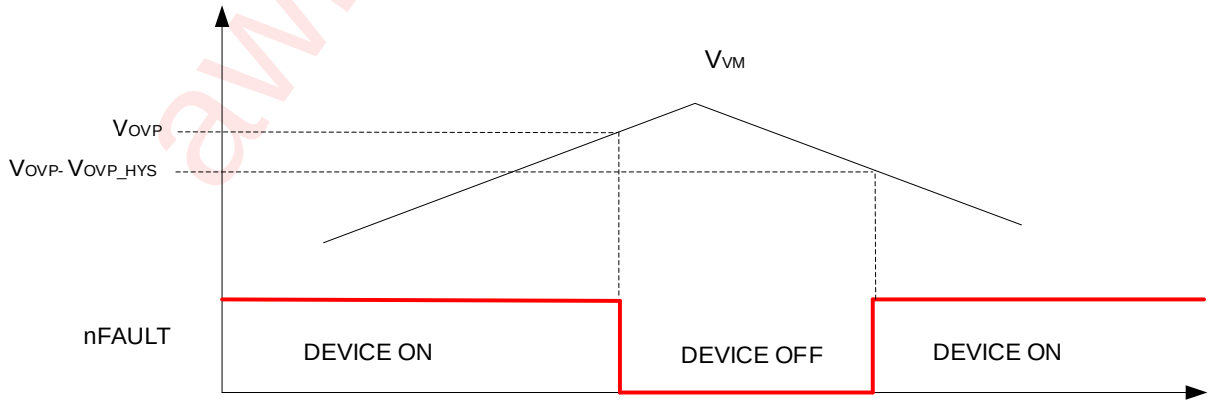


Figure 6 VM OVP Operation

Overcurrent Protection (OCP)

Each MOSFET of the device has a current-limit circuit that limits the current through the MOSFET by removing the gate drive signal. If this current limit exceeds the t_{OCP} deglitch time, the high-side and low-side FETs in the corresponding half bridge will be disabled, and the nFAULT pin will be driven low. The corresponding bits in the overcurrent protection status register (OCP_STAT_x) will be latched high. The charge pump will remain active in this state, and the corresponding bits (HBx_HS_OC / HBx_LS_OC) in the overcurrent protection status register (OCP_STAT_x) will remain set until cleared by reading the (OCP_STAT_x) status register.

Thermal Warning (OTW)

If the device temperature exceeds the trip point of the thermal warning (T_{JW}), the TPW bit is set in the global status register (GLB_STAT). The device performs no additional action and continues to function. The TPW bit remains set until cleared by reading the TPW status in the global status register (GLB_STAT).

Thermal Shutdown (TSD)

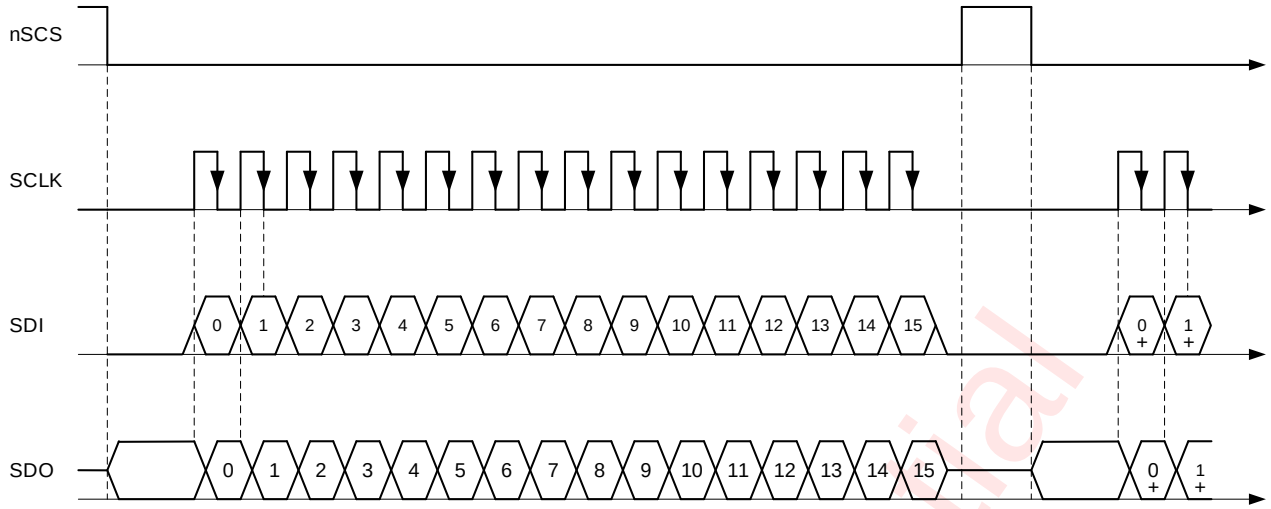
If the die temperature exceeds the trip point of the thermal shutdown limit (T_{JSD}), all half-bridge drivers are disabled, the charge pump is shut down, and the nFAULT pin is driven low. Additionally, the TSD bit is set in the global status register (GLB_STAT). The TSD bit remains latched high indicating that a thermal event occurred until cleared by reading the TSD status in the global status register (GLB_STAT).

SERIAL PERIPHERAL INTERFACE(SPI)

The AWD89XXTSR has a 16-bit SPI interface for output control and diagnostics. This section describes the SPI protocol, the control and status registers.

SPI DESCRIPTION

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input SCLK provided by the microcontroller. SCLK must be Low during nSCS falling edge (Clock Polarity = 0). The SPI incorporates an in-frame response: the content of the addressed register is shifted out at SDO within the same SPI frame.The transmission cycle begins when the chip is selected by the input nSCS (Chip Select Not), Low active. After the nSCS input returns from Low to High, the word that has been read is interpreted according to the content. The SDO output switches to tri-state status (High impedance) at this point, thereby releasing the SDO bus for other use.The state of SDI is shifted into the input register with every falling edge on SCLK. The state of SDO is shifted out of the output register at every rising edge on SCLK (Clock Phase = 1). The SPI protocol of the AWD89XXTSR is compatible with independent slave configuration and with daisy chain. Daisy chaining is applicable to SPI devices with the same protocol. Writing, clearing and reading is done byte wise. The SPI configuration and status bits are not cleared automatically by the device and therefore must be cleared by the microcontroller, e.g. if the TSD bit was set due to over temperature (refer to the respective register description for detailed information).



note: the reversed order of LSB and MSB as shown in this figure compared to the register description

Figure 7 SPI Data Transfer Timing

GLOBAL STATUS REGISTER

The SDO shifts out during the first eight SCLK cycles the Global Status Register. This register provides an overview of the device status. All failures conditions are reported in this byte:

- SPI protocol error (SPI_ERR)
- VM Undervoltage (UV bit)
- VM Overvoltage (OV bit)
- Negated Power ON Reset (NPOR bit)
- Temperature Pre-Warning (TPW bit)
- Temperature Shutdown (TSD bit)

SPI PROTOCOL ERROR DETECTION

The SPI incorporates an error flag in the Global Status Register (SPI_ERR, Bit7) to supervise and preserve the data integrity. If an SPI protocol error is detected during a given frame, the SPI_ERR bit is set in the next SPI communication.

The SPI_ERR bit is set in the following error conditions:

- the number of SCLK clock pulses received when nSCS is Low is not 0, or is not a multiple of 8 and at least 16.

INDEPENDENT SLAVE OPERATION

In an independent slave configuration, the microcontroller controls the nSCS of each slave individually.

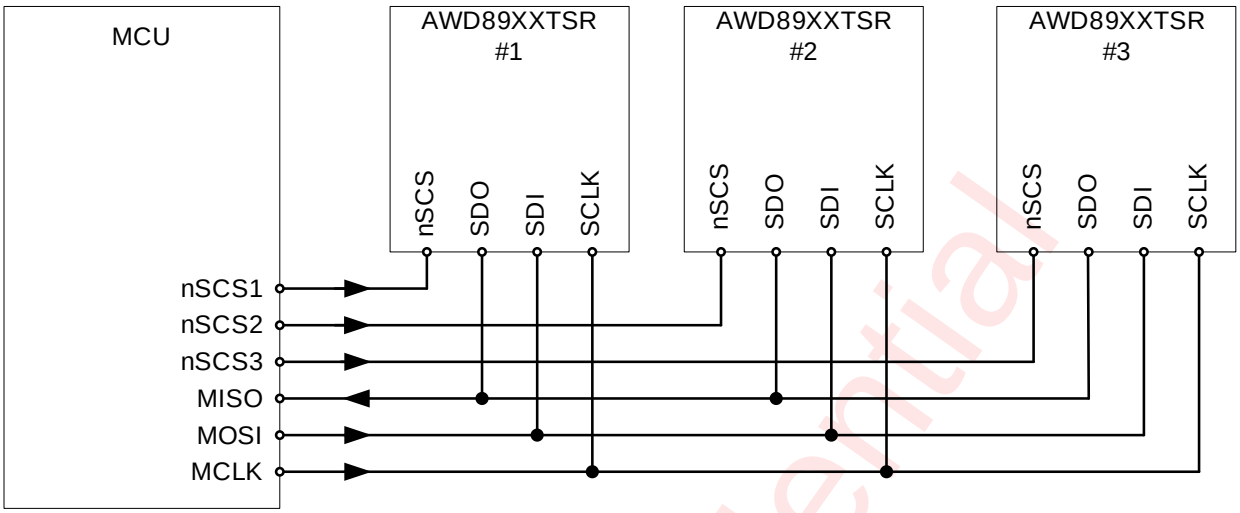


Figure 8 SPI with independent slave configuration

Each SPI communication starts with one address byte followed by one data byte (**Figure 8**).The LSB of the data byte must be set to '1'.The address bytes specifies:

- the type of operation: READ (OP bit =0) or WRITE (OP bit = 1) of the configuration bits.
- The target register address (A[6:2])

  The Last Address Byte Token bit (LABT, Bit1 of the address byte) must be set to 1.

While the microcontroller sends the address byte on SDI, SDO shifts out the Global Status Register.

A further data byte (Bit15...8) is allocated to either configure the half-bridges or retrieve status information of the AWD89xxTSR.

	LSB	Address Byte								Data Byte							**MSB**
	0	1	2	3	4	5	6	7		8	9	10	11	12	13	14	15
SDI	1	LABT = 1	A2	A3	A4	A5	A6	OP		D0	D1	D2	D3	D4	D5	D6	D7

Register content of the selected address

	LSB	Global Status Register								Data Byte (Response)							**MSB**
	0	1	2	3	4	5	6	7		8	9	10	11	12	13	14	15
SDO	0	TPW	TSD	NPOR	OV	UV	-	SPI_ ERR		D0	D1	D2	D3	D4	D5	D6	D7

LSB is sent first in SPI message — Time

Figure 9 SPI Operation Mode with independent slave configuration

Register Configuration

REGISTER LIST

Note: Reserved register should not be written default value

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	HB_ACT_1_CTRL	RW	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	0x00
0x01	HB_ACT_2_CTRL	RW	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	0x00
0x02	HB_ACT_3_CTRL	RW	HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN	0x00
0x03	HB_MODE_1_CTRL	RW	HB4_MODE		HB3_MODE		HB2_MODE		HB1_MODE		0x00
0x04	HB_MODE_2_CTRL	RW	HB8_MODE		HB7_MODE		HB6_MODE		HB5_MODE		0x00
0x05	HB_MODE_3_CTRL	RW	HB12_MODE		HB11_MODE		HB10_MODE		HB9_MODE		0x00
0x06	PWM_FREQ_CTRL	RW	FM_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		0x00
0x07	PWM1_DC_CTRL	RW	PWM1_DC								0x00
0x08	PWM2_DC_CTRL	RW	PWM2_DC								0x00
0x09	PWM3_DC_CTRL	RW	PWM3_DC								0x00
0x0A	FW_1_ CTRL	RW	FW_HB6	FW_HB5	FW_HB4	FW_HB3	FW_HB2	FW_HB1	Reserved		0x00
0x0B	FW_2_CTRL	RW	Reserved		FW_HB12	FW_HB11	FW_HB10	FW_HB9	FW_HB8	FW_HB7	0x00
0x0C	GLB_STAT	RC	SPI_ERR	Reserved	VM_UV	VM_OV	NPOR	TSD	TPW	Reserved	0x00
0x0D	OCP_STAT_1	RC	HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC	0x00
0x0E	OCP_STAT_2	RC	HB8_HS_OC	HB8_LS_OC	HB7_HS_OC	HB7_LS_OC	HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC	0x00
0x0F	OCP_STAT_3	RC	HB12_HS_OC	HB12_LS_OC	HB11_HS_OC	HB11_LS_OC	HB10_HS_OC	HB10_LS_OC	HB9_HS_OC	HB9_LS_OC	0x00
0x13	CONFIG_CTRL	RO	Reserved				CHIP_ID				0x0C
0x14	PWM_DZ_CTRL	RW	PWM_CH3_ ENH_FREQ	PWM_CH2_ ENH_FREQ	PWM_CH1_ ENH_FREQ	HB_DZ_TIME					0x0A
0x16	PWM_ENHSR_CTRL	RW	Reserved						HB_ENHSR	EXT_OVP	0x01

REGISTER DETAILED DESCRIPTION

CONTROL REGISTERS

The half-bridge output must be connected to a PWM generator, enabling HS or LS to be turned on during PWM high levels.

HB_ACT_1_CTRL: (Address 00h)

Bit	Symbol	R/W	Description	Default
7	HB4_HS_EN	RW	Half-bridge 4 high side switch enable 0: HS4 OFF / High Z 1: HS4 Enable	0
6	HB4_LS_EN	RW	Half-bridge 4 low side switch enable 0: LS4 OFF / High Z 1: LS4 Enable	0
5	HB3_HS_EN	RW	Half-bridge 3 high side switch enable 0: HS3 OFF / High Z 1: HS3 Enable	0
4	HB3_LS_EN	RW	Half-bridge 3 low side switch enable 0: LS3 OFF / High Z 1: LS3 Enable	0
3	HB2_HS_EN	RW	Half-bridge 2 high side switch enable 0: HS2 OFF / High Z 1: HS2 Enable	0
2	HB2_LS_EN	RW	Half-bridge 2 low side switch enable 0: LS2 OFF / High Z 1: LS2 Enable	0
1	HB1_HS_EN	RW	Half-bridge 1 high side switch enable 0: HS1 OFF / High Z 1: HS1 Enable	0
0	HB1_LS_EN	RW	Half-bridge 1 low side switch enable 0: LS1 OFF / High Z 1: LS1 Enable	0

HB_ACT_2_CTRL: (Address 01h)

Bit	Symbol	R/W	Description	Default
7	HB8_HS_EN	RW	Half-bridge 8 high side switch enable 0: HS8 OFF / High Z 1: HS8 Enable	0
6	HB8_LS_EN	RW	Half-bridge 8 low side switch enable 0: LS8 OFF / High Z 1: LS8 Enable	0
5	HB7_HS_EN	RW	Half-bridge 7 high side switch enable 0: HS7 OFF / High Z 1: HS7 Enable	0
4	HB7_LS_EN	RW	Half-bridge 7 low side switch enable 0: LS7 OFF / High Z 1: LS7 Enable	0
3	HB6_HS_EN	RW	Half-bridge 6 high side switch enable 0: HS6 OFF / High Z 1: HS6 Enable	0
2	HB6_LS_EN	RW	Half-bridge 6 low side switch enable 0: LS2 OFF / High Z 1: LS2 Enable	0
1	HB5_HS_EN	RW	Half-bridge 5 high side switch enable 0: HS1 OFF / High Z 1: HS1 Enable	0
0	HB5_LS_EN	RW	Half-bridge 5 low side switch enable 0: LS1 OFF / High Z 1: LS1 Enable	0

Register Detailed Description(Continue)

HB_ACT_3_CTRL: (Address 02h)

Bit	Symbol	R/W	Description	Default
7	HB12_HS_EN	RW	Half-bridge 12 high side switch enable 0: HS12 OFF / High Z 1: HS12 Enable	0
6	HB12_LS_EN	RW	Half-bridge 8 low side switch enable 0: LS12 OFF / High Z 1: LS12 Enable	0
5	HB11_HS_EN	RW	Half-bridge 11 high side switch enable 0: HS11 OFF / High Z 1: HS11 Enable	0
4	HB11_LS_EN	RW	Half-bridge 11 low side switch enable 0: LS11 OFF / High Z 1: LS11 Enable	0
3	HB10_HS_EN	RW	Half-bridge 10 high side switch enable 0: HS10 OFF / High Z 1: HS10 Enable	0
2	HB10_LS_EN	RW	Half-bridge 10 low side switch enable 0: LS10 OFF / High Z 1: LS10 Enable	0
1	HB9_HS_EN	RW	Half-bridge 9 high side switch enable 0: HS9 OFF / High Z 1: HS9 Enable	0
0	HB9_LS_EN	RW	Half-bridge 5 low side switch enable 0: LS9 OFF / High Z 1: LS9 Enable	0

HB_MODE_1_CTRL: (Address 03h)

Bit	Symbol	R/W	Description	Default
7:6	HB4_MODE	RW	Half-bridge 4 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
5:4	HB3_MODE	RW	Half-bridge 3 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
3:2	HB2_MODE	RW	Half-bridge 2 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
1:0	HB1_MODE	RW	Half-bridge 1 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0

Register Detailed Description(Continue)

HB_MODE_2_CTRL: (Address 04h)

Bit	Symbol	R/W	Description	Default
7:6	HB8_MODE	RW	Half-bridge 8 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
5:4	HB7_MODE	RW	Half-bridge 7 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
3:2	HB6_MODE	RW	Half-bridge 6 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
1:0	HB5_MODE	RW	Half-bridge 5 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0

HB_MODE_3_CTRL: (Address 05h)

Bit	Symbol	R/W	Description	Default
7:6	HB12_MODE	RW	Half-bridge 12 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
5:4	HB11_MODE	RW	Half-bridge 11 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
3:2	HB10_MODE	RW	Half-bridge 10 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0
1:0	HB9_MODE	RW	Half-bridge 11 mode select 00: No PWM 01: PWM control with PWM Channel 1 10: PWM control with PMW Channel 2 11: PWM control with PWM Channel 3	0

Register Detailed Description(Continue)

PWM_FREQ_CTRL: (Address 06h)

Bit	Symbol	R/W	Description	Default
7:6	FM_FREQ	RW	PWM CLK frequency select 00: 6MHz 01: 3MHz 10: 2MHz 11: 1MHz	0
5:4	PWM_CH3_FREQ	RW	PWM Channel 3 frequency select 00: PWM3 is stopped and off 01: PWM3 frequency: 80Hz 10: PWM3 frequency: 100Hz 11: PWM3 frequency: 200Hz	0
3:2	PWM_CH2_FREQ	RW	PWM Channel 2 frequency select 00: PWM2 is stopped and off 01: PWM2 frequency: 80Hz 10: PWM2 frequency: 100Hz 11: PWM2 frequency: 200Hz	0
1:0	PWM_CH1_FREQ	RW	PWM Channel 1 frequency select 00: PWM1 is stopped and off 01: PWM1 frequency: 80Hz 10: PWM1 frequency: 100Hz 11: PWM1 frequency: 200Hz	0

PWM1_DC_CTRL: (Address 07h)

Bit	Symbol	R/W	Description	Default
7:0	PWM_CH1_DC	RW	PWM Channel 1 Duty Cycle configuration 0000 0000: 100% OFF xxxx xxxx: parts of 255 ON 1111 1111: 100% ON	0

PWM2_DC_CTRL: (Address 08h)

Bit	Symbol	RW	Description	Default
7:0	PWM_CH2_DC	RW	PWM Channel 1 Duty Cycle configuration 0000 0000: 100% OFF xxxx xxxx: parts of 255 ON 1111 1111: 100% ON	0

PWM3_DC_CTRL: (Address 09h)

Bit	Symbol	R/W	Description	Default
7:0	PWM_CH3_DC	RW	PWM Channel 1 Duty Cycle configuration 0000 0000: 100% OFF xxxx xxxx: parts of 255 ON 1111 1111: 100% ON	0

Register Detailed Description(Continue)

FW_1_CTRL: (Address 0Ah)

Bit	Symbol	R/W	Description	Default
7	FW_HB6	RW	HB6 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
6	FW_HB5	RW	HB5 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
5	FW_HB4	RW	HB4 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
4	FW_HB3	RW	HB3 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
3	FW_HB2	RW	HB2 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
2	FW_HB1	RW	HB1 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
1	-	RW	Reserved	0
0	-	RW	Reserved	0

FW_2_CTRL: (Address 0Bh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	
5	FW_HB12	RW	HB6 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
4	FW_HB11	RW	HB5 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
3	FW_HB10	RW	HB4 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
2	FW_HB9	RW	HB3 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
1	FW_HB8	RW	HB2 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0
0	FW_HB7	RW	HB1 free-wheeling configuration 0: Passive free-wheeling 1: Active free-wheeling	0

STATUS REGISTERS

GLB_STAT: (Address 0Ch)

Bit	Symbol	R/W	Description	Default
7	SPI_ERR	RC	SPI error detection 0: No SPI protocol error is detected 1: An SPI protocol error is detected	0
6	Reserved	RO	Not used	0
5	VM_UV	RC	VM undervoltage error detection 0: No undervoltage on V_M detected 1: Undervoltage on V_M detected. Error latched and all outputs disabled	0
4	VM_OV	RC	VM overvoltage error detection 0: No overvoltage on Vs detected 1: Overvoltage on Vs detected. Error latched and all outputs disabled	0
3	NPOR	RC	Not Power On Reset (NPOR) detection 0: POR on EN Or VDD supply rail 1: No POR	0
2	TSD	RC	Temperature shutdown error detection 0: Junction temperature below temperature shutdown threshold 1: Junction temperature has reached temperature shutdown threshold. Error latched and all outputs disabled	0
1	TPW	RC	Temperature pre-warning error detection 0: Junction temperature below temperature pre-warning threshold 1: Junction temperature has reached temperature pre-warning threshold.	0
0	Reserved	RO	Not used	0

OCP_STAT_1: (Address 0Dh)

Bit	Symbol	R/W	Description	Default
7	HB4_HS_OC	RC	High-side (HS) switch of half-bridge 4 overcurrent detection 0: No error on HS4 switch 1: Overcurrent detected on HS4 switch. Error latched and HS4 OFF.	0
6	HB4_LS_ OC	RC	Low-side (LS) switch of half-bridge 4 overcurrent detection 0: No error on LS4 switch 1: Overcurrent detected on LS4 switch. Error latched and LS4 OFF.	0
5	HB3_HS_OC	RC	High-side (HS) switch of half-bridge 3 overcurrent detection 0: No error on HS3 switch 1: Overcurrent detected on HS3 switch. Error latched and HS3 OFF.	0
4	HB3_LS_ OC	RC	Low-side (LS) switch of half-bridge 3 overcurrent detection 0: No error on LS3 switch 1: Overcurrent detected on LS3 switch. Error latched and LS3 OFF.	0
3	HB2_HS_OC	RC	High-side (HS) switch of half-bridge 2 overcurrent detection 0: No error on HS2 switch 1: Overcurrent detected on HS2 switch. Error latched and HS2 OFF.	0
2	HB2_LS_ OC	RC	Low-side (LS) switch of half-bridge 2 overcurrent detection 0: No error on LS2 switch 1: Overcurrent detected on LS2 switch. Error latched and LS2 OFF.	0
1	HB1_HS_OC	RC	High-side (HS) switch of half-bridge 1 overcurrent detection 0: No error on HS1 switch 1: Overcurrent detected on HS1 switch. Error latched and HS1 OFF.	0
0	HB1_LS_ OC	RC	Low-side (LS) switch of half-bridge 1 overcurrent detection 0: No error on LS1 switch 1: Overcurrent detected on LS1 switch. Error latched and LS1 OFF.	0

Register Detailed Description(Continue)

OCP_STAT_2: (Address 0Eh)

Bit	Symbol	R/W	Description	Default
7	HB8_HS_OC	RC	High-side (HS) switch of half-bridge 8 overcurrent detection 0: No error on HS8 switch 1: Overcurrent detected on HS8 switch. Error latched and HS8 OFF.	0
6	HB8_LS_ OC	RC	Low-side (LS) switch of half-bridge 8 overcurrent detection 0: No error on LS8 switch 1: Overcurrent detected on LS8 switch. Error latched and LS8 OFF.	0
5	HB7_HS_OC	RC	High-side (HS) switch of half-bridge 7 overcurrent detection 0: No error on HS7 switch 1: Overcurrent detected on HS7 switch. Error latched and HS7 OFF.	0
4	HB7_LS_ OC	RC	Low-side (LS) switch of half-bridge 7 overcurrent detection 0: No error on LS7 switch 1: Overcurrent detected on LS7 switch. Error latched and LS7 OFF.	0
3	HB6_HS_OC	RC	High-side (HS) switch of half-bridge 6 overcurrent detection 0: No error on HS6 switch 1: Overcurrent detected on HS6 switch. Error latched and HS6 OFF.	0
2	HB6_LS_ OC	RC	Low-side (LS) switch of half-bridge 6 overcurrent detection 0: No error on LS6 switch 1: Overcurrent detected on LS6 switch. Error latched and LS6 OFF.	0
1	HB5_HS_OC	RC	High-side (HS) switch of half-bridge 5 overcurrent detection 0: No error on HS5 switch 1: Overcurrent detected on HS5 switch. Error latched and HS5 OFF.	0
0	HB5_LS_ OC	RC	Low-side (LS) switch of half-bridge 5 overcurrent detection 0: No error on LS5 switch 1: Overcurrent detected on LS5 switch. Error latched and LS5 OFF.	0

OCP_STAT_3: (Address 0Fh)

Bit	Symbol	R/W	Description	Default
7	HB12_HS_OC	RC	High-side (HS) switch of half-bridge 12 overcurrent detection 0: No error on HS12 switch 1: Overcurrent detected on HS12 switch. Error latched and HS12 OFF.	0
6	HB12_LS_ OC	RC	Low-side (LS) switch of half-bridge 12 overcurrent detection 0: No error on LS12 switch 1: Overcurrent detected on LS12 switch. Error latched and LS12 OFF.	0
5	HB11_HS_OC	RC	High-side (HS) switch of half-bridge 11 overcurrent detection 0: No error on HS11 switch 1: Overcurrent detected on HS11 switch. Error latched and HS11 OFF.	0
4	HB11_LS_ OC	RC	Low-side (LS) switch of half-bridge 11 overcurrent detection 0: No error on LS11 switch 1: Overcurrent detected on LS11 switch. Error latched and LS11 OFF.	0
3	HB10_HS_OC	RC	High-side (HS) switch of half-bridge 10 overcurrent detection 0: No error on HS10 switch 1: Overcurrent detected on HS10 switch. Error latched and HS10 OFF.	0
2	HB10_LS_ OC	RC	Low-side (LS) switch of half-bridge 10 overcurrent detection 0: No error on LS10 switch 1: Overcurrent detected on LS10 switch. Error latched and LS10 OFF.	0
1	HB9_HS_OC	RC	High-side (HS) switch of half-bridge 9 overcurrent detection 0: No error on HS9 switch 1: Overcurrent detected on HS9 switch. Error latched and HS9 OFF.	0
0	HB9_LS_ OC	RC	Low-side (LS) switch of half-bridge 9 overcurrent detection 0: No error on LS9 switch 1: Overcurrent detected on LS9 switch. Error latched and LS9 OFF.	0

Register Detailed Description(Continue)

CONFIG_CTRL: (Address 13h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0
3:0	CHIP_ID	RO	CHIP_ID 1100: AWD8912TSR 1010: AWD8910TSR 1000: AWD8908TSR 0110: AWD8906TSR	-

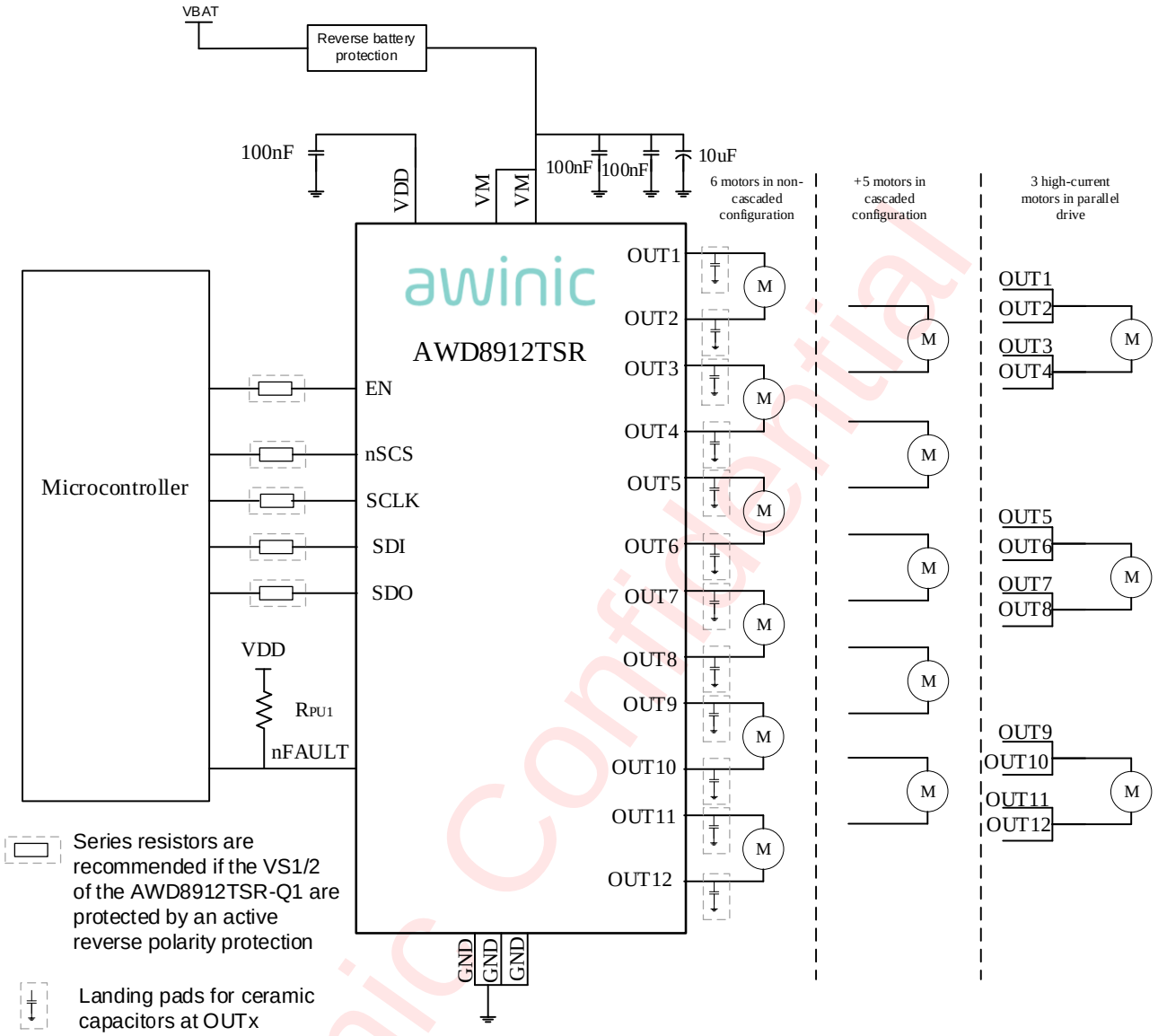
PWM_DZ_ CTRL: (Address 14h)

Bit	Symbol	R/W	Description	Default
7	PWM_CH3_ENH_FREQ	RW	PWM Chanel3 enhance frequency select: 0: Don't use enhance function ; 1: Open enhance funtion with PWM_CH3_FREQ register 0xx: PWM3 frequency: 0Hz~200Hz 100: PWM3 frequency: 0Hz 101: PWM3 frequency: 400Hz 110: PWM3 frequency: 800Hz 111: PWM3 frequency: 2000Hz	0
6	PWM_CH2_ENH_FREQ	RW	PWM Chanel2 enhance frequency select: 0: Don't use enhance function ; 1: Open enhance funtion with PWM_CH2_FREQ register 0xx: PWM2 frequency: 0Hz~200Hz 100: PWM2 frequency: 0Hz 101: PWM2 frequency: 400Hz 110: PWM2 frequency: 800Hz 111: PWM2 frequency: 2000Hz	0
5	PWM_CH1_ENH_FREQ	RW	PWM Chanel3 enhance frequency select: 0: Don't use enhance function ; 1: Open enhance funtion with PWM_CH1_FREQ register 0xx: PWM1 frequency: 0Hz~200Hz 100: PWM1 frequency: 0Hz 101: PWM1 frequency: 400Hz 110: PWM1 frequency: 800Hz 111: PWM1 frequency: 2000Hz	0
4:0	HB_DZ_TIME	RW	PWM dead time control HB_ENHSR=1(Fast), (2.5*HB_DZ_TIME)us HB_ENHSR=0(Normal), (4*2.5*HB_DZ_TIME)us	0x0A

PWM_PHASE: (Address 16h)

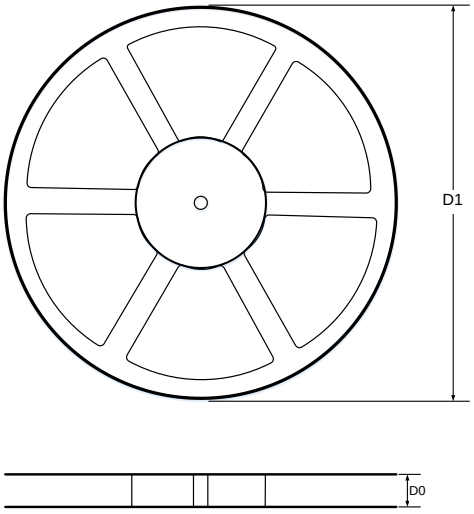
Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1	HB_ENHSR	RW	12 Channel SR enhance 0: 0.45V/us 1: 2.5V/us	0
0	EXT_OVP	RW	OVP voltage select 0: OVP voltage 22V 1: OVP voltage 34.5V	1

Application information

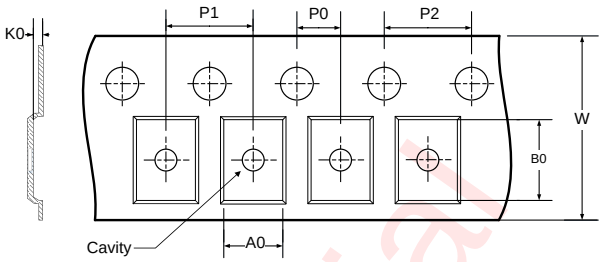


TAPE AND REEL INFORMATION

REEL DIMENSIONS

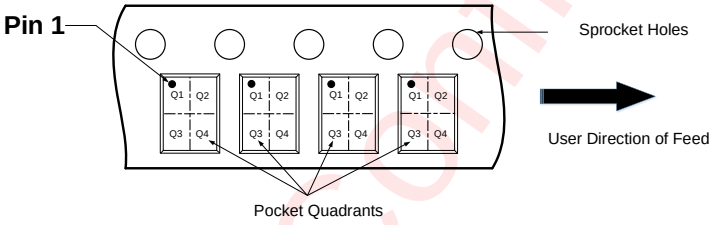


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



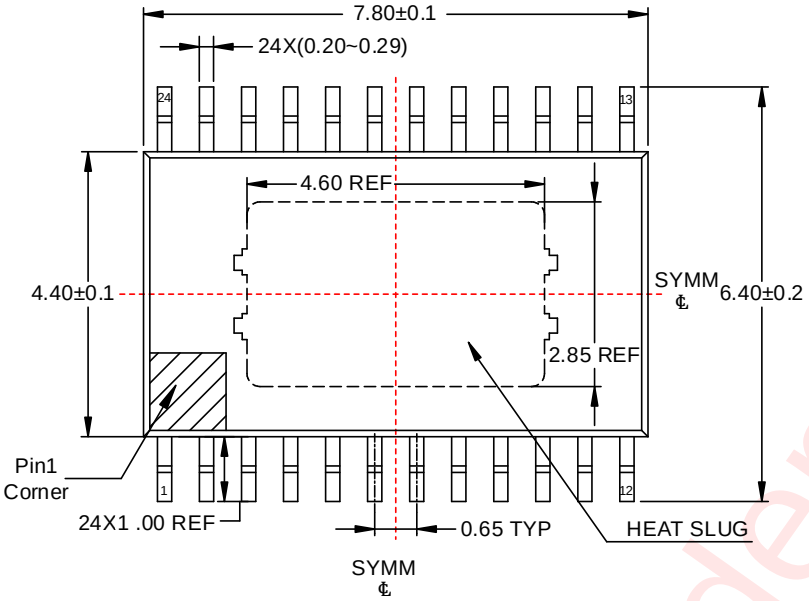
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

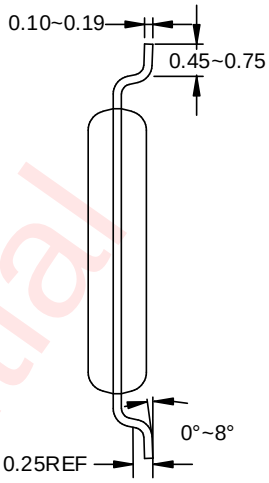
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	16.4	6.95	8.3	1.6	2	8	4	16	Q1

All dimensions are nominal

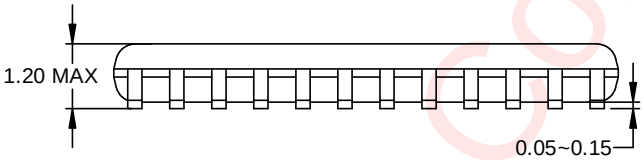
PACKAGE DESCRIPTION



Top View



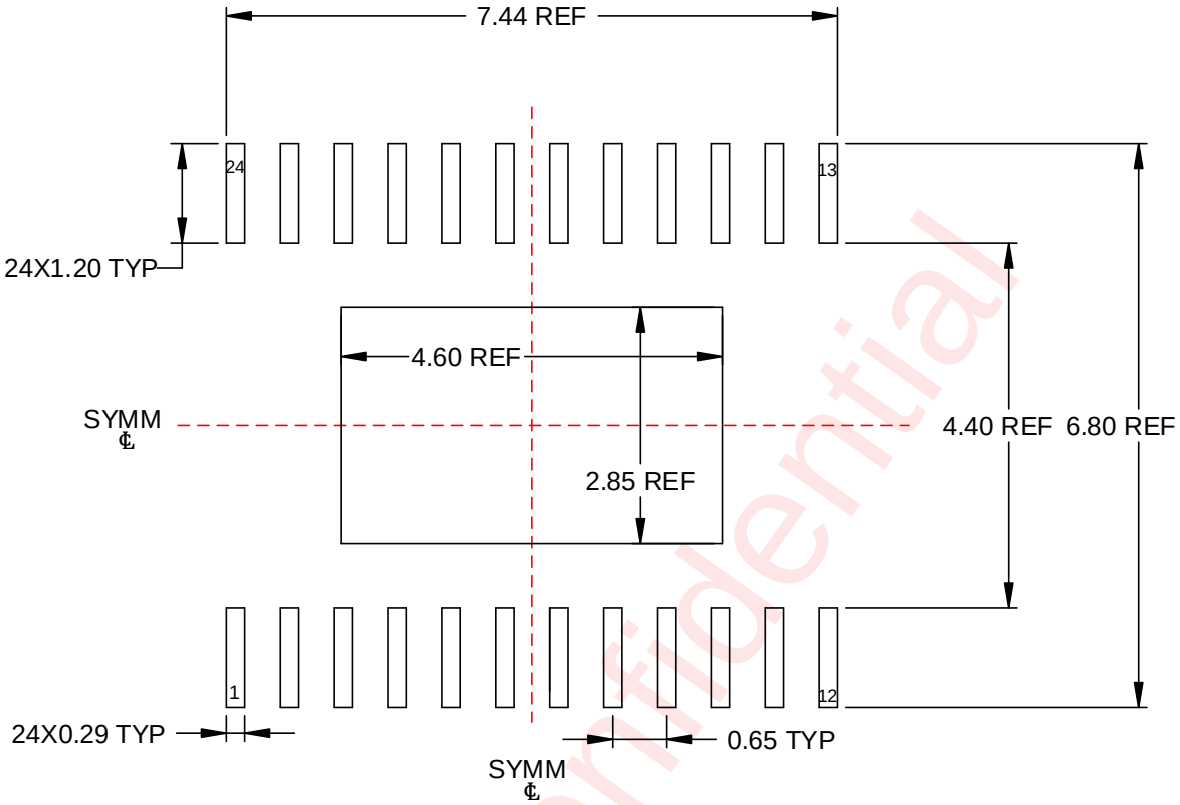
Side View

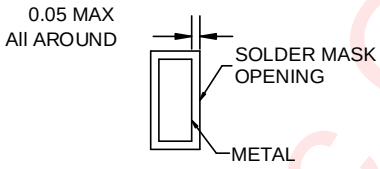


Side View

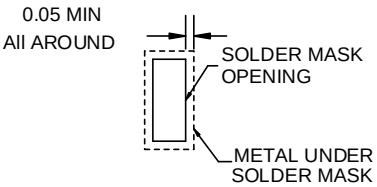
Unit:mm

LAND PATTERN DATA





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Aug. 2023	officially released

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