Over-Voltage Protection Load Switch with Surge Protection

Features

- Highly reliable FCQFN 1.3mm×1.8mm-12L package
- Surge protection
  - IEC 61000-4-5: 100V
- Integrated low R_{dson} nFET switch: typical 33mΩ
- 5A continuous current capability
- Default Over-Voltage Protection threshold
  - AW3291XA: 6.8V
- OVP threshold adjustable range: 4V to 24V
- Input system ESD protection
  - IEC 61000-4-2 Contact discharge: ±8kV
  - IEC 61000-4-2 Air gap discharge: ±15kV
- Input voltage: $28V_{DC}$
- Fast turn-off response: typical 70ns
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)

Applications

- Smartphones
- Tablets
- Charging Ports

General Description

AW3291XA family OVP load switch features surge protection, an internal clamp circuit protects the device from surge voltages up to 100V.

AW3291XA features an ultra-low 33mΩ (typ.) R_{dson} nFET load switch. When input voltage exceeds the OVP threshold, the switch is turned off very fast to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages up to $28V_{DC}$.

The default OVP threshold is 6.8V (AW3291XA), the OVP threshold can be adjusted from 4V to 24V through external OVLO pin.

The device features an open-drain output ACOKB, when $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$ and the switch is on, ACOKB will be driven low to indicate a good power input, otherwise it is high impedance.

This device features over-temperature protection that prevents itself from thermal damaging.

Typical Application Circuit

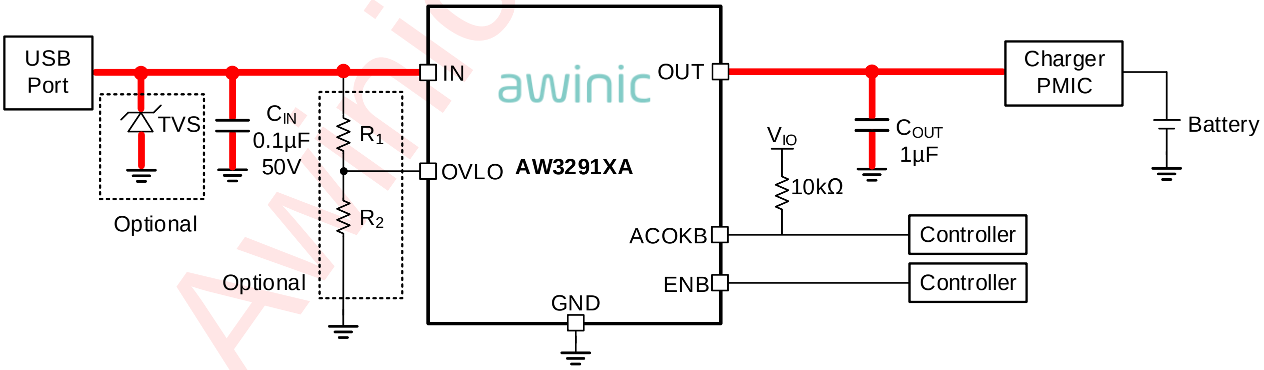

Figure 1 AW3291XA Typical Application Circuit

R_1 and R_2 are used for OVP threshold adjustment, to use default OVP threshold, connect OVLO to ground.

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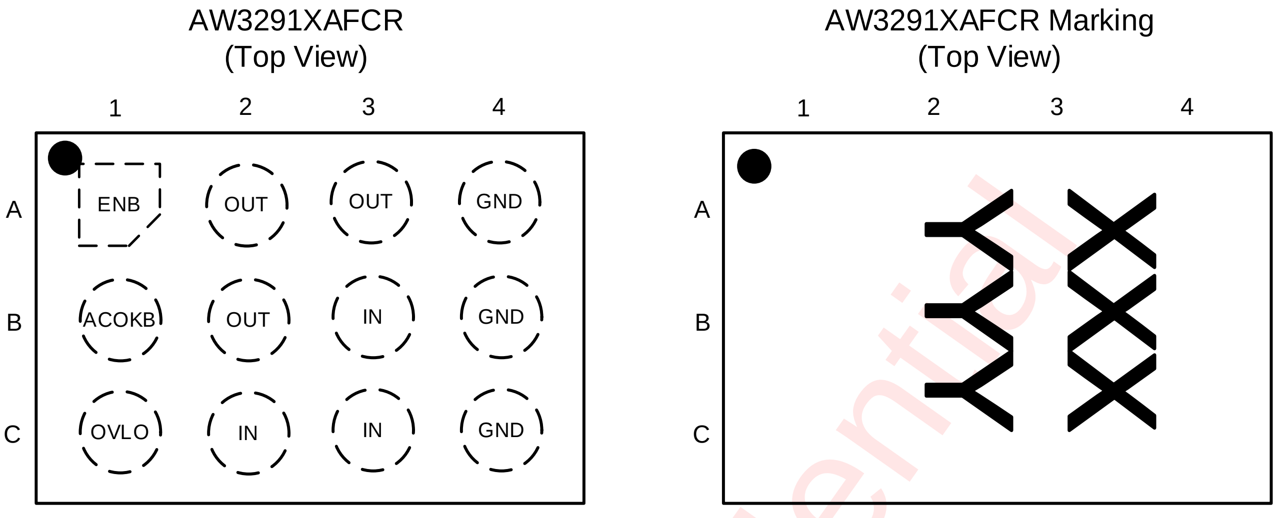
Pin Configuration and Top Mark



XXX - Marking
YYY - Production tracing code

Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
A1	ENB	Enable pin, active low
B1	ACOKB	Power good flag, active-low, open-drain output. When V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}, ACOKB is pulled low, otherwise it's hi-Z state
C1	OVLO	OVP threshold adjustment pin
C2, C3, B3	IN	Switch input and device power supply
A2, A3, B2	OUT	Switch output
A4, B4, C4	GND	Device ground

Functional Block Diagram

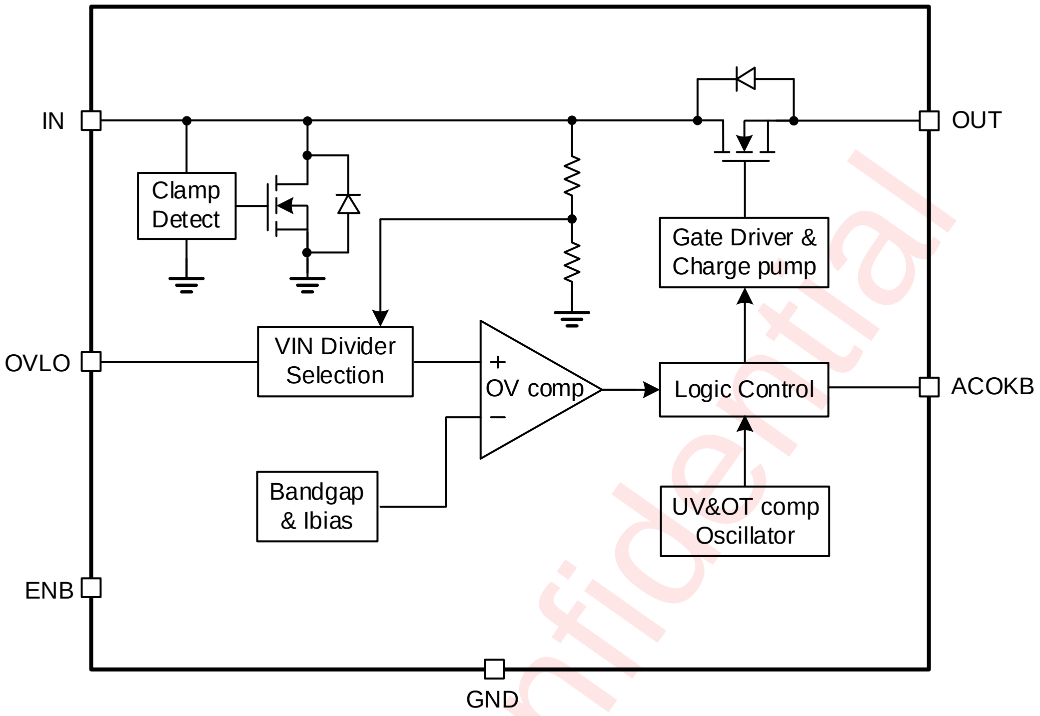


Figure 3 Functional Block Diagram

Typical Application Circuits

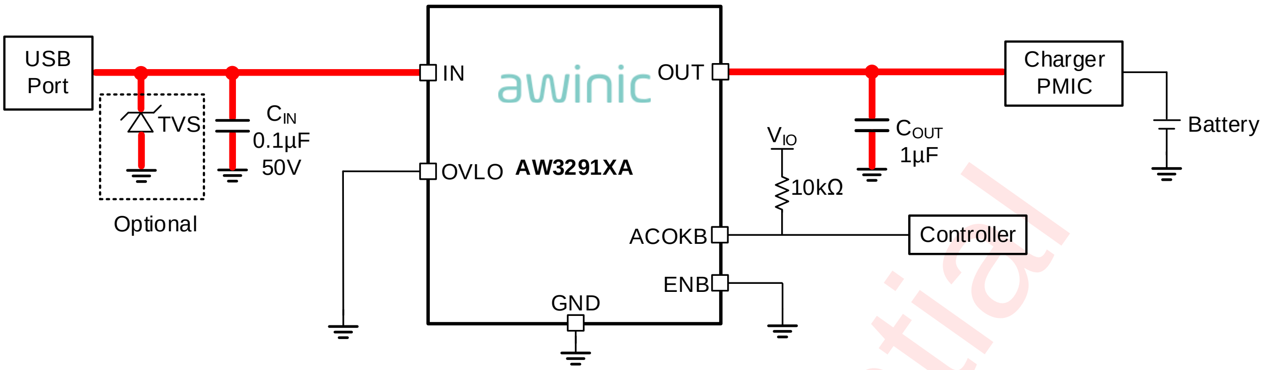


Figure 4 AW3291XA Typical Application Circuit(Using Default OVP Threshold)

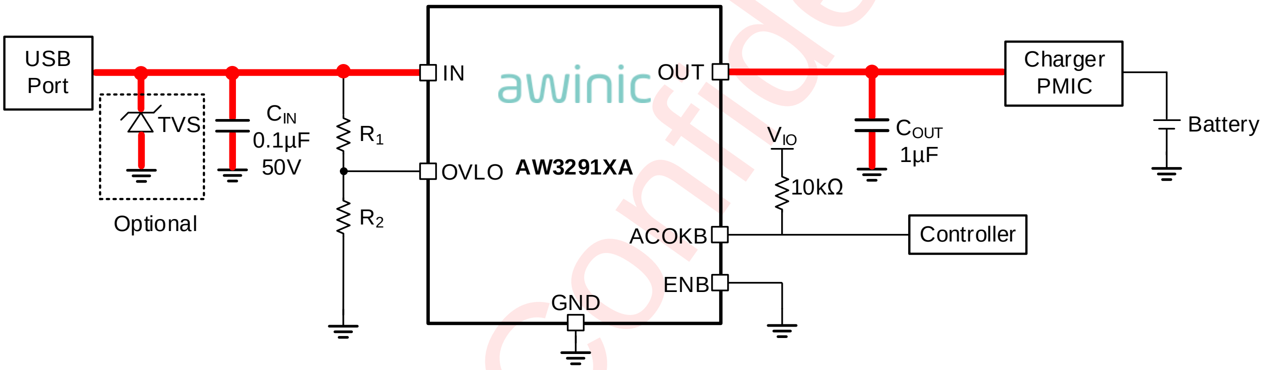


Figure 5 AW3291XA Typical Application Circuit(Using External Resistors Set OVP Threshold)

Notice for Typical Application Circuits:

1. If VBUS is required to pass surge voltage greater than 100V, external TVS is needed, the maximum clamping voltage of the TVS should be below 32V.
2. When the default OVP threshold is used, connect OVLO pin to GND directly or through a 0Ω resistor. **OVLO pin cannot be left floating.**
3. If R_1 and R_2 are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision.
4. If ACOKB is not used, it can be left floating, or short to GND.
5. C_{IN} = 0.1µF is recommended for typical application, larger C_{IN} is also acceptable. The rated voltage of C_{IN} should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW3291XA is used, the rated voltage of C_{IN} should be 50V.
6. C_{OUT} = 1µF is recommended for typical application, larger C_{OUT} is also acceptable. The rated voltage of C_{OUT} should be larger than the OVP threshold. For example, if the OVP threshold is 6.8V, the rated voltage of C_{OUT} should be 10V or higher.

Ordering Information

Part Number	**Temperature**	**Package**	**Marking**	**Moisture Sensitivity Level**	**Environmental Information**	**Delivery Form**
AW32915AFCR	-40°C ~ 85°C	FCQFN 1.3mm×1.8mm -12L	RZR	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE 1)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IN}	Input voltage		-0.3	28	V
V_{OUT}	Output voltage		-0.3	See(NOTE 2)	V
V_{OVLO}	OVLO voltage		-0.3	6	V
V_{ACOKB}	ACOKB voltage		-0.3	6	V
V_{ENB}	ENB voltage		-0.3	6	V
I_{SW}	Continuous current of switch IN-OUT(NOTE 3)	Continuous current on IN and OUT pin		5	A
I_{PEAK}	Peak current	Peak input and output current on IN and OUT pin(10ms)		8	A
I_{DIODE}	Continuous diode current	Continuous forward current through the nFET body diode		1.5	A
T_A	Ambient temperature		-40	85	°C
T_J	Junction temperature		-40	150	°C
T_{STG}	Storage temperature		-65	150	°C
T_{LEAD}	Soldering temperature	At leads, 10 seconds		260	°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: 28V or V_{IN}+0.3V, whichever is smaller.

NOTE3: Limited by thermal design.

Thermal Information

Symbol	Parameter	Condition	Value	Unit
$R_{\theta JA}$	Thermal resistance from junction to ambient (NOTE 1)	In free air	65	°C/W

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

ESD and Latch-up Ratings

Symbol	Parameter	Condition	Value	Unit
V_{ESD}	IEC61000-4-2 system ESD on IN pin with 0.1μF C_{IN}	Contact discharge	±8	kV
		Air gap discharge	±15	kV
	Human Body Model	ESDA/JEDEC JS-001-2017	±2	kV
	Charged Device Model	ESDA/JEDEC JS-002-2018	±1.5	kV
$I_{Latch-up}$	Latch-up	JESD78E	±200	mA

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input DC voltage	2.8		27	V
C_{IN}	Input capacitance		0.1		μF
C_{OUT}	Output load capacitance		1	100	μF

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 0.1μF, I_{IN}≤ 5A and T_A = 25℃.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{IN_CLAMP}	Input clamp voltage	I_{IN} = 10mA		32.2		V
R_{dson}	Switch on resistance	V_{IN} = 5V, I_{OUT} = 1A, T_A = 25°C		33		mΩ
I_Q	Input quiescent current	V_{IN} = 5V, V_{OVLO}=0V,I_{OUT} = 0A		65	130	μA
I_{IN_OVLO}	Input current at over-voltage condition	V_{IN} = 5V, V_{OVLO}=3V,V_{OUT} = 0V		65	130	μA
V_{OVLO_TH}	OVLO set threshold		1.16	1.20	1.24	V
V_{OVLO_RNG}	OVLO threshold adjustable range		4		24	V
V_{OVLO_SEL}	External OVLO select threshold	OVLO rising	0.14	0.20	0.26	V
		Hysteresis		0.04		V
I_{OVLO}	OVLO pin leakage current	V_{OVLO}=V_{OVLO_TH}	-0.2		0.2	μA
Protection						
V_{IN_OVLO}	OVP trip level	V_{IN} rising	6.66	6.80	6.94	V
		Hysteresis		0.14		
V_{IN_UVLO}	UVLO trip level	V_{IN} rising		2.65	2.8	V
		Hysteresis		0.1		
T_{SDN}	Shutdown temperature			150		°C
T_{SDN_HYS}	Shutdown temperature hysteresis			20		°C

Electrical Characteristics (Continued)

T_A = -40°C to 85°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 0.1μF, $I_{IN} \leq$ 5A and T_A = 25℃.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
Digital Logical Interface						
V_{OL}	ACOKB output low voltage	I_{SINK} =1mA			0.4	V
I_{LEAK_ACOKB}	ACOKB leakage current	V_{IO} =5V, ACOKB de-asserted	-0.5		0.5	μA
V_{IH}	ENB input high voltage		1.2			V
V_{IL}	ENB input low voltage				0.5	V
I_{LEAK_ENB}	ENB leakage current	V_{ENB} =5V	0		2	μA
Timing Characteristics (Figure 6)						
t_{DEB}	Debounce time	From V_{IN} > V_{IN_UVLO} to 10% V_{OUT}		12		ms
t_{START}	Start-up time	From V_{IN} > V_{IN_UVLO} to ACOKB low		24		ms
t_{ON}	Switch turn-on time	R_L = 100Ω, C_L = 22μF, V_{OUT} from 10% V_{IN} to 90% V_{IN}		0.6		ms
t_{OFF}	Switch turn-off time	C_L = 0μF, R_L = 100Ω, V_{IN} > V_{IN_OVLO} to V_{OUT} stop rising, V_{IN} rise at 10V/μs		70		ns

Timing Diagram

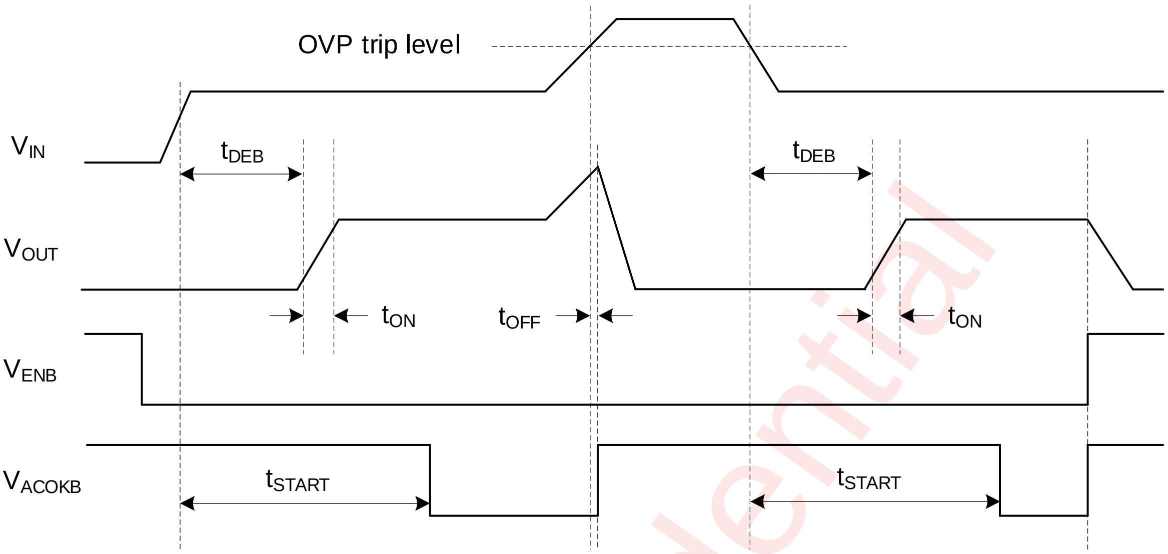


Figure 6 Timing Diagram

Typical Characteristics

V_{IN} = 5V, V_{ENB} = 0V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25°C unless otherwise specified.

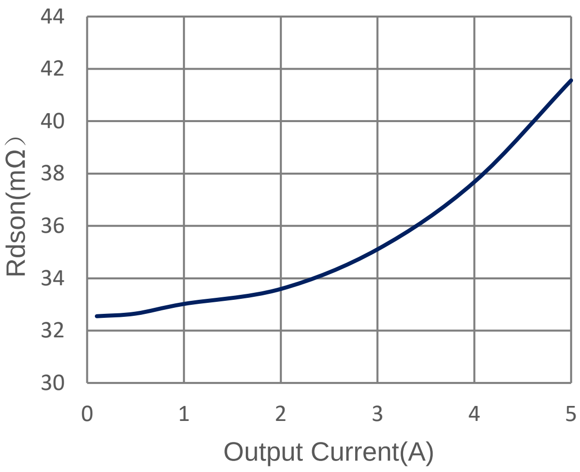


Figure 7 R_{dson} vs. Output Current

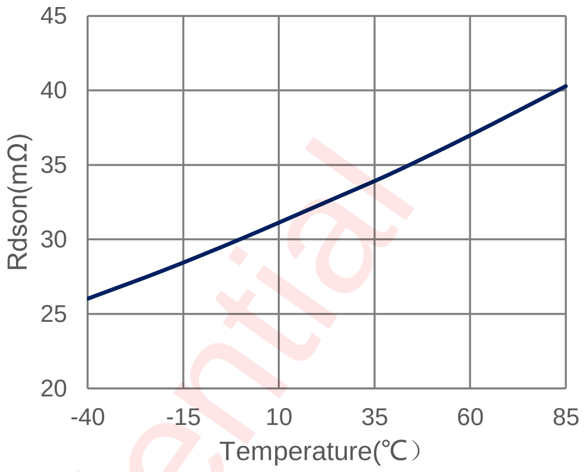


Figure 8 R_{dson} vs. Temp. (I_{OUT} = 1A)

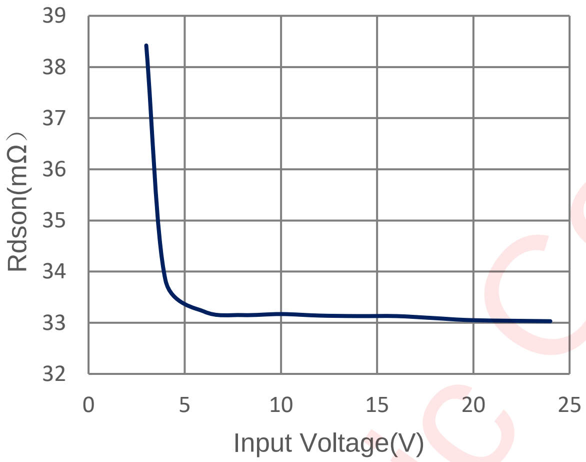


Figure 9 R_{dson} vs. Input Voltage (I_{OUT} =1A)

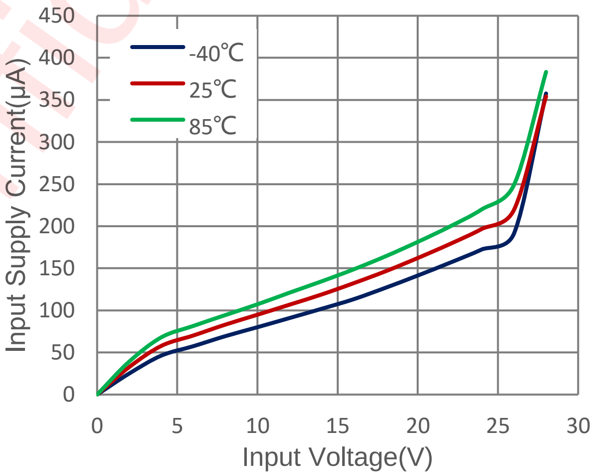


Figure 10 Input Supply Current vs. Supply Voltage

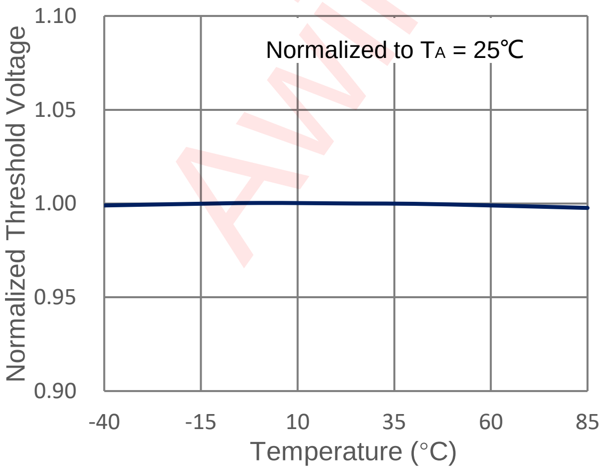


Figure 11 Normalized Internal OVP Threshold vs. Temp.

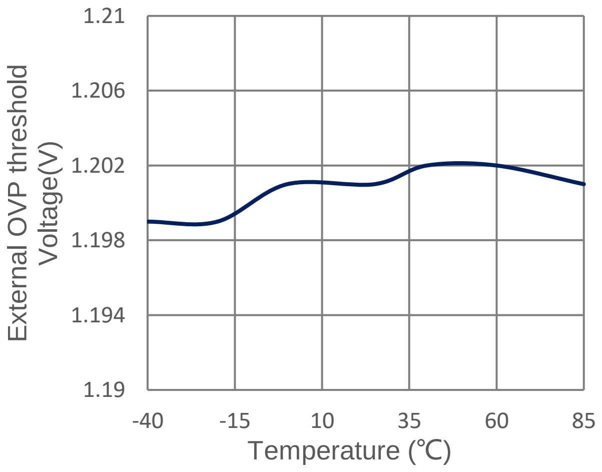
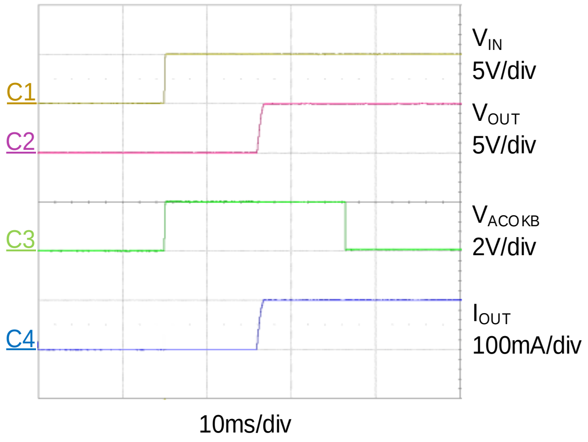


Figure 12 OVLO Set Threshold vs. Temp.

Typical Characteristics (Continued)

V_{IN} = 5V, V_{ENB} = 0V, V_{OVLO} = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, and T_A = 25°C unless otherwise specified.



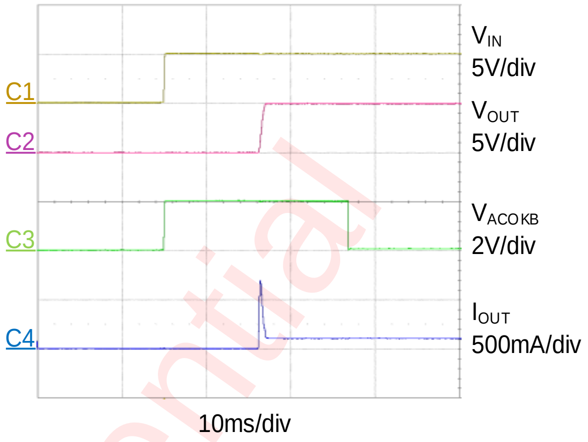


Figure 13 Power-up (C_{OUT} = 1μF, 100mA load)

Figure 14 Power-up (C_{OUT} = 100μF, 100mA load)

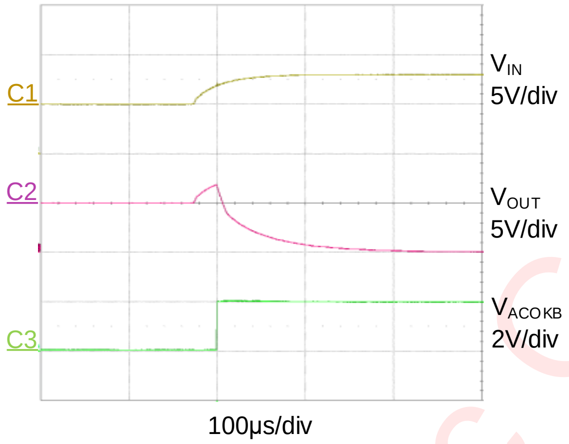


Figure 15 OVP Response

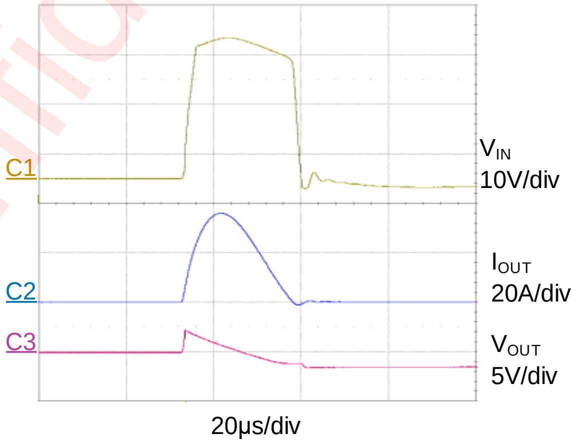


Figure 16 110V Surge Response(R_L=50Ω)

Functional Description

Device Operation

If the AW3291XA is enabled and the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on. ACOKB will be driven low about 24ms after V_{IN} valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 70ns. If ENB is pulled high, or input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

Surge Protection

The AW3291XA integrates a clamp circuit to suppress input surge voltage. For surge voltages between V_{IN_OVLO} and V_{IN_CLAMP}, the switch will be turned off but the clamp circuit will not work. For surge voltages greater than V_{IN_CLAMP}, the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 70ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

OVP Threshold Adjustment

If the default OVP threshold is used, OVLO pin must be grounded. If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

For example, if we select R_1 = 1MΩ and R_2 = 100kΩ, then the new OVP threshold calculated from the above formula is 13.2V. The OVP threshold adjustment range is from 4V to 24V. When the OVLO pin voltage V_{OVLO} exceeds V_{OVLO_SEL} (0.2V typical), V_{OVLO} is compared with the reference voltage V_{OVLO_TH} (1.2V typical) to judge whether input supply is over-voltage.

ACOKB Output

The device features an open-drain output ACOKB, it should be connected to the system I/O rail through a pull-up resistor. If the device is enabled and $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$, ACOKB will be driven low indicating the switch is on with a good power input. If OVP, UVLO, or OT occurs, or ENB is pulled high, the switch will be turned off and ACOKB will be pulled high.

USB On-The-Go (OTG) Operation

If V_{IN} = 0V and OUT is supplied by OTG voltage, the body diode of the load switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When $V_{IN} > V_{IN\_UVLO}$, internal charge pump begins to open the load switch after debounce time (about 12ms). After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum.

PCB Layout Consideration

To make fully use of the performance of AW3291XA, the guidelines below should be followed.

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW3291XA) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW3291XA) and close to OUT pin.

2. If external TVS is used, IN pin routing passes through the external TVS firstly, and then connect AW3291XA.

3. Red bold paths on figure 4 and 5 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

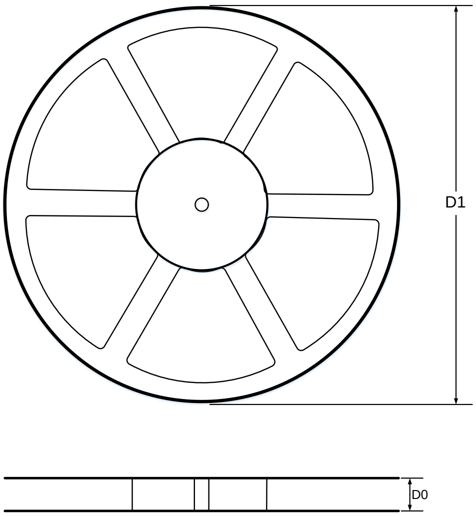
4. If R_1 and R_2 are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.

5. The power trace from USB connector to AW3291XA may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.

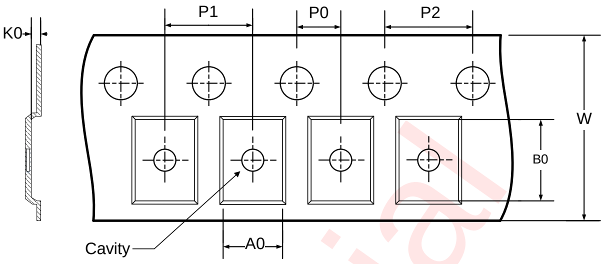
6. Use rounded corners on the power trace from USB connector to AW3291XA to decrease EMI coupling.

Tape and Reel Information

REEL DIMENSIONS

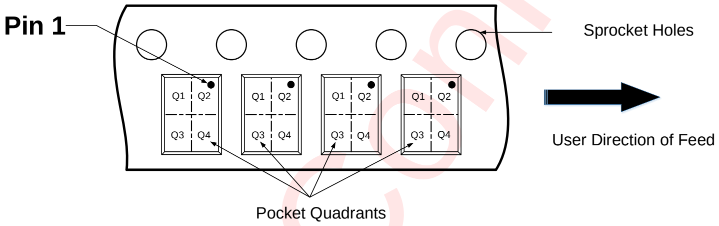


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



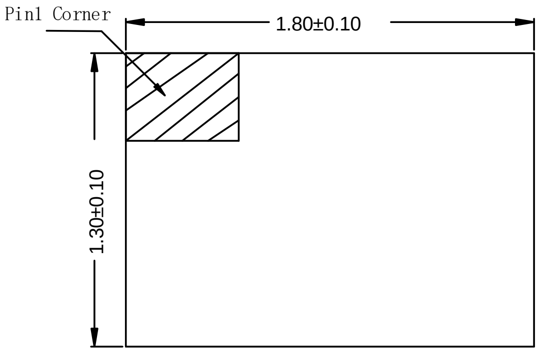
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

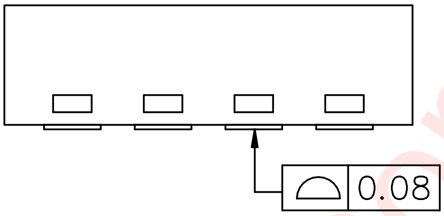
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.58	2.04	0.73	2	4	4	8	Q2

All dimensions are nominal

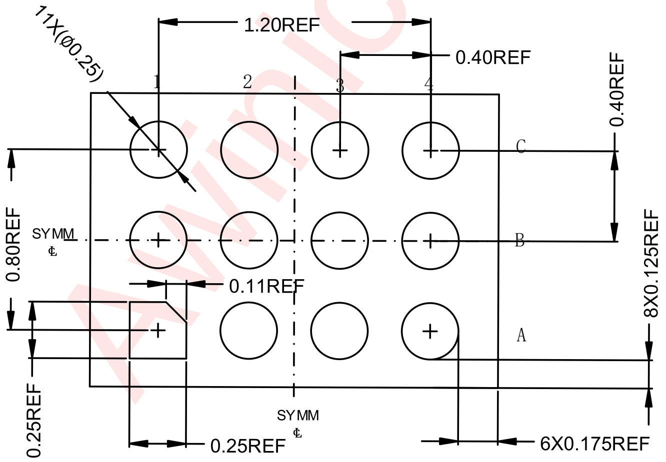
Package Description



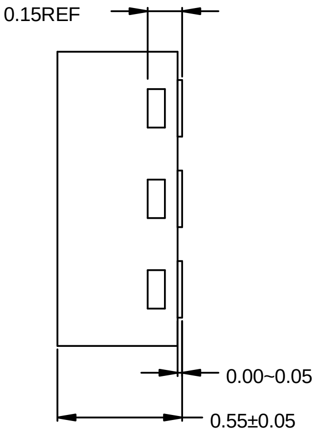
TOP VIEW



SIDE VIEW



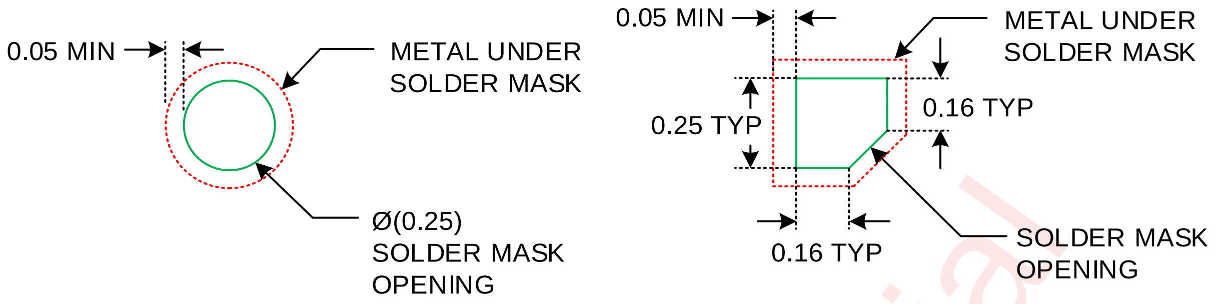
BOTTOM VIEW



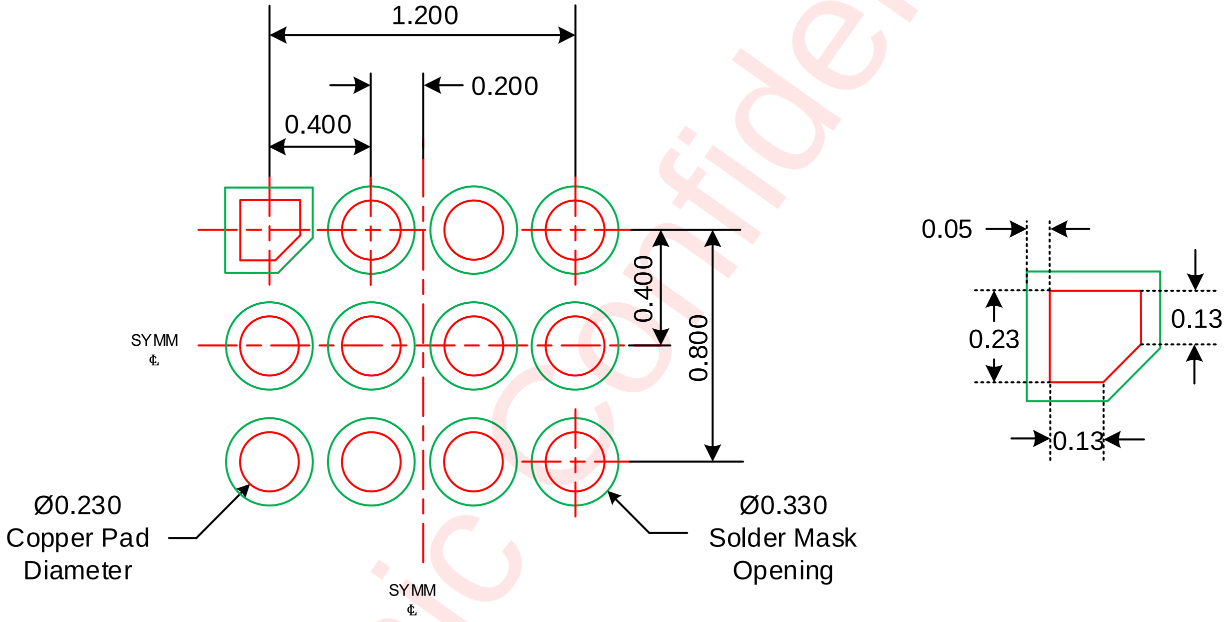
SIDE VIEW

UNIT:mm

Land Pattern Data



Pad Type: Solder Mask Defined



PAD Type: Non-Solder Mask Defined

NOTE:

1. Not to scale
2. Unit: mm.

Revision History

Version	Date	Change Record
V1.0	Sept. 2021	Officially released.
V1.1	Mar.2024	Change V_{IN_CLAMP} value(P8)

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