OIS Close Loop Driver with Internal Hall Sensor

Features

- Supply Voltage : 2.5V to 3.6V
- 2-wire Serial Interface(I²C)
  - ♦ Support Private / Broadcast Communication
  - ♦ Support Frequency Up to 3.4MHz
  - ♦ Support 1.2V / 1.8V I²C Interface
  - ♦ Support Automatic Address Recognition
- Built-in Constant Current Driver
  - ♦ ±150mA Current
  - ♦ 12-bit DAC
- Built-in Hall Sensor
  - ♦ Si Hall Sensor
  - ♦ 8-level Hall Sensor Signal Amplification
  - ♦ Support Hall Sensor Calibration
- Built-in 16bit A/D converter
  - ♦ 14-bit Resolution
  - ♦ Support Temperature and Hall Sampling
- Built-in 512 Bytes eFlash for User
- Built-in PID Controller
  - ♦ PID Coefficients can be Specified by I²C
  - ♦ Support Multi-scenes Application
- Filter Coefficients can be Specified by I²C
- Support Linearization Calibration
- Support Real-time Detection of Vibration Status
- Package
  - ♦ WLCSP 0.600mm x 2.150mm x 0.335mm-6B

General Description

AW86031 is an optical image stabilization (OIS) controller and close loop driver chip, which integrated a constant current driver. The default output current is ±150mA. The supply voltage range is from 2.5V to 3.6V.

AW86031 is controlled through the I²C serial interface that operates at clock rate up to 3.4MHz. The I²C device address can be configured by eFlash. The default address is 0xD8 (7-bit 0x6C).

AW86031 includes internal hall, 512 Bytes eFlash for user, digital PID controller, digital filter, A/D converter, D/A converter, and linearization calibration algorithm .

AW86031 can be used for auto focus or optical image stabilization applications in mobile cameras, digital cameras, camcorders, security cameras, web cameras and action cameras.

Applications

Mobile Camera

Digital Camera

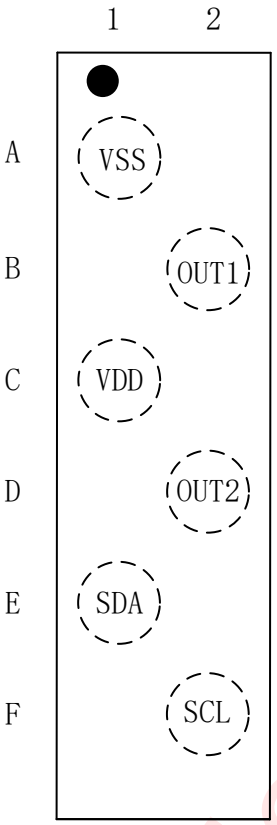
Camcorder

Security Camera

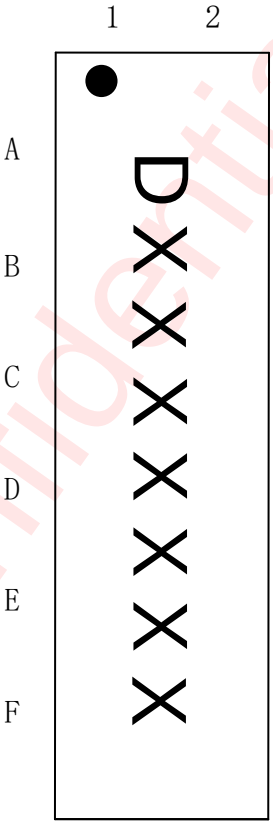
Web Camera and Action cameras

Pin Configuration And Top Mark

AW86031CSR (Top View)



AW86031CSR Marking (Top View)



D – AW86031CSR
XXXXXXX – Production Tracing Code

Figure 1 AW86031 Pin Configuration And Top Mark

Pin Definition

No.	NAME	DESCRIPTION
A1	VSS	Ground
C1	VDD	Chip power supply
E1	SDA	I²C bus data input/output
B2	OUT1	H-bridge driver
D2	OUT2	H-bridge driver
F2	SCL	I²C bus clock input

Functional Block Diagram

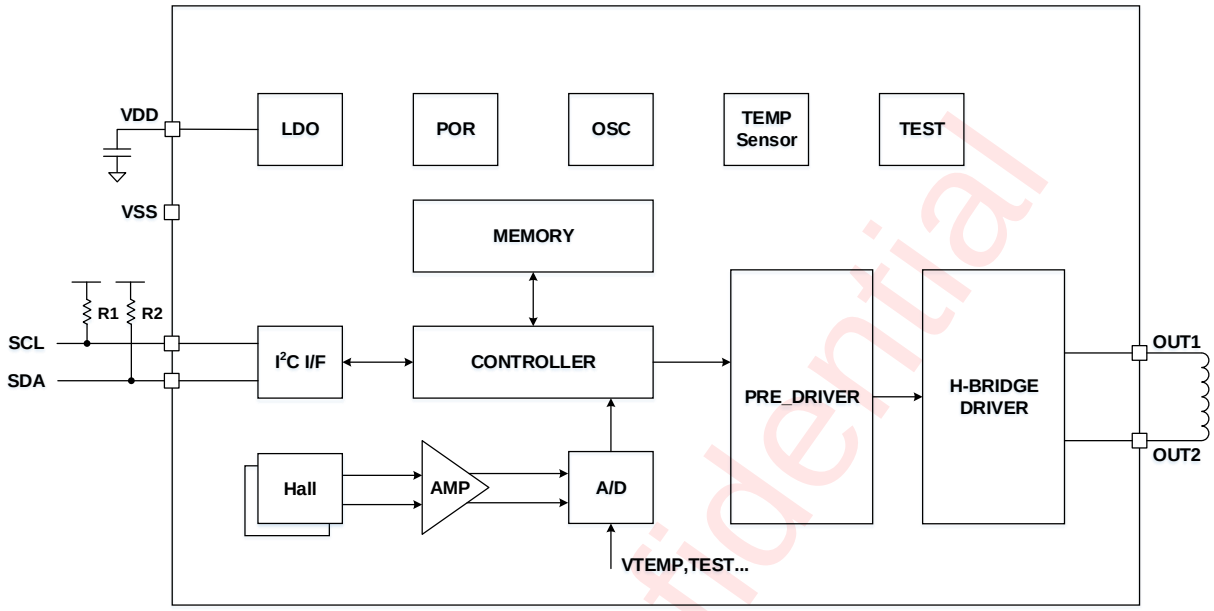


Figure 2 AW86031 Function Block Diagram

Typical Application Circuit

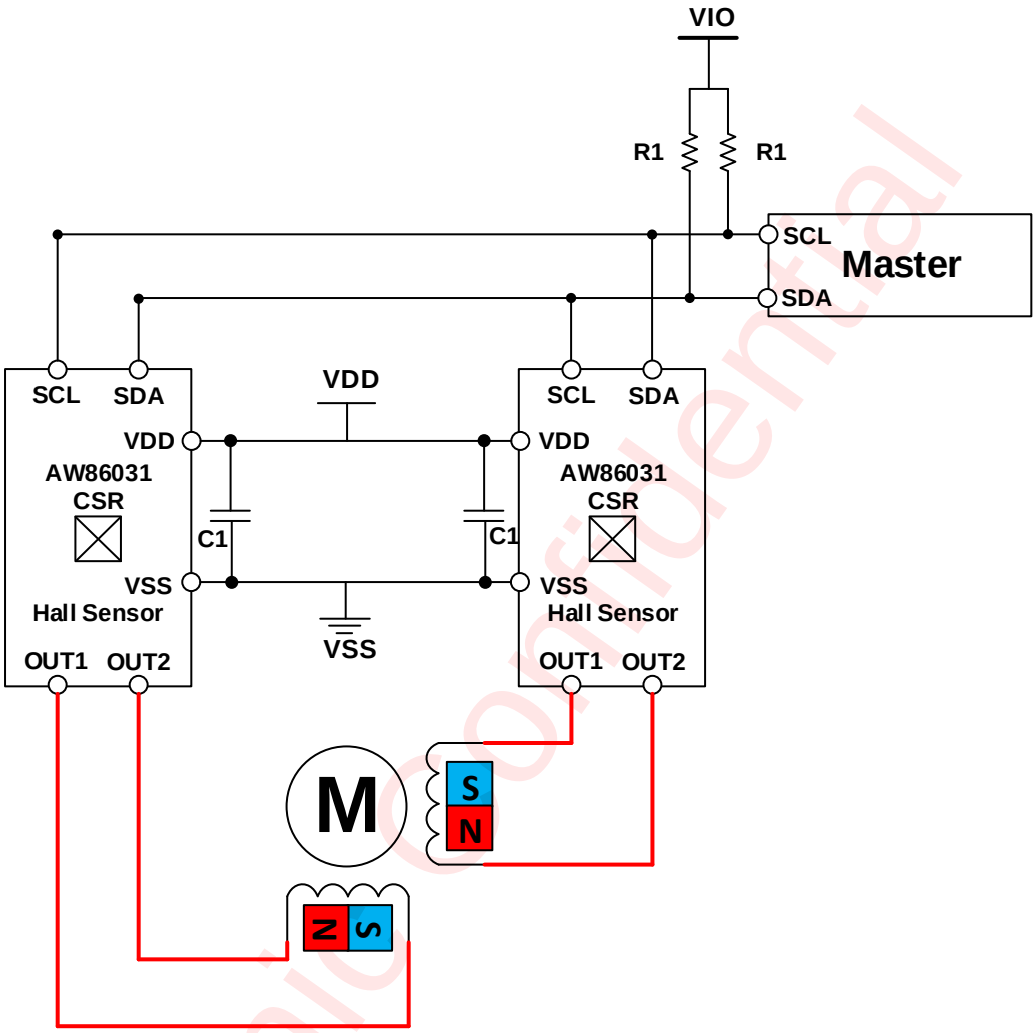


Figure 3 Typical Application Circuit Of AW86031(NOTE1)

NOTE1: More details please refer to "Application Information" and "PCB Layout Consideration".

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86031CSR	-40°C ~ 85°C	WLCSP 0.60mm x 2.15mm x 0.335mm -6B	D	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings

Parameters	Range(NOTE2)
Supply voltage range V_{DD}	-0.3V to 4.2V
Control input voltage range V_{IN}	-0.3V to V_{DD}+0.3V(MAX:4.2V)
Operating free-air temperature range T_{OPR}	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature range T_{STG}	-55°C to 150°C
Lead temperature (soldering 10 seconds)	280°C
ESD(NOTE3)	
Test standard(HBM): ESDA/JEDEC JS-001-2017	±2000V
Test standard(CDM): ESDA/JEDEC JS-002-2018	±1500V
Test standard(MM): JESD22-A115C	±400V
Latch-up	
Test standard: JESD78E	+IT：200mA -IT：-200mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	2.5	2.8	3.6	V
Control Input Voltage	V_{IN}	0		3.6	V

Electrical Characteristics

V_{DD}=2.8V, T_A=25°C for typical values (unless otherwise noted)

Parameter	Symbol	Notes	Condition	Min.	Typ.	Max.	Unit	Applicable pins
Supply Current	IDD	Sleep Mode (0x42[3] = 1)	No Load	3	7	10	μA	
		Sleep Mode (0x42[3] = 0)	No Load	15	25	40	μA	
	IDD	Active Mode	No Load	3	6.8	9	mA	
Supply Turn On Time	TTURNON	(NOTE4)		0.05		3	ms	
Re-start Time	TRESTART	(NOTE5)		50			ms	
Turn On Delay	TDELAY	(NOTE6)		0.5			ms	
DC Characteristics: input/output level								
High-level input voltage	VIH		CMOS compliant Schmidt	0.84			V	SCL, SDA
Low-level input voltage	VIL					0.36	V	
low-level output voltage	VOL		IOL= 20mA			0.4	V	SDA
Driver Output Characteristics								
Output Current	IFULL	Maximum current		140	150	160	mA	OUT1, OUT2
	ILEAK	Leakage current				10	μA	
Output On resistance	ROUTRES	Resistance			2.5		Ω	
eFlash Memory Characteristics								
eFlash Endurance	FEN			1000			Cycles	Flash
eFlash Data Retention	FRE			10			Years	
Program time	TPRO					7.5	μs	
Erase time	TERASE					4	ms	

NOTE4: Start time of V_{DD} power up.

NOTE5: Restart time between power off and power on, and make sure power off reaches V_{SS}.

NOTE6: 2-wire serial interface can operate delay time after power supply reaches 90% of the V_{DD} level.

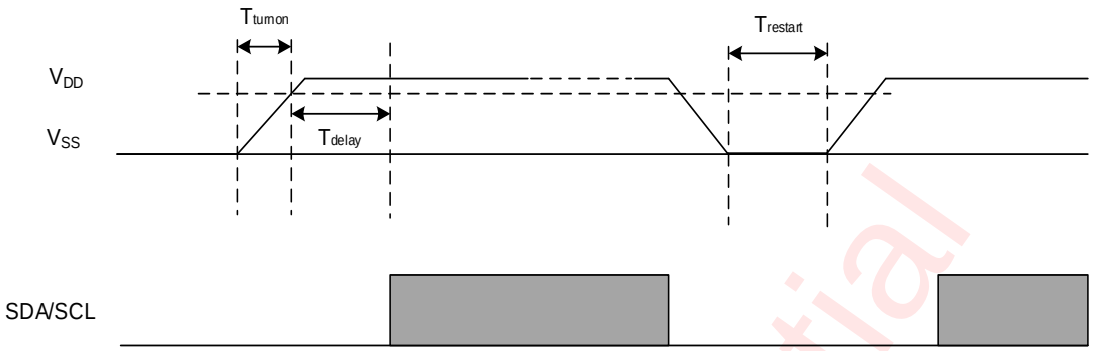


Figure 4 V_{DD} Supply And I^2C Interface Timing

Detailed Functional Description

AW86031 is a close-loop driver chip which can detect the magnet position of Bi-directional voice coil motor(VCM) accurately. The example of magnet movement is shown in the figure below.

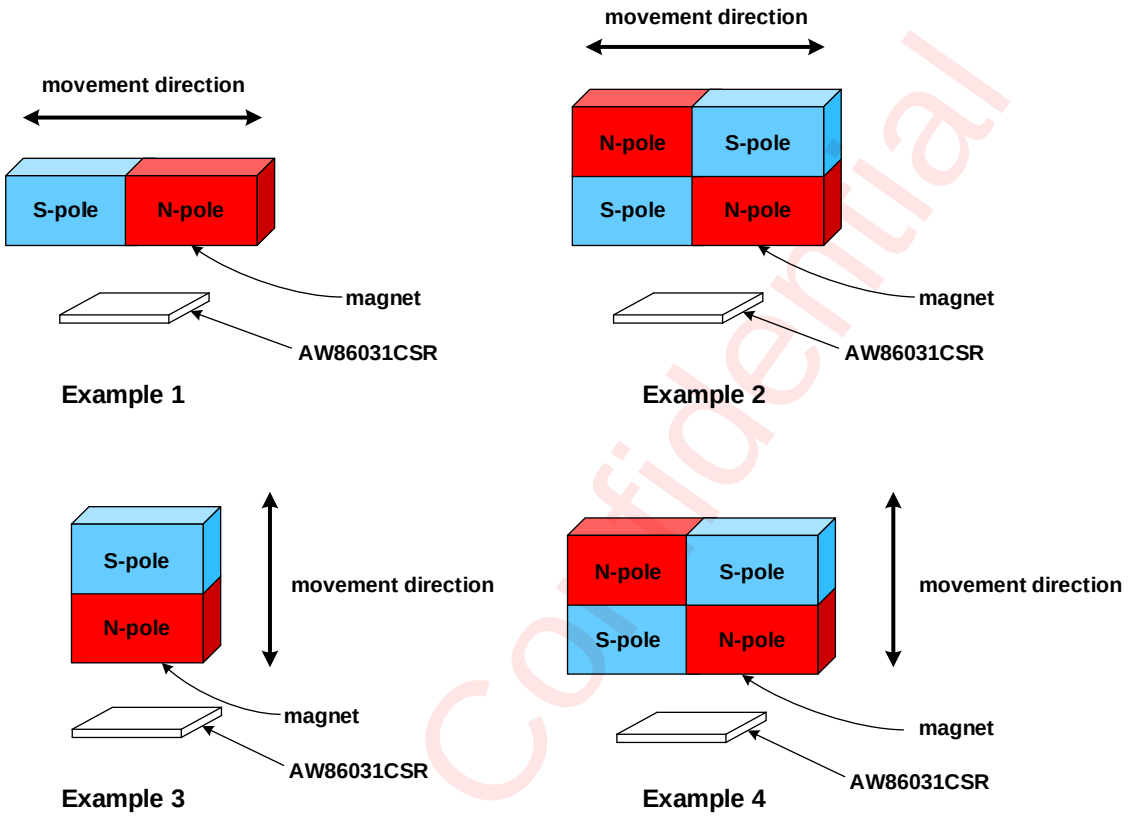


Figure 5 Example Of Magnet Movement

Power-on Sequence

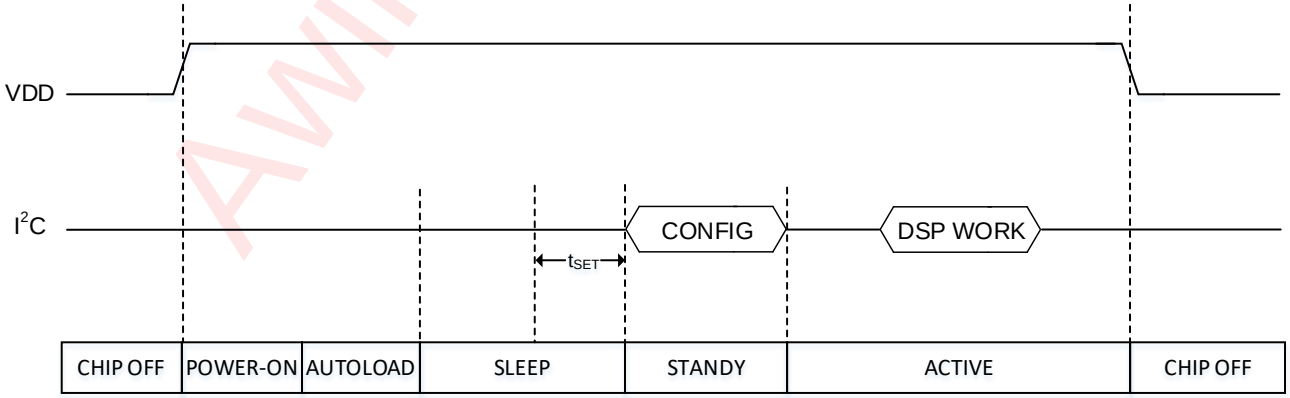


Figure 6 Power-on Sequence

The power on sequence of this device is illustrated in the above figure. In this process, the memory data is automatically loaded into cache with CRC-check algorithm. The result of CRC-check (Address: 09h) can be accessed through I²C interface. At the end of auto-load operation, the device enters Sleep Mode. Mode-switch

can be realized by setting register CHIP_MODE. The above figure is only one example of the cases what can happen after jumping from sleep. Setup waiting time (t_{SET}) is needed when switching the device from Sleep Mode to Standby Mode or Active Mode.

Operation Mode

The device supports 3 operation modes, which are Sleep Mode, Standby Mode and Active Mode. Modes can be switched by configuring register CHIP_MODE.

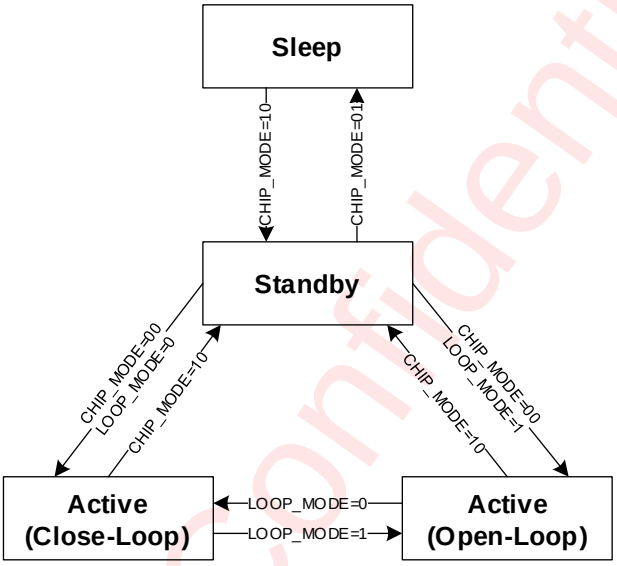


Figure 7 AW86031 Operation Mode

Sleep Mode

The device automatically enters the Sleep mode after power-on process or by setting register CHIP_MODE to “2’b01”. In this mode, I²C interface is accessible, while almost all circuits inside are not work for low power consumption. However, some registers related to scene-switch(1Eh~21h) and e512’(22h~32h) cannot be configured. The device will jump out of this mode when user sets register CHIP_MODE to “2’b00” or “2’b10”. It should be noted that there is a time delay from Sleep mode to Standby or Active mode. The delay time is about 400μs.

Standby Mode

The device switches to Standby Mode by setting register CHIP_MODE to “2’b10”. The output of H-bridge is high-impedance in this mode, while all registers and memory data can be operated. The device will jump out of this mode when register CHIP_MODE is set to “2’b00” or “2’b01”.

Active Mode

The device can be set to Active Mode when register CHIP_MODE is set to “2’b00”. In this mode, VCM can be driven to the target position by H-bridge circuit. The register LOOP_MODE is used to switch the Sub-Active Mode between Open-Loop Mode and Close-Loop Mode, the default setting is “1’b0” which means Close-Loop Mode.

I²C Operation

This device supports the I²C serial bus and data transmission protocol in Fast-mode(Fm) at 400kHz, Fast-mode plus(Fm+) at 1MHz and High-speed mode (Hs-mode) at 3.4MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ. This device can support different high level (1.2V~3.3V) of this I²C interface.

Device Address

Normal Mode

The default device address is 0xD8(7-bit 0x6C), and which can be changed by eFlash memory, the permitted I²C addresses are any non-conflicting 7-bit value between 0x00 and 0x7F.

Self-Adapting Identification Mechanism

The device can self-adaptively identify and adjust the I²C interface and device address according to the hardware connection. As the connection method shown in the following figure, if the device address of Slave A is 0xD8(7-bit 0x6C), then the device address of Slave B is 0xDA(7-bit 0x6D), which means the LSB of the device address of Slave B takes the inverse logic.

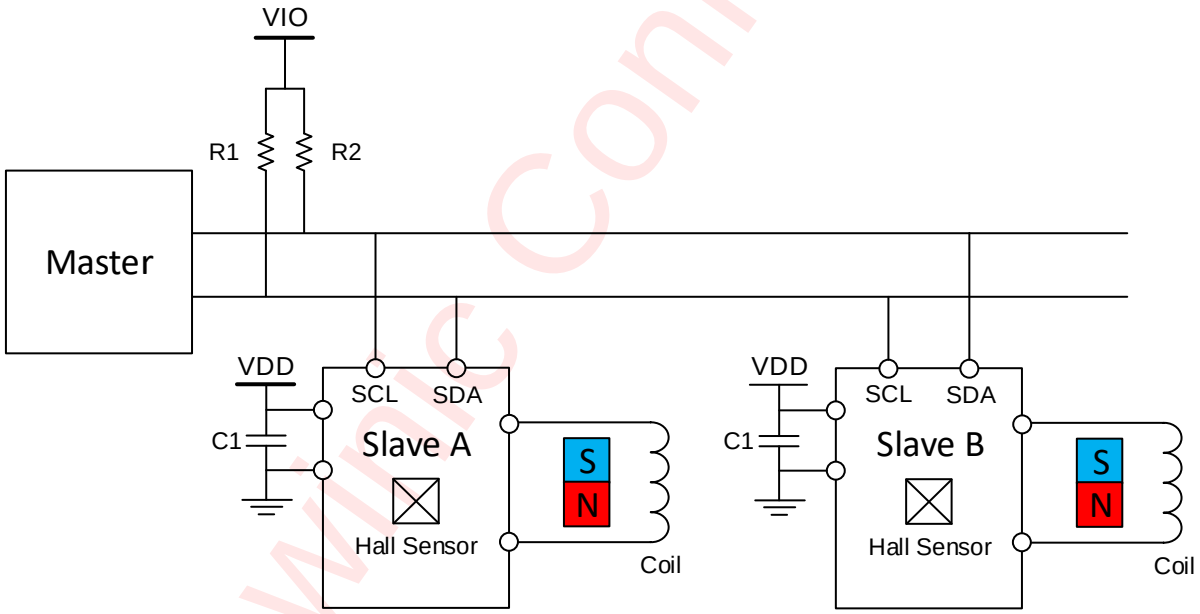


Figure 8 Hardware Connection of Self-Adapting Identification

Broadcast Mode

The device supports broadcast mode, which is not available while broadcast address conflicts with device address. The default broadcast address is 0x00(7-bit 0x00), and which can be changed by eFlash memory, the permitted I²C addresses are any non-conflicting 7-bit value between 0x00 and 0x7F. The broadcast address is additionally used in advanced broadcast mode.

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

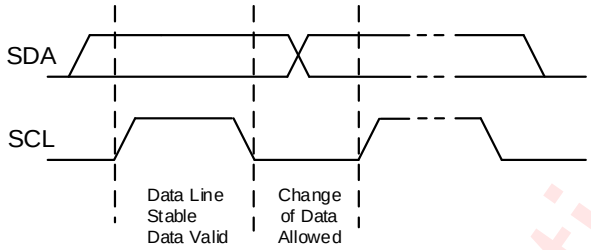


Figure 9 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

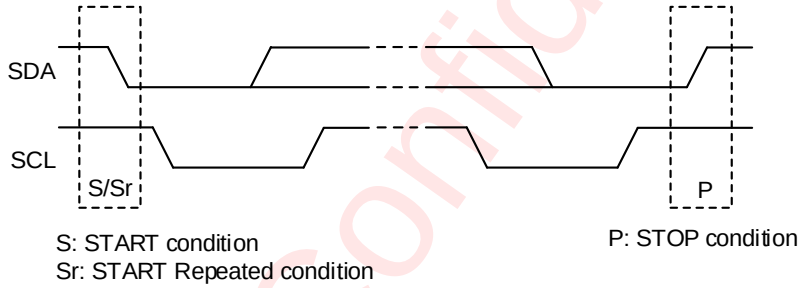


Figure 10 I²C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

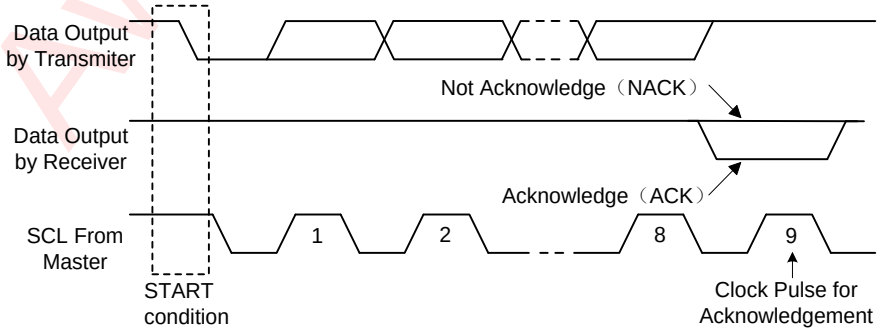


Figure 11 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledgment bits are transferred by the slave device.

As shown in the figure below, the device supports three write modes: Normal Mode, Broadcast Mode, Advanced Broadcast Mode.

Normal Mode

As shown in the figure below, the transmission process follows the steps below:

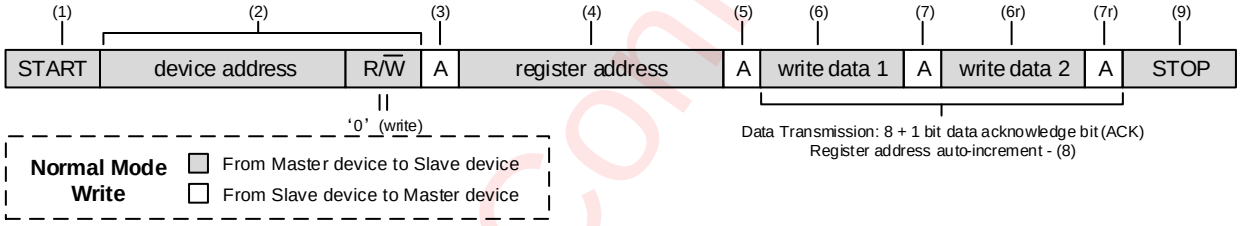


Figure 12 Normal Mode Write Cycle

(1) Master device generates START condition to indicate write cycle start.

(2) Master device transmits 7-bits device address and followed by the "read/write" flag ($R/\overline{W}$ = 0).

(3) Slave device transmits an acknowledgment bit (ACK) to confirm whether the device address is correct.

(4) Master device transmits 8-bits register address.

(5) Slave device transmits an acknowledgment bit (ACK) to confirm whether the register address is correct.

(6) Master device transmits 8-bits write data to the register which needs to be written.

(7) Slave device transmits an acknowledgment bit (ACK) to confirm whether the data is sent successfully.

(8) If master device needs to continue transmitting data, just need to repeat the step 6~7, the following data will adaptively enter burst transmission, which means the corresponding register address will auto-increment.

(9) Master device generates STOP condition to indicate write cycle end.

Broadcast Mode

The transmission process follows the figure below:

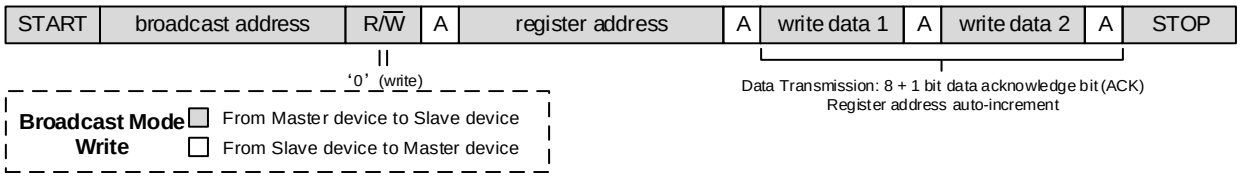


Figure 13 Broadcast Mode Write Cycle

The only difference from Normal Mode is that the device address is replaced by the broadcast address, so that all slaves which respond broadcast call will receive the same write data.

Setup Method

Broadcast mode is available after completing the following configuration. As shown in figure xx, if the hardware connection of slave A is defined as positive, then slave B is negative:

Slave	Connection	Sequence	Device Address.	Register Address.	Register Data	Description
A	positive	1	0xD8	0x54	0x49	Set to improve the stability of multi-device linkage
		2	0xD8	0x55	0xFF	Set to configure write cycle data burst length
		3	0xD8	0x57	0x01	Set to configure data burst slot of each slave
B	negative	1	0xDA	0x54	0x46	Set to improve the stability of multi-device linkage
		2	0xDA	0x55	0xFF	Set to configure write cycle data burst length
		3	0xDA	0x57	0x01	Set to configure data burst slot of each slave

Advanced Broadcast Mode

The transmission process follows the figure below:

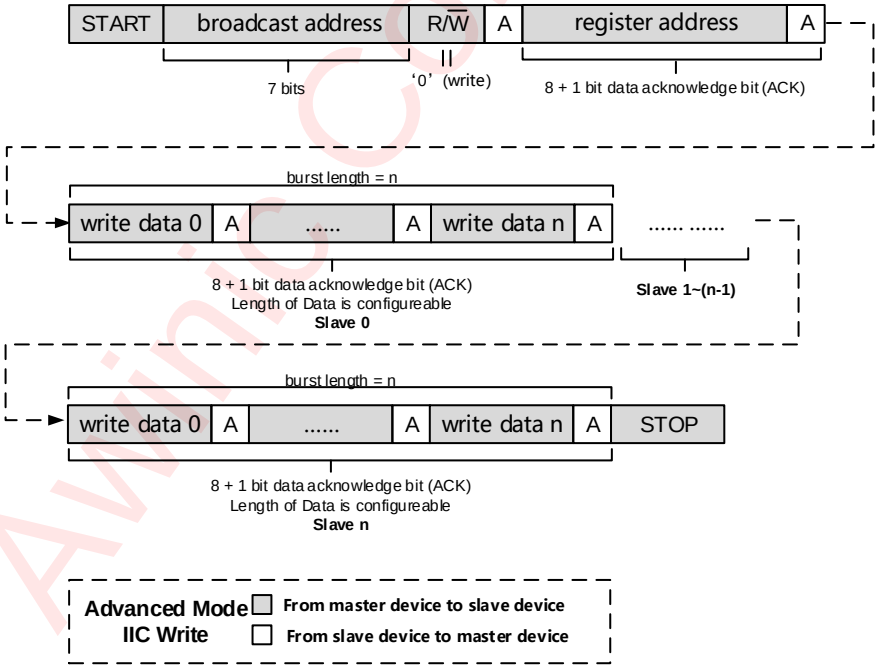


Figure 14 Advanced Broadcast Mode Write Cycle

Setup Method

Advanced broadcast mode is available after completing the following configuration. As shown in figure xx, if the hardware connection of slave A is defined as positive, then slave B is negative. For example, the host needs to send a total of 4 bytes write data if it is assumed that the TARGET registers of two devices are driven synchronously.

Slave	Connection	Sequence	Device Address	Register Address.	Register Data	Description
A	positive	1	0xD8	0x54	0x49	Set to improve the stability of multi-device linkage
		2	0xD8	0x55	0x02	Set to configure write cycle data burst length
		3	0xD8	0x57	0x01	Set to configure data burst slot of each slave
B	negative	1	0xDA	0x54	0x46	Set to improve the stability of multi-device linkage
		2	0xDA	0x55	0x02	Set to configure write cycle data burst length
		3	0xDA	0x57	0x02	Set to configure data burst slot of each slave

Data Update Mechanism – Real-Time Mode

Real-time mode is one of the data update mechanism supported by the device in advanced broadcast mode. Each slave will automatically update the data after writing data matching the configured data burst length.

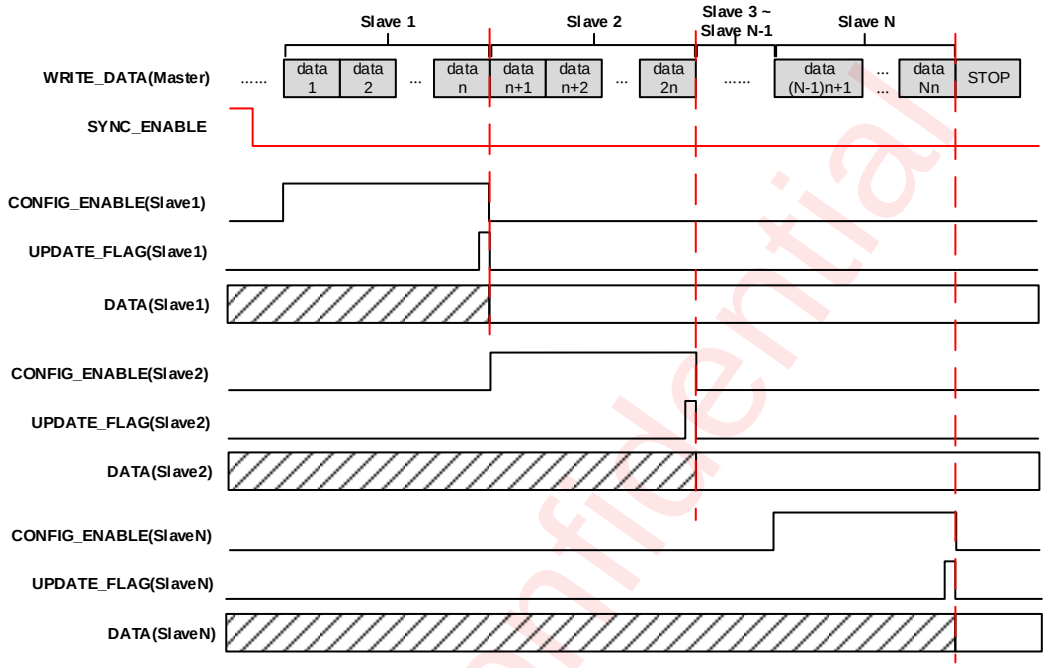


Figure 15 Real-Time Update

Data Update Mechanism – Synchronous Mode

Synchronous mode is one of the data update mechanism supported by the device in advanced broadcast mode. All slaves will automatically update the data after writing a complete data stream and generating a STOP flag.

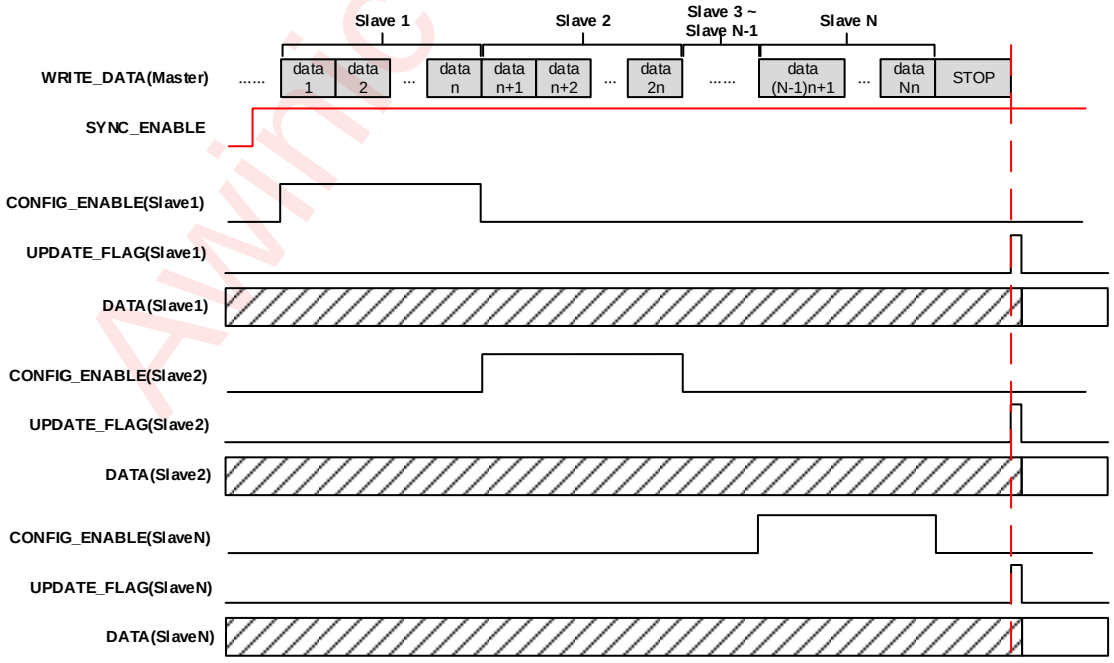


Figure 16 Synchronous Update

Read Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. The master device sends START state and slave address twice, and sends the opposite "read/write" flag after the change. Meanwhile, acknowledgment bits are transferred by the master device after the change.

As shown in the figure below, the device supports two read modes: Normal Mode, Advanced Broadcast Mode.

Normal Mode

As shown in the figure below, the transmission process follows the steps below:

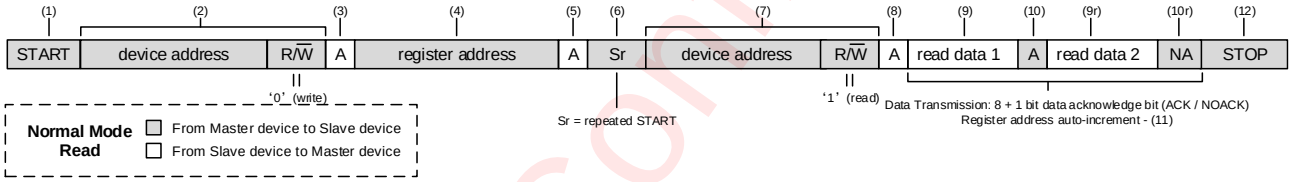


Figure 17 Normal Mode Read Cycle

(1) Master device generates START condition to indicate write cycle start.

(2) Master device transmits 7-bits device address and followed by the "read/write" flag ($R/\overline{W}$ = 0).

(3) Slave device transmits an acknowledgment bit (ACK) to confirm whether the device address is correct.

(4) Master device transmits 8-bits register address.

(5) Slave device transmits an acknowledgment bit (ACK) to confirm whether the register address is correct.

(6) Master device generates repeated START condition to indicate read cycle start.

(7) Master device transmits 7-bits device address and followed by the "read/write" flag ($R/\overline{W}$ = 1).

(8) Slave device transmits an acknowledgment bit (ACK) to confirm whether the device address is correct.

(9) Slave device transmits 8-bits read data from the register which needs to be read.

(10) Master device transmits an acknowledgment bit (ACK) to confirm whether the data is sent successfully. Specially, it is not necessary to acknowledge the last data, which means a non-acknowledgment (NOACK) is acceptable.

(11) If slave device needs to continue transmitting data, just need to repeat the step 9~10, the following data will adaptively enter burst transmission, which means the corresponding register address will auto-increment.

(12) Master device generates STOP condition to indicate read cycle end.

Advanced Broadcast Mode

The transmission process follows the figure below:

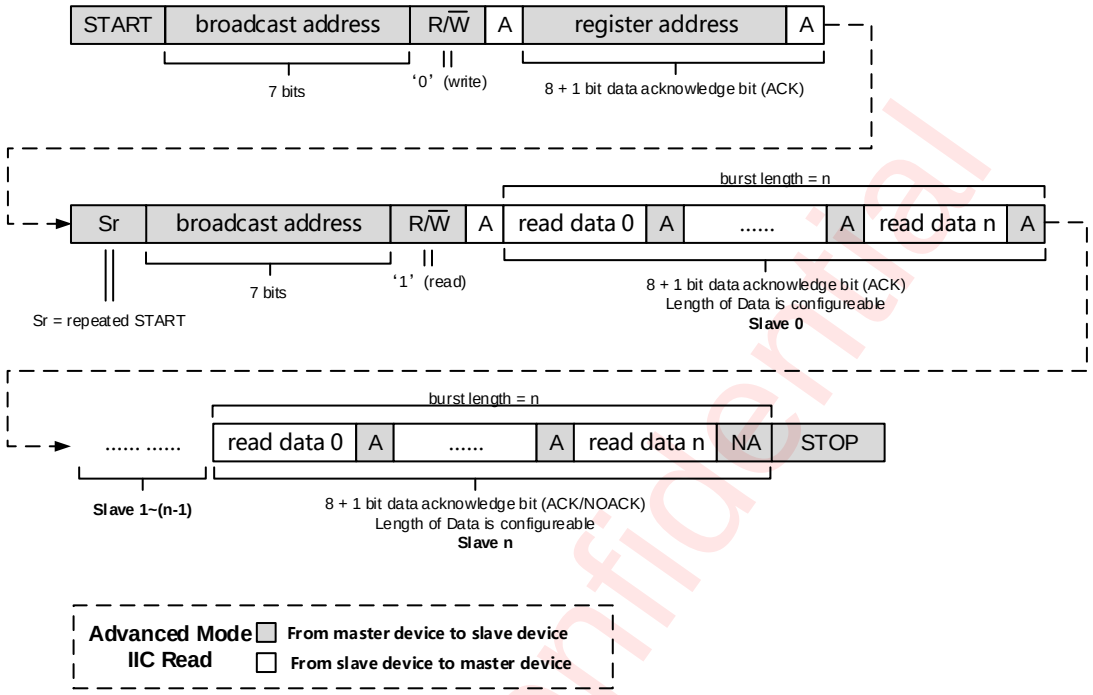


Figure 18 Advanced Broadcast Mode Read Cycle

Setup Method

Advanced broadcast mode is available after completing the following configuration. As shown in figure xx, if the hardware connection of slave A is defined as positive, then slave B is negative. For example, the host needs to receive a total of 12 bytes read data if it is assumed that the ADC_CH registers of two devices needs to be returned.

Slave	Connection	Sequence	Device Address.	Register Address.	Register Data	Description
A	positive	1	0xD8	0x54	0x49	Set to improve the stability of multi-device linkage
		2	0xD8	0x56	0x06	Set to configure read cycle data burst length
		3	0xD8	0x57	0x01	Set to configure data burst slot of each slave
B	negative	1	0xDA	0x54	0x46	Set to improve the stability of multi-device linkage
		2	0xDA	0x56	0x06	Set to configure read cycle data burst length
		3	0xDA	0x57	0x02	Set to configure data burst slot of each slave

Timing Feature

Parameter			Fm		Fm+		Hs-mode		Unit
No.	Symbol	Name	Min	Max	Min	Max	Min	Max	
1	f_{SCL}	SCL Clock frequency		400		1000		3400	KHz
2	t_{LOW}	SCL Low level Duration	1.30		0.50		0.16		μs
3	t_{HIGH}	SCL High level Duration	0.60		0.26		0.06		μs
4	t_{RISE}	SCL, SDA rise time		0.30		0.12		0.04	μs
5	t_{FALL}	SCL, SDA fall time		0.30		0.12		0.04	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.60		0.26		0.16		μs
7	$t_{HD:STA}$	(repeat-start) start condition hold time	0.60		0.26		0.16		μs
8	$t_{SU:STO}$	Stop condition setup time	0.60		0.26		0.16		μs
9	t_{BUF}	Time between start and stop condition	1.30		0.50		0.16		μs
10	$t_{SU:DAT}$	SDA setup time	0.10		0.05		0.01		μs
11	$t_{HD:DAT}$	SDA hold time	0	0.90	0	0.45	0	0.07	μs

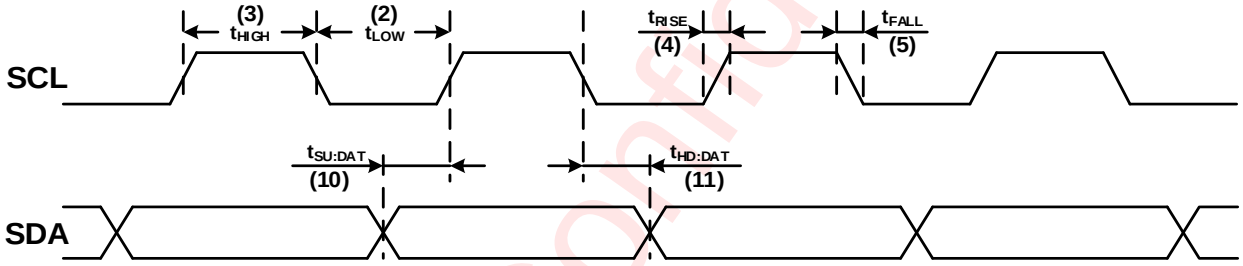


Figure 19 SCL and SDA timing relationships in the data transmission process

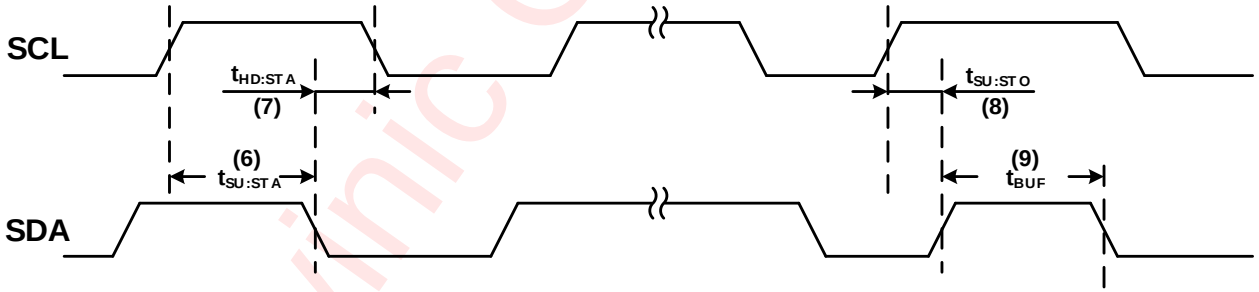


Figure 20 The timing relationship between START and STOP state

eFlash

The storage space of eFlash is 2K bytes and 512 bytes of them is available for users. eFlash data can automatically loaded into cache during power-on process and can also be refreshed with the data in cache. It supports self-check, erase-program-protection and data backup for critical area. ACC_FLS_KEY and ACC_CAC_KEY must be unlocked before operating eFlash. Besides, one-click-programming operation is available in addition to the normal functions.

Erase Operation

The sector/block erase operation allows the system to erase the eFlash on sector-by-sector or block-by-block. The sector architecture is based on uniform sector size of 64 bytes. The block size is 128 bytes. The protection must be unlock before erasing the critical area.

Program Operation

It is necessary to erase the area which need to be refreshed before programing eFlash. The mapping relationship between eFlash and cache should be pre-configured as well. The protection must be unlock before programming the critical area. One-click-programming operation, which based on the program operation, is an extension feature of the device.

Read Operation

There are two types of reading operation, normal read and self-check read. Normal read means reading the data in eFlash without the CRC-check. Self-check read is just the opposite. Before self-check read, the CRC checking code should be programmed into eFlash along with the data to be verified.

DSP System

Remapping Function

The purpose of remapping function is to form a mapping relationship between the target code and stroke. The gain value and the offset value can be configured via I²C based on the motor characteristics.

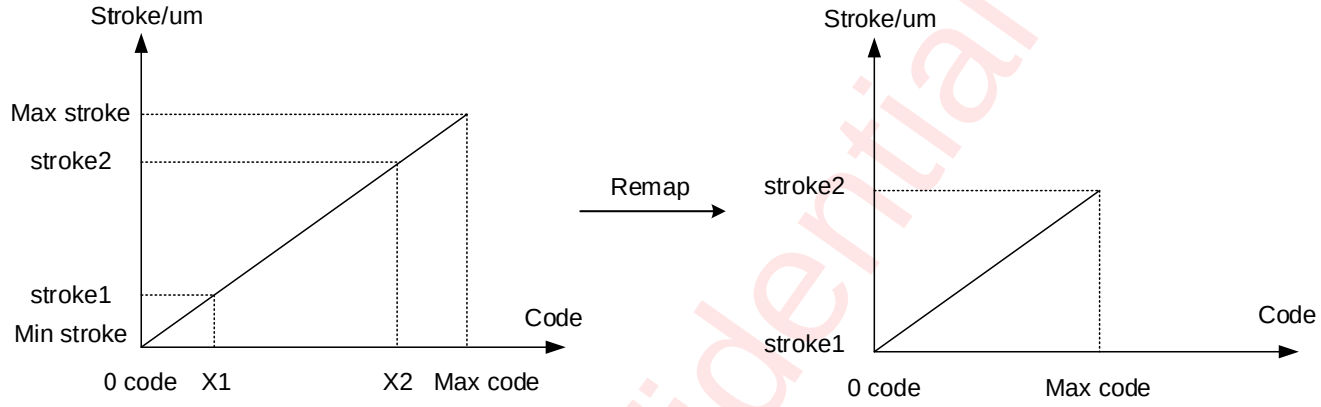


Figure 21 Remapping Function

PID Control

In order to realize the quick stabilization of the motor, there is a built-in PID algorithm circuit in AW86031. It supports the output limiting function and the branch P, I and D parameters are dynamically configurable. In order to increase the stability of the motor, the output of PID can be frozen through the I²C interface. Besides, the output of PID can also be closed for ball motor to reduce power consumption. The PID algorithm circuit is shown in the figure below.

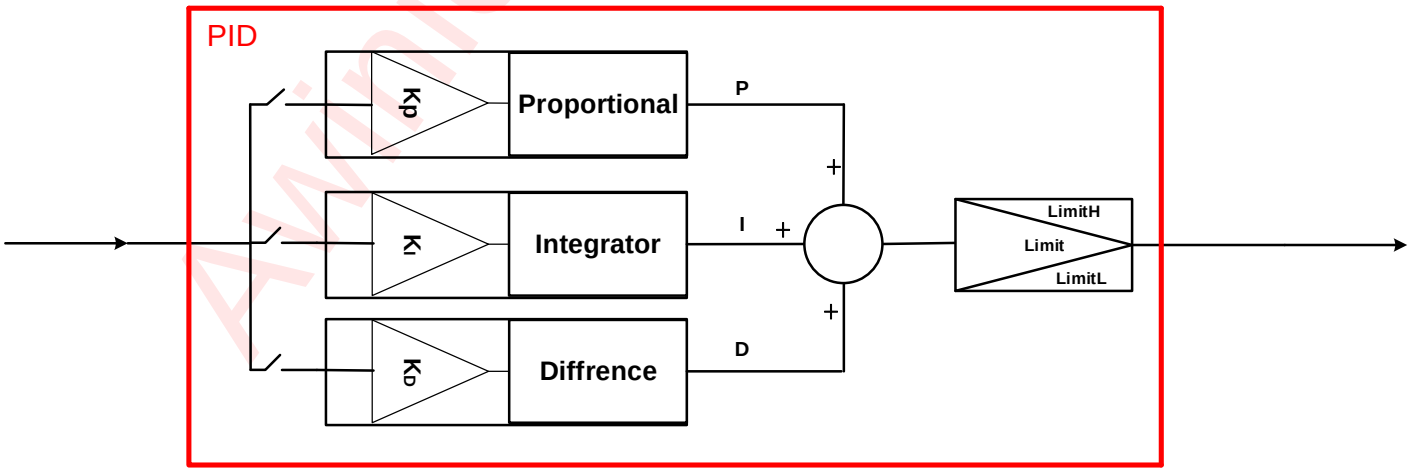


Figure 22 PID Typical Diagram

Linearization Calibration

The device IC supports linearization calibration ,which is carried out through a straight line fitted by the input

signal and VCM stroke. The following is a diagram of this mode.

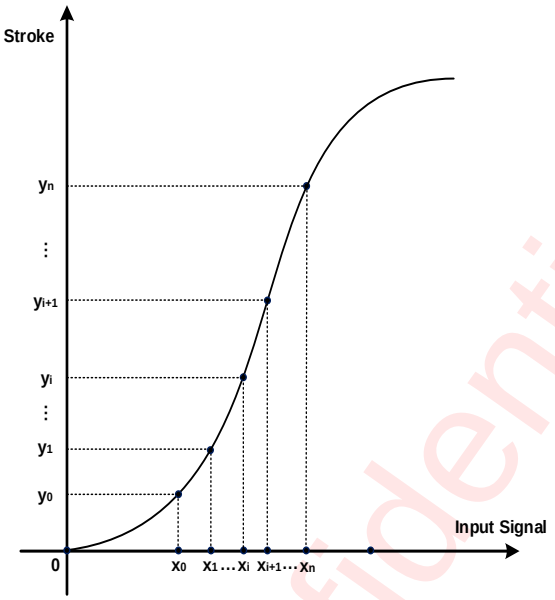


Figure 23 The Linearization Calibration Mode

Protection Mechanism

Over Current Protection (OCP)

This protection function is triggered when the current of any output tube is beyond the pre-set threshold. The output stages will be shut down to prevent damage to itself. After a configurable delay, the output stages of device will restart and the current protection circuit will keep on monitoring as well. The register CHIP_STATUS[5] – OC is accessible to users to monitor this status.

Register Configuration

Register List(NOTE7)

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	TARGET0	RW	TARGH								0x80
0x01	TARGET1	RW	TARGL								0x00
0x02	MODE_CTRL	RW		CHIP_MODE						LOOP_MODE	0x20
0x03	WORK_EN	RW			—	SYNC_TRIG_OFF		—	—	WORK_EN	0x01
0x05	CRC_STATUS0	RO	CRC_STATUS0								0x00
0x06	CRC_STATUS1	RO	CRC_STATUS1								0x00
0x07	CRC_STATUS2	RO	CRC_STATUS2								0x00
0x08	CRC_STATUS3	RO	CRC_STATUS3								0x00
0x09	CRC_STATUS4	RO	CRC_STATUS4								0x00
0x0A	CHIP_STATUS	RW			OC	—	—	—	—	—	0x00
0x0B	PID_STATUS	RW	PID_DONE	PID_BUSY	P_OVFL	P_UDFL	D_OVFL	D_UDFL	PID_OVFL	PID_UDFL	0x00
0x0C	AFE_STATUS	RW	AFE_BUSY	—	HALL_DIV_DIV0	AFE_ERR	AFE_TIME_OUT	ADC_CUR_CH			0x00
0x0D	ADC_CH0H	RO	ADC_CH0H								0x00
0x0E	ADC_CH0L	RO	ADC_CH0L								0x00
0x0F	ADC_CH1H	RO	ADC_CH1H								0x00
0x10	ADC_CH1L	RO	ADC_CH1L								0x00
0x11	ADC_CH2H	RO	ADC_CH2H								0x00
0x12	ADC_CH2L	RO	ADC_CH2L								0x00
0x13	EIS_OUTH	RO	EIS_OUTH								0x10
0x14	EIS_OUTL	RO	EIS_OUTL								0x00
0x15	DRV_OUTH	RO	DRV_OUTH								0x08
0x16	DRV_OUTL	RO	DRV_OUTL								0x00
0x1E	SCSR	RW	AUTO_SCSW_EN	DIRECT_JUMP	SCSW2FLS_BUSY	SCSW2FLS_HIS	SCSW2FLS_CUR	VIBRATING	CONVERGED	REVIBRATE	0x00
0x1F	SCSTCNTH	RO	SCSTCNTH								0x00
0x20	SCSTCNTL	RO	SCSTCNTL								0x00
0x21	ERGDR	RW	SCSW_AUTO_JUMPDIR			ERGD_MAN_JUMPDIR			ERGD_DONE	ERGD_BYPASS	0x01
0x22	SCSWCR	RW	SCSWCR								0x00
0X23	ACC_FLS_KEY	RW	ACC_FLS_KEY								0x00
0X24	ACC_CAC_KEY	RW	ACC_CAC_KEY								0x00
0X26	WP_UNLOCK	RW	WP_UNLOCK								0x00
0x27	OCPO	RW	OCPO								0x00
0x28	EFLASH_ADDR0	RW	BDGFLSNVR				BDGFLSADDR0				0x00
0x29	EFLASH_ADDR1	RW	BDGFLSADDR1								0x00
0x2A	EFLASH_MAP0	RW					ISPFLSMAP0				0x00
0x2B	EFLASH_MAP1	RW	ISPFLSMAP1								0x00
0x2C	CACHE_MAP	RW	CACMAP								0x00
0x2D	CMD_WORD_LEN	RW	ISPWL								0x3F
0x2E	EFLASH_CFG	RW	ISP_TESTEN	ISP_DPSTB_EN	ISP_MAIN_EN	ISP_NVR_EN	ISP_BLOCK	ISP_NVR	ISP_CHIP	ISP_EN	0x60
0x2F	CMD	RW					ISP_CMD				0x08
0x30	CMD_GO	RW	ISP_G0								0x00
0x31	EFLASH_STATUS	RO	ISP_WP_ERROR	ISP_WP_OK	ISP_CMD_BUSY	WKUP_DONE	TRIM_DONE	AUTO_DONE	FLTLIN_DONE	INIT_DONE	0x00
0x32	FLS_T_PGS_WUP	RW	FLS_T_PGS_WUP								0x35
0x33	FLS_DOUT0	RO	FLS_DOUT0_FD								0x00
0x34	FLS_DOUT1	RO	FLS_DOUT1_FD								0x00
0x35	FLS_DOUT2	RO	FLS_DOUT2_FD								0x00
0x36	FLS_DOUT3	RO	FLS_DOUT3_FD								0x00
0x37	RESERVED0	RW	RESERVED0								0x00
0x38	CHIP_ID	RO	CHIP_ID								0x79
0x42	TRIM0	RW					VBG_SEL				0x0C
0x50	PCAC_FLAG	RW	PCAC_FLAG								0xFF
0x51	MODCTRCR	RW	WORK_EN_CAC	CHIP_MODE_CAC		DSP_GATE_EN	LIN_BYPASS	—	EIS_SEL	LIN_SEL	0xA8
0x52	DEVADDR	RW	DEV_ADDR								0x6C
0x53	GNRADDR	RW	GNR_ADDR								0x00
0x54	IIC_CFG	RW	EFLASH_IIC_EN	EN_GNR_ACK	DELAY_SEL	DEG_SEL	SDA_SEL	SCL_SEL	POS_CTR_OFF	NEG_CTR_OFF	0x40
0x55	BURST_LEN_W	RW	CFG_BURST_LEN_W								0xFF
0x56	BURST_LEN_R	RW	CFG_BURST_LEN_R								0xFF
0x57	BURST_SLOT	RW	—	—	—	—	CFG_SLOT_NUM				0x01

NOTE7: eFlash cache registers are identified with a green background.

Register Detailed Description

TARGET0: (Address 00h) Target Register High Part

Bit	Symbol	R/W	Description	Default
7:0	TARGH	RW	13-bits Target Register High Part :Target[12:5]	0x80

TARGET1: (Address 01h) Target Register Low Part

Bit	Symbol	R/W	Description	Default
7:3	TARGL	RW	13-bits Target Register Low Part : Target[4:0]	0x00
2:0	RESERVED	RW	Reserved	0x0

MODE_CTRL: (Address 02h) Chip Mode Switch Control Register

Bit	Symbol	R/W	Description	Default
7	RESERVED	RW	Reserved	0x0
6:5	CHIP_MODE	RW	Chip Mode Switch b00: Active mode b01: Sleep mode(PD mode, default) b10: Standby mode b11: Reserved	0x1
4:1	RESERVED	RW	Reserved	0x0
0	LOOP_MODE	RW	Loop Mode Switch 0: Close Loop 1: Open Loop	0x0

WORK_EN: (Address 03h) Active Mode Work Enable Register

Bit	Symbol	R/W	Description	Default
7:5	RESERVED	RW	Reserved	0x0
4	SYNC_TRIG_OFF	RW	Target Data Synchronous Trigger 0: Enable(default) 1: Disable	0x0
3:1	RESERVED	RW	Reserved	0x0
0	WORK_EN	RW	Active Mode Work Enable 0: Disable 1: Enable	0x1

CRC_STATUS0: (Address 05h) CRC Data Register Page0

Bit	Symbol	R/W	Description	Default
7:0	CRC_STATUS0	RO	CRC Data Register Page0 [8*4+:8]	0x00

CRC_STATUS1: (Address 06h) CRC Data Register Page1

Bit	Symbol	R/W	Description	Default
7:0	CRC_STATUS1	RO	CRC Data Register Page1 [8*3+:8]	0x00

CRC_STATUS2: (Address 07h) CRC Data Register Page2

Bit	Symbol	R/W	Description	Default
7:0	CRC_STATUS2	RO	CRC Data Register Page2 [8*2+:8]	0x00

CRC_STATUS3: (Address 08h) CRC Data Register Page3

Bit	Symbol	R/W	Description	Default
7:0	CRC_STATUS3	RO	CRC Data Register Page3 [8*1+:8]	0x00

CRC_STATUS4: (Address 09h) CRC Data Register Page4

Bit	Symbol	R/W	Description	Default
7:0	CRC_STATUS4	RO	CRC Data Register Page4 [8*0+:8]	0x00

CHIP_STATUS: (Address 0Ah) Chip Status Register

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	RW	Reserved	0x0
5	OC	RW	Over Current Flag Access CHIP_STATUS to Clear the OC Flag	0x0
4:0	RESERVED	RW	Reserved	0x0

PID_STATUS: (Address 0Bh) PID Status Register

Bit	Symbol	R/W	Description	Default
7	PID_DONE	RO	PID Controller Work Done	0x0
6	PID_BUSY	RO	PID Controller Work Busy	0x0
5	P_OVFL	RWC	Factor P Overflow Flag Write 1 to Clear The Factor P Saturation Flag	0x0
4	P_UDFL	RWC	Factor P Underflow Flag Write 1 to Clear The Factor P Saturation Flag	0x0
3	D_OVFL	RWC	Factor D Overflow Flag Write 1 to Clear The Factor D Saturation Flag	0x0
2	D_UDFL	RWC	Factor P Underflow Flag Write 1 to Clear The Factor D Saturation Flag	0x0

1	PID_OVFL	RWC	PID Controller Output Overflow Write 1 to Clear The PID Saturation Flag	0x0
0	PID_UNFL	RWC	PID Controller Output Underflow Write 1 to Clear The PID Saturation Flag	0x0

AFE_STATUS: (Address 0Ch) AFE Status Register

Bit	Symbol	R/W	Description	Default
7	AFE_BUSY	RO	AFE Work Busy	0x0
6	RESERVED	RO	Reserved	0x0
5	HALL_DIV_DIV0	RWC	HALL_DIV Divide Zero Flag Write 1 to Clear the Feedback Error Flag	0x0
4	AFE_ERR	RWC	AFE Error Flag Write 1 to Clear the Feedback Error Flag	0x0
3	AFE_TIME_OUT	RO	AFE Timeout Flag	0x0
2:0	ADC_CUR_CH	RO	ADC Current Digital Channel	0x0

ADC_CH0H: (Address 0Dh) ADC Channel 0 Data High Part

Bit	Symbol	R/W	Description	Default
7:0	ADC_CH0H	RO	ADC Channel 0 Data High Part	0x00

ADC_CH0L: (Address 0Eh) ADC Channel 0 Data Low Part

Bit	Symbol	R/W	Description	Default
7:0	ADC_CH0L	RO	ADC Channel 0 Data Low Part	0x00

ADC_CH1H: (Address 0Fh) ADC Channel 1 Data High Part

Bit	Symbol	R/W	Description	Default
7:0	ADC_CH1H	RO	ADC Channel 1 Data High Part	0x00

ADC_CH1L: (Address 10h) ADC Channel 1 Data Low Part

Bit	Symbol	R/W	Description	Default
7:0	ADC_CH1L	RO	ADC Channel 1 Data Low Part	0x00

ADC_CH2H: (Address 11h) ADC Channel 2 Data High Part

Bit	Symbol	R/W	Description	Default
7:0	ADC_CH2H	RO	ADC Channel 2 Data High Part	0x00

ADC_CH2L: (Address 12h) ADC Channel 2 Data Low Part

Bit	Symbol	R/W	Description	Default
7:0	ADC_CH2L	RO	ADC Channel 2 Data Low Part	0x00

EIS_OUTH: (Address 13h) EIS Output Data High Part

Bit	Symbol	R/W	Description	Default
7:0	EIS_OUTH	RO	EIS Output Data High Part	0x10

EIS_OUTL: (Address 14h) EIS Output Data Low Part

Bit	Symbol	R/W	Description	Default
7:0	EIS_OUTL	RO	EIS Output Data Low Part	0x00

DRV_OUTH: (Address 15h) Driver Output Data High Part

Bit	Symbol	R/W	Description	Default
7:0	DRV_OUTH	RO	Driver Output Data High Part	0x08

DRV_OUTL: (Address 16h) Driver Output Data Low Part

Bit	Symbol	R/W	Description	Default
7:0	DRV_OUTL	RO	Driver Output Data Low Part	0x00

SCSR: (Address 1Eh) Servo Convergence Status Register

Bit	Symbol	R/W	Description	Default
7	AUTO_SCSW_EN	RW	Auto-Switch Scenes Parameter Enable 0: Disable 1: Enable	0x0
6	DIRECT_JUMP	RO	Indicate Jump to Direct When 1	0x0
5	SCSW2FLS_BUSY	RO	Indicate That Scenes is Switching	0x0
4	SCSW2FLS_HIS	RO	Indicate the historical operation of Scene Switching	0x0
3	SCSW2FLS_CUR	RO	Indicate That Scenes Switch Has Happened for Current Target Access SCSR to Clear the SCSW2FLS_CUR Flag.	0x0
2	VIBRATING	RO	Close Loop Vibrating	0x0
1	CONVERGED	RO	Close Loop Converged	0x0
0	REVIBRATE	RO	Close Loop Re-vibrating Access SCSR to Clear the REVIBRATE Flag.	0x0

SCSTCNTH: (Address 1Fh) Servo Convergence Settling Time

Bit	Symbol	R/W	Description	Default
7:0	SCSTCNTH	RO	Servo Convergence Time Time = { SCSTCNTH, SCSTCNTL };	0x00

SCSTCNTL: (Address 20h) Servo Convergence Settling Time				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	SCSTCNTL	RO	Servo Convergence Settling Time Time = { SCSTCNTH, SCSTCNTL };	0x00

ERGDR: (Address 21h) Ergodic Scene Operation Configuration				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	SCSW_AUTO_JUMPDIR	RO	Scenes Switch Auto Jump Direction	0x0
4:2	ERGD_JUMPDIR	RO	Ergodic Operation Jump Direction	0x0
1	ERGD_DONE	RO	Ergodic Operation Done	0x0
0	ERGD_BYPASS	RW	Ergodic Operation Enable 0: Disable 1: Enable	0x1

SCSWCR: (Address 22h) Scenes Switch Controller Register				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	SCSWCR	RW	Scenes Switch Controller Register Must Enable FLS_KEY before Access SCSWCR 0x1A: 1th Scene, Read Out 0x01 0x2A: 2th Scene, Read Out 0x02 0x3A: 3th Scene, Read Out 0x03 0x4A: 4th Scene, Read Out 0x04	0x00

ACC_FLS_KEY: (Address 23h) Access eFlash Key				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	FLS_KEY	RW	Access EFLASH Key Write 0x8A to enable eFlash access authority, Read 0x01 when be enabled.	0x00

ACC_CAC_KEY: (Address 24h) Access CACHE Key				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CAC_KEY	RW	Access CACHE Key Write 0x5A to enable CACHE access authority, Read 0x01 when be enabled.	0x00

WP_UNLOCK: (Address 26h) Write Protection Unlock Key				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	WP_UNLOCK	RW	Write Protection Unlock Key Write 0x88 to unlock Chip Erase protection, Read 0x04 when be enabled. Write 0x55 to unlock eFlash Main Program & Erase protection, Read 0x01 when be enabled. (For head 500bytes only)	0x00

OCPO: (Address 27h) One Click Program				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	OCPO	RW	One Click Program When Write: 0x87: Main One Click Program Trigger. When Read: Bit[7:6]: Reserved Bit[5]: NVR OCP Flag, auto clear when OCP done. Bit[4]: NVR OCP Flag, auto clear when OCP done. Bit[3:0]: OCP_STATE	0x00

EFLASH_ADDR0: (Address 28h) Bridge eFlash Access Address High Part				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	BDGFLSNVR	RW	Bridge eFlash Access NVR Enable Must Enable FLS_KEY before Access BDGFLSNVR	0x0
6:4	RESERVED	RW	Reserved	0x0
3:0	BDGFLSADDR0	RW	Bridge eFlash Access Address High Part Must Enable FLS_KEY before Access BDGFLSADDR0. Unit is Byte, But Must Align By Word. Address = (BDGFLSADDR0 << 8) + BDGFLSADDR1	0x0

EFLASH_ADDR1: (Address 29h) Bridge eFlash Access Address Low Part				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	BDGFLSADDR1	RW	Bridge eFlash Access Address Low Part Must Enable FLS_KEY before Access BDGFLSADDR1. Unit is Byte, But Must Align By Word. Address = (BDGFLSADDR0 << 8) + BDGFLSADDR1	0x00

EFLASH_MAP0: (Address 2Ah) ISP eFlash Mapping Address High Part				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ISPFLSMAP0	RW	ISP eFlash Mapping Address High Part Must Enable FLS_KEY before Access ISPFLSMAP0. Unit Is Byte, But Must Be Align By Word. Address = (ISPFLSMAP0 << 8) + ISPFLSMAP1	0x00

EFLASH_MAP1: (Address 2Bh) ISP eFlash Mapping Address Low Part				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ISPFLSMAP1	RW	ISP eFlash Mapping Address Low Part Must Enable FLS_KEY before Access ISPFLSMAP1. Unit Is Byte, But Must Be Align By Word. Address = (ISPFLSMAP0 << 8) + ISPFLSMAP1	0x00

CACHE_MAP: (Address 2Ch) CACHE Mapping Address				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CACMAP	RW	CACHE Mapping Address Must Enable FLS_KEY before Access CACMAP. Unit Is Byte, But Must Be Align By Word.	0x00

CMD_WORD_LEN: (Address 2Dh) ISP Access Byte Length				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ISPWL	RW	ISP Access Word Length Must Enable FLS_KEY before Access ISPWL. Unit Is Byte, But Must Be Align By Word.	0x3F

EFLASH_CFG: (Address 2Eh) eFlash Configure				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	ISP_TESTEN	RW	eFlash Test Enable Must Enable FLS_KEY before Access ISP_TESTEN 0: disable 1: enable	0x0
6	ISP_DPSTB_EN	RW	Deep Standby Enable Must Enable FLS_KEY before Access ISP_DPSTB_EN 0: disable 1: enable	0x1
5	ISP_MAIN_EN	RW	eFlash Main Memory Access Enable Must Enable FLS_KEY before Access ISP_MAIN_EN 0: disable 1: enable	0x1
4	ISP_NVR_EN	RW	eFlash NVR Memory Access Enable Must Enable FLS_KEY before Access ISP_NVR_EN 0: disable 1: enable	0x0
3	ISP_BLOCK	RW	ISP Block Access Enable Must Enable FLS_KEY before Access ISP_BLOCK. Configure When Block Erase. Every Block Contains 128Bytes, ISPFLSMAP0[11:7] Indicate Which Block.	0x0
2	ISP_NVR	RW	ISP NVR Main Memory Selector Must Enable FLS_KEY before Access ISP_NVR 0: Main Array 1: NVR Every NVR Contains 64Bytes; NVR2 Program By Fab, ISPFLSMAP1[6] Indicate NVR1 or NVR2. 0: NVR1 1: NVR2	0x0
1	ISP_CHIP	RW	ISP Chip Access Enable Must Enable FLS_KEY before Access ISP_CHIP. Configure When Chip Erase. 0: disable 1: enable	0x0
0	ISP_EN	RW	ISP Access Enable Must Enable FLS_KEY before Access ISP_EN 0: eFlash Bridge 1: ISP	0x0

CMD: (Address 2Fh) ISP Access Controller				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	RESERVED	RW	Reserved	0x0
3:0	ISP_CMD	RW	ISP Access Command Write 0x00 to eFlash data Load And Refresh Data To Cache. Write 0x02 to Program And Save Data From Cache. Write 0x04 to Erase. Write 0x08 to Load NVR1/MAIN And Refresh To Cache. Write 0x0A to Load Only for CRC.	0x8

CMD_GO: (Address 30h) ISP Access Go Trigger				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ISP_GO	RW	ISP Access Go Trigger Write 0xAA to Enable ISP Access Go Trigger.	0x00

EFLASH_STATUS: (Address 31h) eFlash Status				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	ISP_WP_ERROR	RO	Program & Erase Protect Unlock Error Flag for NVR & Part Main	0x0
6	ISP_WP_OK	RO	Program & Erase Protect Unlock Success Flag for NVR & Part Main	0x0
5	ISP_CMD_BUSY	RO	eFlash is Handing Command	0x0
4	WKUP_DONE	RO	eFlash Wake Up Flag	0x0
3	TRIM_DONE	RO	Trim Data Has Load to Cache	0x0
2	AUTO_DONE	RO	Auto Load Finished Flag	0x0
1	FLTLIN_DONE	RO	FLTLIN Parameter CRC Check Finished Flag	0x0
0	INIT_DONE	RO	eFlash Ready Flag	0x0

FLS_T_PGS_WUP: (Address 32h) eFlash Time Configuration for Tpgs & Tprog & Twup				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:0	FLS_T_PGS_WUP	RW	eFlash Time Configuration for Tpgs & Tprog & Twup WEb low to PROG2 high setup time @Tpgs: 3us ~ 4.8us Bits(x4) Program time @Tprog: 6us ~ 7.5us Wake up time from deep standby mode to any operation(CEb low) @Twup: 3us ~ unlimited	0x35

FLS_DOUT0: (Address 33h) eFlash data by bridge

Bit	Symbol	R/W	Description	Default
7:0	FLS_DOUT0	RO	eFlash data by bridge read output FLS_DOUT = (FLS_DOUT0 << 24) + (FLS_DOUT1 << 16) + (FLS_DOUT2 << 8) + FLS_DOUT3	0x00

FLS_DOUT1: (Address 34h) eFlash data by bridge

Bit	Symbol	R/W	Description	Default
7:0	FLS_DOUT1	RO	eFlash data by bridge read output FLS_DOUT = (FLS_DOUT0 << 24) + (FLS_DOUT1 << 16) + (FLS_DOUT2 << 8) + FLS_DOUT3	0x00

FLS_DOUT2: (Address 35h) eFlash data by bridge

Bit	Symbol	R/W	Description	Default
7:0	FLS_DOUT2	RO	eFlash data by bridge read output FLS_DOUT = (FLS_DOUT0 << 24) + (FLS_DOUT1 << 16) + (FLS_DOUT2 << 8) + FLS_DOUT3	0x00

FLS_DOUT3: (Address 36h) eFlash data by bridge

Bit	Symbol	R/W	Description	Default
7:0	FLS_DOUT3	RO	eFlash data by bridge read output FLS_DOUT = (FLS_DOUT0 << 24) + (FLS_DOUT1 << 16) + (FLS_DOUT2 << 8) + FLS_DOUT3	0x00

RESERVED0: (Address 37h) Reserved Register 0

Bit	Symbol	R/W	Description	Default
7:0	RESERVED0	RW	Reserved Register 0	0x00

CHIP_ID: (Address 38h) Chip ID

Bit	Symbol	R/W	Description	Default
7:0	CHIP_ID	RO	Chip ID	0x79

TRIM0: (Address 42h) TRIM0

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	RW	Reserved	0x0
3	VBG_SEL	RW	V2I_BIAS Reference Voltage Selection 0: VDD 1: VBG	0x1
2:0	RESERVED	RW	Reserved	0x4

PCAC_FLAG: (Address 50h) Private Cache Operation Permission Flag

Bit	Symbol	R/W	Description	Default
7:0	PCAC_FLAG	RW	Private Cache Operation Permission Flag Write 0xAA to unlock operation permission.	0xFF

MODCTRCR: (Address 51h) Mode Controller Register

Bit	Symbol	R/W	Description	Default
7	WORK_EN_CAC	RW	Active Mode Work Enable(Initialization) 0: Disable 1: Enable	0x1
6:5	CHIP_MODE_CAC	RW	Chip Mode Switch(Initialization) b00: Active mode b01: Sleep mode(PD mode, default) b10: Standby mode b11: Reserved	0x1
4	DSP_GATE_EN	RW	DSP Clock Gating Enable 0: Disable 1: Enable	0x0
3	LIN_BYPASS	RW	Configurable Linear Bypass 0: Normal 1: Bypass	0x1
2	RESERVED	RW	Reserved	0x0
1	EIS_SEL	RW	EIS Mode Selection 0: EIS_OUT = FB_OUT (Feedback, Linear Output) 1: EIS_OUT = FW_BIAS_OUT(Feedforward, TARG - ERR)	0x0
0	LIN_SEL	RW	Linear Input Load Path Selection 0: Load Linear 1: Load EIS_OUT	0x0

DEVADDR: (Address 52h) IIC Device Address

Bit	Symbol	R/W	Description	Default
7	RESERVED	RW	Reserved	0x0
6:0	DEV_ADDR	RW	IIC Device Address for Private Call	0x6C

GNRADDR: (Address 53h) IIC General Address

Bit	Symbol	R/W	Description	Default
7	RESERVED	RW	Reserved	0x0

6:0	GNR_ADDR	RW	IIC General Address for General Call	0x00

IIC_CFG: (Address 54h) IIC Configuration Register

Bit	Symbol	R/W	Description	Default
7	EFLASH_IIC_EN	RW	eFlash Load Mode Switch 0: Real-time load eFlash data in Active Mode 1: Operate IIC Command to load eFlash data	0x0
6	EN_GNR_ACK	RW	General Mode Acknowledge Enable 0: Disable 1: Enable	0x1
5	DELAY_SEL	RW	Delay Mode Selection Set to 1 means increase delay for both SCL/SDA.	0x0
4	DEG_SEL	RW	Deglitch Mode Selection Set to 1 means increase deglitch for both SCL/SDA.	0x0
3	SDA_SEL	RW	Deglitch Setting for SDA For positive connection used only, default is balanced deglitch setting.	0x0
2	SCL_SEL	RW	Deglitch Setting for SCL For negative connection used only, default is balanced deglitch setting.	0x0
1	POS_CTR_OFF	RW	Positive Slave Controller Work Disable For negative connection used only, default is dual salve controller work simultaneously.	0x0
0	NEG_CTR_OFF	RW	Negative Slave Controller Work Disable For positive connection used only, default is dual salve controller work simultaneously.	0x0

BURST_LEN_W: (Address 55h) IIC General Mode Burst Length of Write Data Configuration Register

Bit	Symbol	R/W	Description	Default
7:0	CFG_BURST_LEN_W	RW	IIC General Mode Burst Length of Write Data Configuration Default length is 256 in General Default Mode. Set to 1 in General Default Mode means burst transmission is forbidden. Set to 0 equals set to 1.	0xFF

BURST_LEN_R: (Address 56h) IIC General Mode Burst Length of Read Data Configuration Register

Bit	Symbol	R/W	Description	Default
7:0	CFG_BURST_LEN_R	RW	IIC General Mode Burst Length of Read Data Configuration Default length is 256 in General Default Mode. Read transmission in General Default Mode is forbidden. Set to 0 equals set to 1.	0xFF

BURST_SLOT: (Address 57h) IIC General Mode Slot Configuration Register

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	RW	Reserved	0x0
3:0	CFG_SLOT_NUM	RW	IIC General Mode Slot Number Configuration It must be set to 1 for each slaves which is in the same system during General Default Mode. Set to 0 equals set to 1.	0x1

Application Information

Capacitor Selection

Recommend decoupling capacitor (C1) value is at least 1μF.

Resistor Selection

Recommend pull-up resistor (Rp) value is 4.7kΩ@f_{SCL}=400kHz, 1kΩ@f_{SCL}=1MHz or 270Ω@f_{SCL}=3.4MHZ.

PCB Layout Consideration

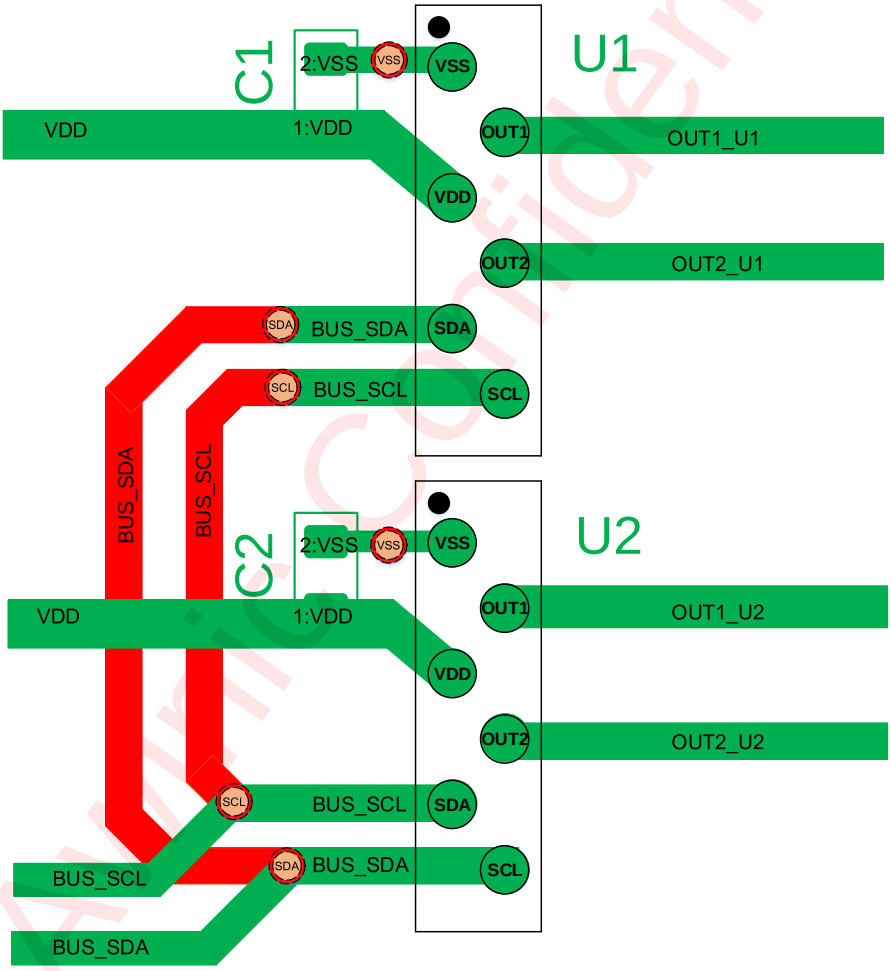


Figure 26 AW86031 PCB Layout Placement

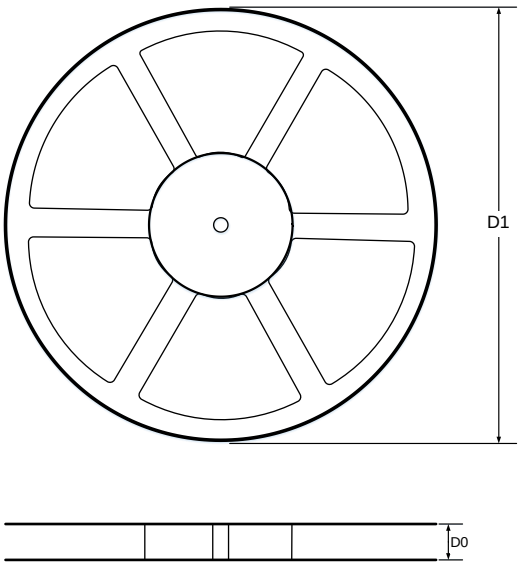
To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. The decoupling capacitor C1 should be placed close to the chip VDD and GND on the same layer as the chip to ensure the best filtering effect.
2. I^2C bus should be surrounded by GND as much as possible.
3. VDD,OUT1,OUT2 should be routed as thick as possible after exiting from the pad to meet the overcurrent capability; VDD,OUT1,OUT2 must be routed to meet at least 250mA of current.
4. For ensuring the built-in hall work properly, the chip should be kept away from transformers, inductors,

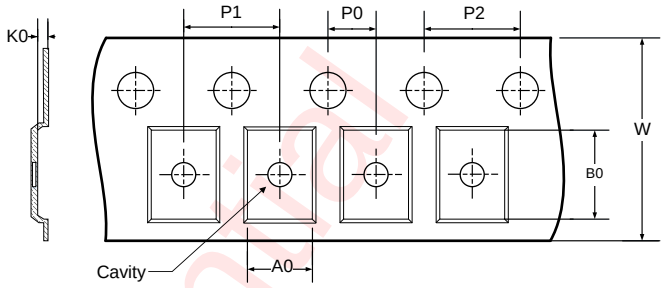
high-current wiring and other devices that generate magnetic fields, and make sure there is no magnetic shielding material between the chip and the magnet.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

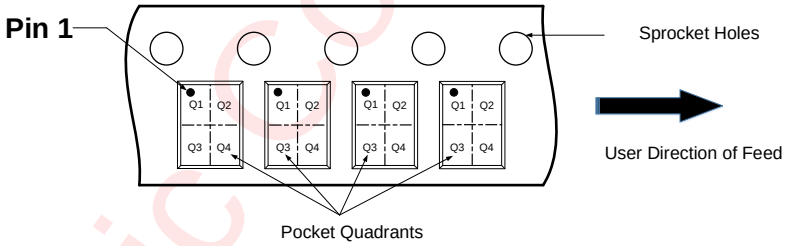


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



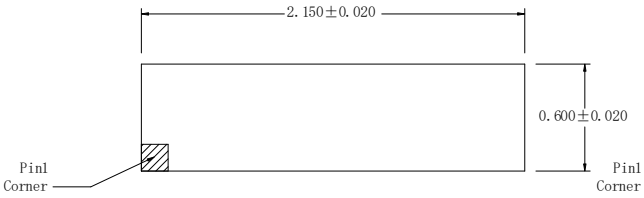
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

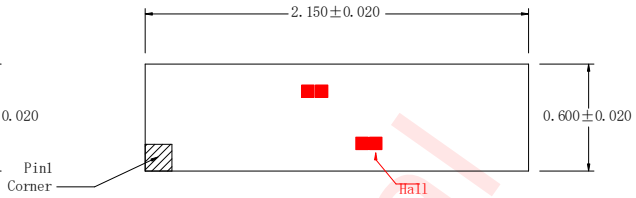
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	8.6	0.7	2.3	0.4	2	4	4	8	Q1

All dimensions are nominal

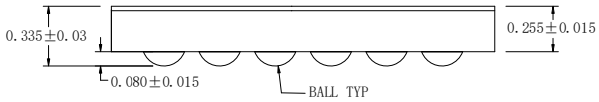
PACKAGE DESCRIPTION



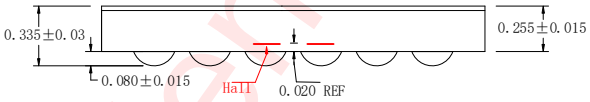
Top View



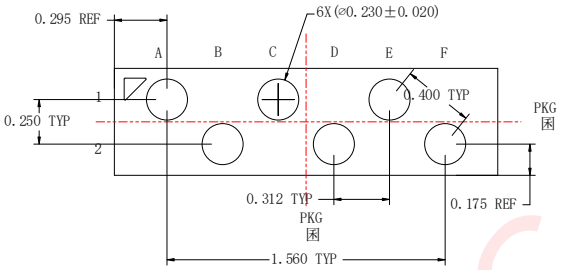
Top View With Hall



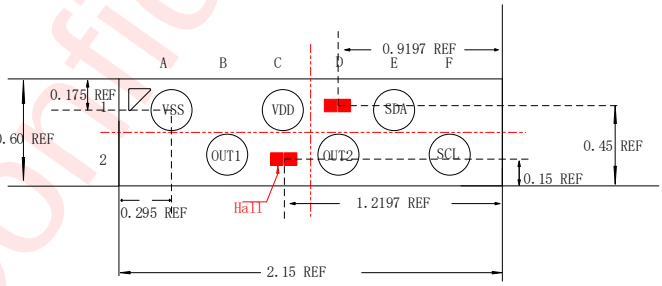
Side View



Side View With Hall



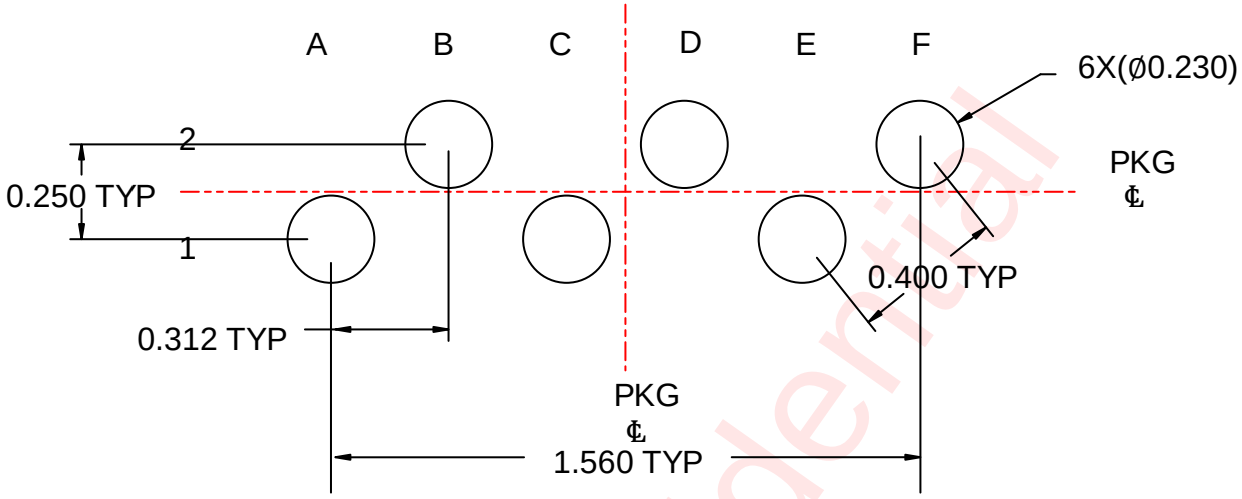
Bottom View

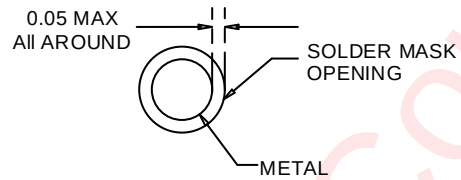


Bottom View With Hall

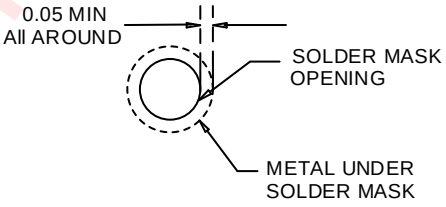
Unit: mm

LAND PATTERN DATA





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2022	Officially released.
V1.1	Apr. 2023	Update the description of linearization Calibration Update the description of Protection Mechanism Update the description of Electrical Characteristics Update the Typical Application Circuit Update the 512 bytes of eflash is available for users Update the description of General Description Update the description of target register
V1.2	Oct. 2023	Update the open-loop and closed-loop state switching picture Modify eflash lifetime and usage description Delete the RSTN pin of the power-on sequence Modify the 0x0a register description
V1.3	Feb. 2024	Fix the real-time name error on page 14 The minimum power supply voltage is changed from 1.8V to 2.5V Add a sleep mode power description Add the 0x42 register description Modify VIH, VIL, and IOL on page 6
V1.4	Apr. 2024	Change the format of the package description Add the hall location
V1.5	Oct. 2024	Modify the Supply Turn On Time Modify the description of NOTE4, NOTE5, and NOTE6

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