2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

Features

- Voltage Level Translator Without Direction-Control Signal
- Maximum Data Rates
  - 24Mbps (Push Pull)
  - 2Mbps (Open Drain)
- Power Supply Range:
  - A Port and VCCA: 1.1V to 3.6 V
  - B Port and VCCB: 1.65 V to 5.5 V
  - VCCA ≤ VCCB
- Pull Up Resistors are Integrated in A Port and B Port
- No Power-Supply Sequencing Required: Either VCCA or VCCB Can be Ramped First
- Support Ultra-Low Power Consumption Mode with OE Pin is Low Voltage Level
- Latch -Up Performance Exceeds ±200mA Under JESD 78 Standard
- DFN 1.4mm×1.0mm×0.37mm-8L Package
- FOWLP 0.928mm×1.928mm×0.463mm-8B Package

Applications

- I^2C / SMBus
- UART
- GPIO
- Handheld Devices Interface

General Description

AW39112 is a 2-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. It needs two separate power supply rails, with the A ports tracks the V_{CCA} ranging from 1.1 V to 3.6 V, and the B ports tracks the V_{CCB} ranging from 1.65 V to 5.5 V. This makes the chip has capabilities of support both lower and higher logic signal levels translation between any of the 1.2V, 1.8 V, 2.5 V, 3.3 V, and 5 V voltage nodes.

The OE input circuit is supplied by VCCA. Meanwhile, OE is recommended to be tied to GND through an external pull-down resistor to ensure all I/O to be pulled to the supply voltage. No power supply sequencing requirements means either VCCA or VCCB can be powered up first, and OE should be enabled after both VCCA and VCCB are established.

Typical Application Circuit

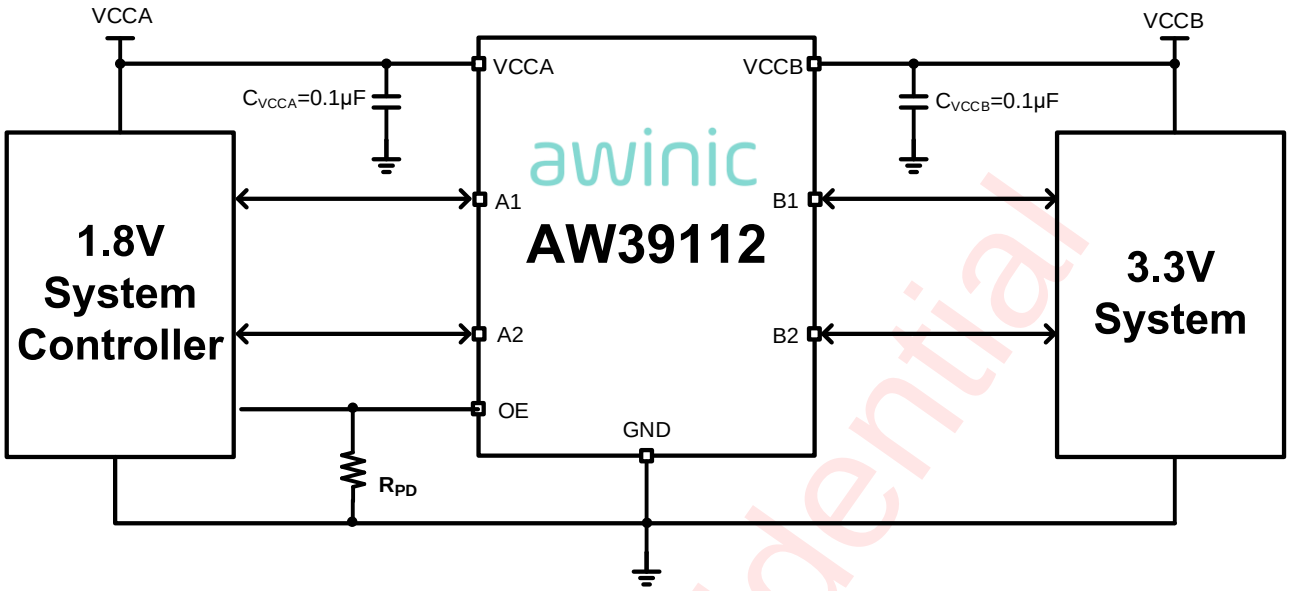


Figure 1 Typical Application Circuit of AW39112

Pin Configuration And Top Mark

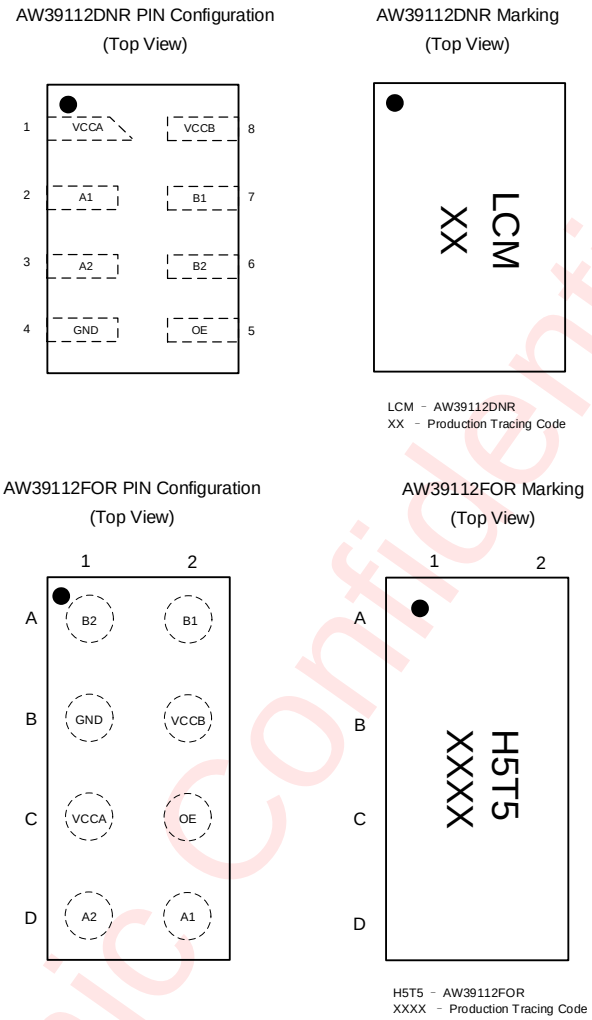


Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin No.		Pin Name	Description
DNR	FOR		
1	C1	VCCA	A-port supply voltage. 1.1V ≤ VCCA ≤ 3.6 V, VCCA ≤ VCCB.
2	D2	A1	Input/output A1.
3	D1	A2	Input/output A2.
4	B1	GND	Ground.
5	C2	OE	Output enable.
6	A1	B2	Input/output B2.
7	A2	B1	Input/output B1.
8	B2	VCCB	B-port supply voltage. 1.65 V ≤ VCCB ≤ 5.5 V.

Functional Block Diagram

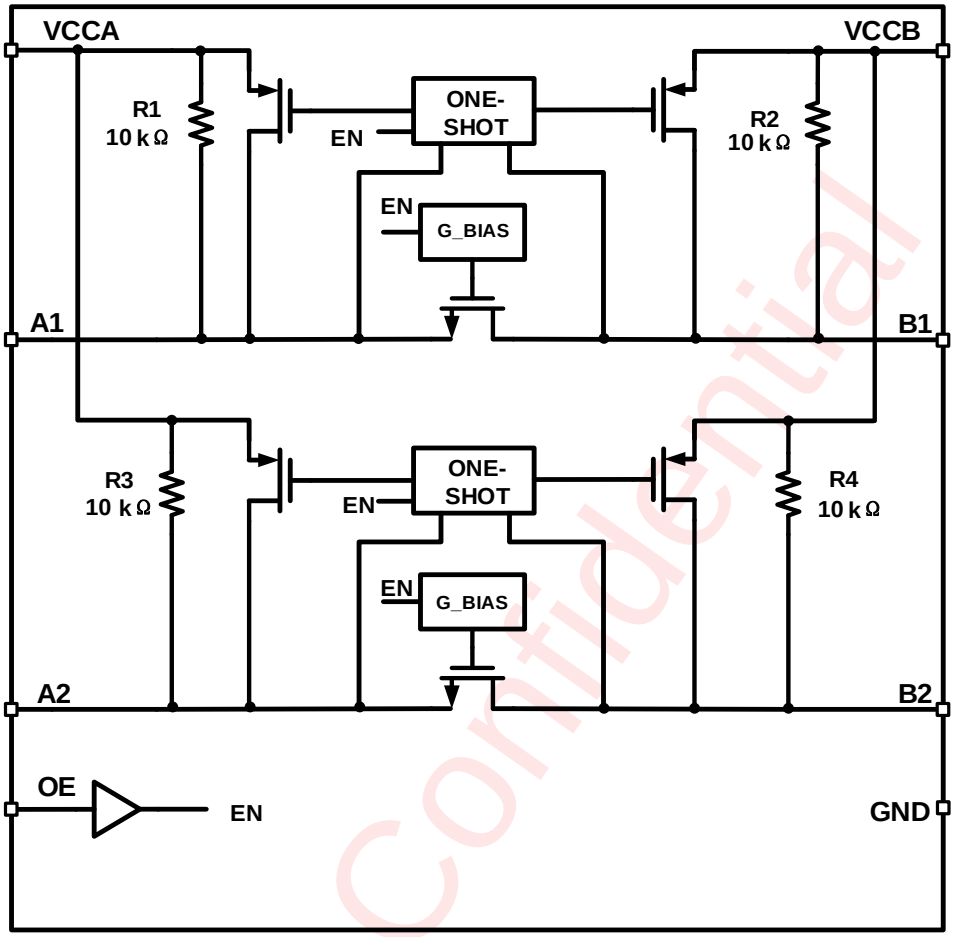


Figure 3 AW39112 Function Block

Typical Application Circuit

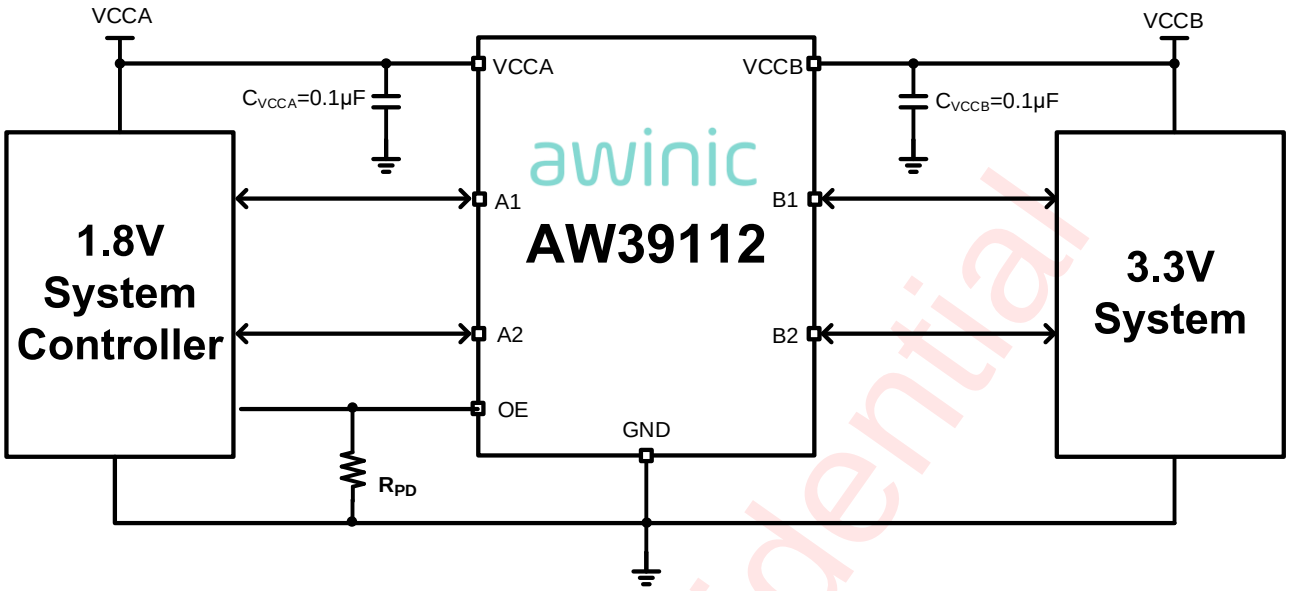


Figure 4 AW39112 Application Circuit

Notice for typical application circuits:

1. In any case, the A/B Ports Voltage cannot be higher than the VCCA/VCCB voltage. Otherwise, the leakage current will flow from A/B Ports to VCCA/VCCB.
2. The device driving the A/B ports must have the driving capacity at least ±1 mA.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW39112DNR	-40°C～85°C	DFN 1.4mm×1.0mm ×0.37mm-8L	LCM	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW39112FOR	-40°C～85°C	FOWLP 0.928mm×1.928mm ×0.463mm-8B	H5T5	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		MIN	MAX	UNIT
Supply voltage range V_{CCA}(NOTE2)		-0.5	5	V
Supply voltage range V_{CCB}(NOTE2)		-0.5	6.5	V
Input voltage range, V_I (NOTE2)	A port	-0.5	5	V
	B port	-0.5	6.5	V
Output voltage range in high or low state, V_O (NOTE2)	A port	-0.5	5	V
	B port	-0.5	6.5	V
Input clamp current, I_{Ik}	V_I<0		-50	mA
Output clamp current, I_{OK}	V_O<0		-50	mA
Operating free-air temperature range		-40	85	°C
Operating junction temperature T_J		-40	125	°C
Storage temperature T_{STG}		-65	150	°C
Lead temperature (Soldering 10 seconds)			260	°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: With respect to GND

ESD Rating And Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 3)	±2	kV
CDM(NOTE 4)	±1.5	kV
Latch-Up(NOTE 5)	+IT: 200 -IT: -200	mA

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

NOTE4: Test method: ESDA/JEDEC JS-002-2018

NOTE5: Test method: JESD78E

Recommended Operating Conditions

VCCI is the VCC associated with the input port.

PARAMETERS		CONDITIONS		MIN	MAX	UNIT
V_{CCA}	Supply voltage for A port			1.1	3.6	V
V_{CCB}	Supply voltage for B port			1.65	5.5	V
V_{IH}	High-level input voltage	A-port	V_{CCA}=1.1V~1.95V V_{CCB}=1.65V~5.5V	V_{CCI}-0.3	V_{CCI}	V
			V_{CCA}=2.3V~3.6V V_{CCB}=1.65V~5.5V	V_{CCI}-0.4	V_{CCI}	V
		B-port	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V	V_{CCI}-0.4	V_{CCI}	V
		OE input	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V	V_{CCA}×0.65	5.5	V
V_{IL}	Low-level input voltage	A-port	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V	0	0.15	V
		B-port	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V	0	0.15	V
		OE input	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V	0	V_{CCA}×0.35	V
Δt/ΔV	Input transition rise or fall rate	A-port (NOTE 6)	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V		10	ns/V
		B-port (NOTE6)	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V		10	ns/V
		Control input	V_{CCA}=1.1V~3.6V V_{CCB}=1.65V~5.5V		10	ns/V
T_A	Operating junction temperature TA			-40	85	°C

NOTE6: The parameter is defined for push-pull driving.

Thermal Information

PARAMETERS	VALUE	UNIT
Junction-to-ambient thermal resistance θ_{JA}	246	°C /W

Electrical Characteristics

DC Electrical Characteristics

Operating under recommended conditions, VCCA ≤ VCCB, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	V_{CCA}(V)	V_{CCB}(V)	MIN	TYP	MAX	UNIT
V_{OHA}	Port A output high voltage	I_{OH}= -20μA, V_{IB}≥V_{CCB}-0.4V	1.1~3.6	1.65~5.5	V_{CCA}×0.67			V
V_{OLA}	Port A output low voltage	I_{OL}=1mA, V_{IB}≤0.15V					0.4	V
V_{OHB}	Port B output high voltage	I_{OH}= -20μA, V_{IA}≥V_{CCA}-0.2V			V_{CCB}×0.67			V
V_{OLB}	Port B output low voltage	I_{OL}=1mA, V_{IA}≤0.15V					0.4	V
I_I	OE input leakage current	V_I=V_{CCI} or GND, T_A=25°C			-1		1	μA
		V_I=V_{CCI} or GND, T_A=-40°C to 85°C			-2		2	μA
I_{OZ}	A or B port output current	OE=V_{IL}, V_I=GND, T_A=-40°C to 85°C			-2		2	μA
		OE=V_{IL}, V_I= V_{CCI}, T_A=-40°C to 85°C			-1		1	μA
I_{CCA}	VCCA supply current	OE=V_{IH}, V_I=V_O=Open, I_O=0, T_A=25°C	1.1~3.6	1.65~5.5			1	μA
			3.6	0			1	μA
			0	5.5			-1	μA
		OE=V_{IH} V_I=V_O=Open, I_O=0, T_A=85°C	3.6	5.5		0.06		μA
			3.6	0		0.05		μA
			0	5.5		-0.01		μA
I_{CCB}	VCCB supply current	OE=V_{IH} V_I=V_O=Open, I_O=0, T_A=25°C	1.1~3.6	1.65~5.5			8	μA
			3.6	0			-1	μA
			0	5.5			1	μA
		OE=V_{IH} V_I=V_O=Open, I_O=0, T_A=85°C	3.6	5.5		2		μA
			3.6	0		-0.01		μA
			0	5.5		0.04		μA
I_{CCB}+ I_{CCA}	Combined supply current	V_I=V_O=Open I_O=0	1.1~3.6	1.65~5.5			9	μA
R_{PU}	Resistor pull-up value	T_A=25°C	1.1~3.6	1.65~5.5	8	10	12	kΩ
R_{NPASS}	The resistor of NMOSFET between A port and B port	OE=V_{IH}, V_I=0.15V I_{source}=10mA, T_A=25°C	1.8	3.3		25		Ω
C_{IO}	Input / Output capacitance	A port: T_A=25°C	3.3	3.3		3.4		pF
		B port: T_A=25°C	3.3	3.3		3.4		pF
C_I	Input capacitance	OE: T_A=25°C	3.3	3.3		1		pF

Timing Requirements *(NOTE1)*

Output load: C_L=15pF, push-pull driver, and T_A=-40°C to 85°C.

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
V_{CCA}=1.1V±0.15V / 2.5V±0.2V / V_{CCA}=3.3V±0.3V					
Data Rate		V_{CCB}=1.8V±0.2V		21	Mbps
		V_{CCB}=3.3V±0.3V		24	
		V_{CCB}=5V±0.5V		24	
t_w	Pulse Duration	V_{CCB}=2.5V±0.2V	45		ns
		V_{CCB}=3.3V±0.3V	40		
		V_{CCB}=5V±0.5V	40		

NOTE1: The parameter's variation is guaranteed by design, not production tested.

Switch Characteristics

Output load: C_L=15pF, T_A=25°C for typical values (unless otherwise noted), V_{CCA}=1.1V

PARAMETER	TEST CONDITION		V_{CCB}=1.65V	V_{CCB}=3.3V	V_{CCB}=5V	UNIT
			TYP	TYP	TYP	
t_{PHL} *(NOTE2)*	A to B	Push-pull	12	17.9	23.5	ns
		Open-drain	8.6	13.5	18.8	
t_{PLH} *(NOTE2)*	A to B	Push-pull	18.8	15.7	15.2	ns
		Open-drain	27.3	26.4	19.4	
t_{PHL} *(NOTE2)*	B to A	Push-pull	3.6	3.2	2.8	ns
		Open-drain	4.7	3.5	3.7	
t_{PLH} *(NOTE2)*	B to A	Push-pull	8.7	2.7	1.8	ns
		Open-drain	0.5	0.8	0.8	
t_{en} Enable time	OE to A or B		31	14.8	12.8	ns
t_{dis} disable time	OE to A or B		139.8	161	97	ns
t_{rA} output rise time	A port rise time	Push-pull	24.3	15.3	8.9	ns
		Open-drain	162.4	106.3	76.2	
t_{rB} output rise time	B port rise time	Push-pull	35.6	24.2	17.1	ns
		Open-drain	141.2	65.5	30.9	
t_{fA} output fall time	A port fall time	Push-pull	6.4	5.3	3.1	ns
		Open-drain	5.6	4.6	4.2	
t_{fB} output fall time	B port fall time	Push-pull	15	25.8	37.5	ns
		Open-drain	12.3	21.8	31.4	
t_{SK} Skew time output	Channel to channel skew		4.9	4.7	4.3	ns

Output load: C_L=15pF, T_A=25°C for typical values (unless otherwise noted), V_{CCA}=1.8V.

PARAMETER	TEST CONDITION		V_{CCB}=1.8V	V_{CCB}=3.3V	V_{CCB}=5V	UNIT
			TYP	TYP	TYP	
t_{PHL} *(NOTE2)*	A to B	Push-pull	1.4	2.3	3.2	ns
		Open-drain	3.6	4	4.7	
t_{PLH} *(NOTE2)*	A to B	Push-pull	2.1	3.2	3.3	ns
		Open-drain	0.1	0.2	0.3	
t_{PHL} *(NOTE2)*	B to A	Push-pull	3.1	2.3	1.8	ns

PARAMETER	TEST CONDITION		V_{CCB}=1.8V	V_{CCB}=3.3V	V_{CCB}=5V	UNIT
			TYP	TYP	TYP	
		Open-drain	2.4	1.9	2	
t_{PLH}(NOTE2)	B to A	Push-pull	4	2.3	1.7	ns
		Open-drain	0.19	0.28	0.38	
t_{en} Enable time	OE to A or B		21	10.7	7.2	ns
t_{dis} disable time	OE to A or B		138	152.7	156.5	ns
t_{rA} output rise time	A port rise time	Push-pull	10.2	4.5	4.1	ns
		Open-drain	118.4	77.3	56.2	
t_{rB} output rise time	B port rise time	Push-pull	8.2	5.6	4.7	ns
		Open-drain	125.3	60.3	29.4	
t_{fA} output fall time	A port fall time	Push-pull	5.9	2.5	1.4	ns
		Open-drain	4.5	3.9	3.5	
t_{fB} output fall time	B port fall time	Push-pull	3.7	4.2	5.4	ns
		Open-drain	6.6	6.8	7.7	
t_{SK} Skew time output	Channel to channel skew		0.8	0.7	0.7	ns

Output load: C_L=15pF, T_A=25°C for typical values (unless otherwise noted), VCCA=2.5V

PARAMETER	TEST CONDITION		V_{CCB}=2.5V	V_{CCB}=3.3V	V_{CCB}=5V	UNIT
			TYP	TYP	TYP	
t_{PHL}(NOTE2)	A to B	Push-pull	1.6	1.7	1.9	ns
		Open-drain	1.8	2	2.8	
t_{PLH}(NOTE2)	A to B	Push-pull	1.7	2.2	2.4	ns
		Open-drain	0.1	0.1	0.2	
t_{PHL}(NOTE2)	B to A	Push-pull	2	1.8	1.6	ns
		Open-drain	1	1.3	1.3	
t_{PLH}(NOTE2)	B to A	Push-pull	2.2	1.7	1.4	ns
		Open-drain	0.1	0.1	0.2	
t_{en} Enable time	OE to A or B		11.6	9.1	7.3	ns
t_{dis} disable time	OE to A or B		143.4	152.4	154.9	ns
t_{rA}output rise time	A port rise time	Push-pull	4.4	3.7	2.9	ns
		Open-drain	88.7	74.1	54.5	
t_{rB} output rise time	B port rise time	Push-pull	4.6	4.1	3.6	ns
		Open-drain	91.8	67.1	37.2	
t_{fA} output fall time	A port fall time	Push-pull	2.9	2.6	2.4	ns
		Open-drain	3.8	3.3	2.6	
t_{fB} output fall time	B port fall time	Push-pull	2.7	3.2	3.4	ns
		Open-drain	3.8	4	5.1	
t_{SK} Skew time output	Channel to channel skew		0.8	0.8	0.9	ns

Output load: C_L=15pF, T_A=25°C for typical values (unless otherwise noted), VCCA=3.3V

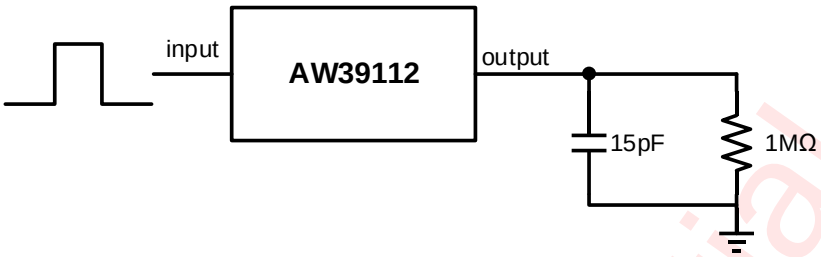
PARAMETER	TEST CONDITION		V_{CCB}=3.3V	V_{CCB}=5V	UNIT
			TYP	TYP	
t_{PHL}(NOTE2)	A to B	Push-pull	1	1.5	ns
		Open-drain	0.9	1.4	

PARAMETER	TEST CONDITION		V_{CCB}=3.3V	V_{CCB}=5V	UNIT
			TYP	TYP	
t_{PLH} (NOTE2)	A to B	Push-pull	1.7	1.8	ns
		Open-drain	0.1	0.2	
t_{PHL} (NOTE2)	B to A	Push-pull	1.7	1.6	ns
		Open-drain	0.5	1.2	
t_{PLH} (NOTE2)	B to A	Push-pull	1.8	1.4	ns
		Open-drain	0.1	-0.1	
t_{en} Enable time	OE to A or B		7.9	6.9	ns
t_{dis} disable time	OE to A or B		148.1	159.7	ns
t_{rA} output rise time	A port rise time	Push-pull	3.3	2.8	ns
		Open-drain	69.3	51.8	
t_{rB} output rise time	B port rise time	Push-pull	3.7	3.3	ns
		Open-drain	72.6	43.1	
t_{fA} output fall time	A port fall time	Push-pull	2.6	2.4	ns
		Open-drain	3.4	3.1	
t_{fB} output fall time	B port fall time	Push-pull	2.5	2.8	ns
		Open-drain	3.4	3.6	
t_{SK} Skew time output	Channel to channel skew		1.2	1.1	ns

NOTE2: t_{PHL} presents propagation delay from high to low, and t_{PLH} presents propagation delay from low to high.

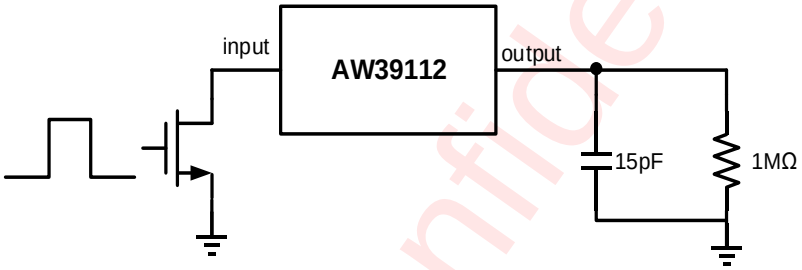
Typical Characteristics

Test Information



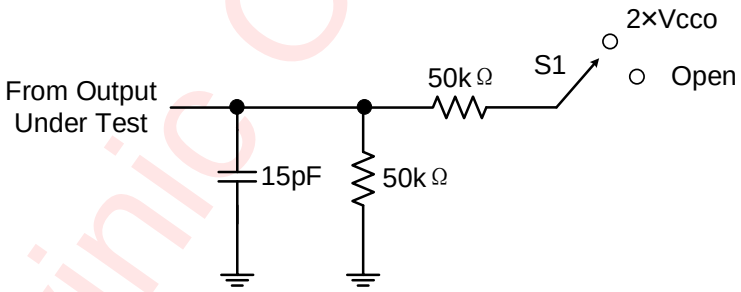
Test Circuit for Date Rate, Pulse Duration, Propagation Delay, Rise Time and Fall Time

Figure 5 Load Circuit of Push-Pull Driver



Test Circuit for Date Rate, Pulse Duration, Propagation Delay, Rise Time and Fall Time

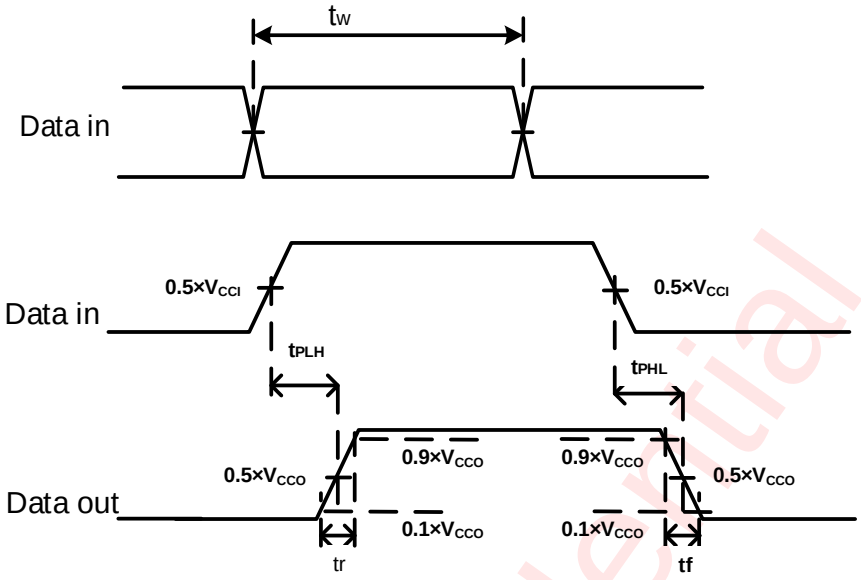
Figure 6 Load Circuit of Open-Drain Driver



TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{cco}$
t_{PHZ}/t_{PZH}	Open

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. VCCI is the VCC associated with the input port.
4. VCCO is the VCC associated with the output port.
5. The resistance and Capacitance values at output notes above are the total effective values.

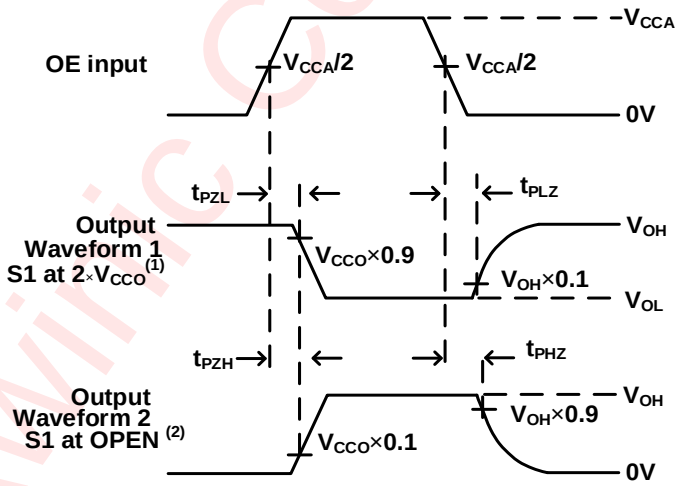
Figure 7 Load Circuit for Enable-Time and Disable-Time Measurement



The input pulses should have the following characteristics:

1. f_{IN} ≤10MHz.
2. dv/dt ≥ 1V/ns.

Figure 8 Timing Parameter Definition

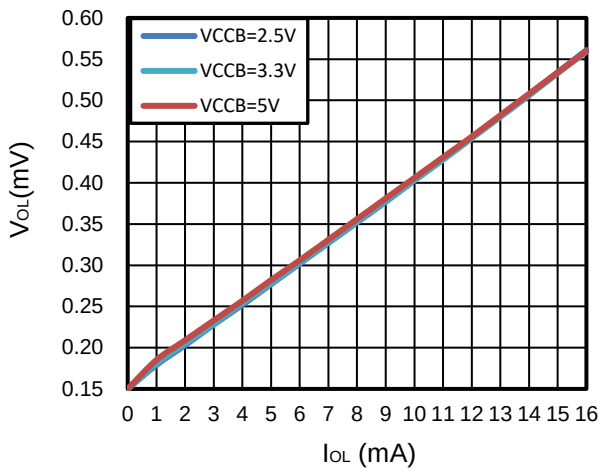


(1) The Waveform 1 is obtained under the condition that the input is low and S1 at 2*V_{CCO}.

(2) The Waveform 2 is obtained under the condition that the input and S1 at OPEN.

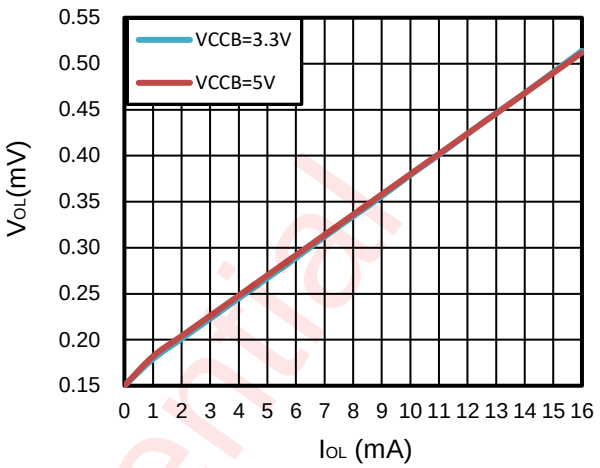
Figure 9 Enable and Disable Times

Typical Curve T_A=25°C



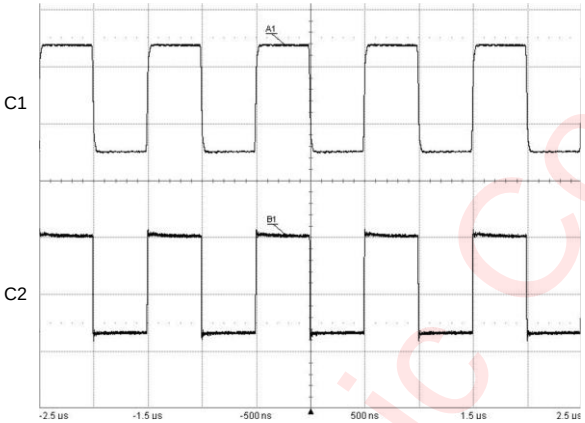
V_{CCA}=1.8V, OE=1, V_{ILA}=0.15V

Figure 10 Low-Level Output Voltage vs Low-Level Current



V_{CCA}=3.3V, OE=1, V_{ILA}=0.15V

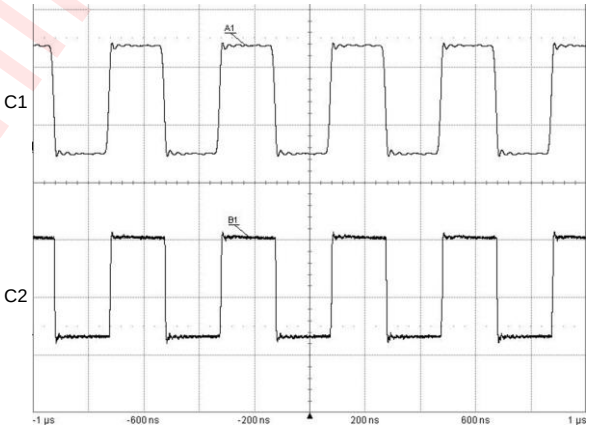
Figure 11 Low-Level Output Voltage vs Low-Level Current



C1: 1.00V/div C2: 2.00V/div

V_{CCA}=1.8V, V_{CCB}=3.3V, OE=1, Push-Pull Driver
Signal is translated from A port to B port

Figure 12 Level Translation of a 1MHz Signal



C1: 1.00V/div C2: 2.00V/div

V_{CCA}=1.8V, V_{CCB}=3.3V, OE=1, Push-Pull Driver
Signal is translated from A port to B port

Figure 13 Level Translation of a 2.5MHz Signal

Detailed Functional Description

AW39112 is a 2-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. Port A can support I/O voltages from 1.1 V to 3.6 V, while Port B is able to support I/O voltage range from 1.65 V to 5.5 V. The chip uses a transmission gate architecture with an rising edge rate accelerator (one-shot), to increase overall data rate. Also, 10kΩ pull-up resistors are integrated in the chip, which ensures the chip not only supports push-pull applications but also can be used in open-drain applications directly.

One-shot Accelerator

The One-Shot rising edge accelerator circuit speeds up the rising edge to help increasing the chip's data rate. Once the chip has detected the rising edge of the input signal from low to high, the one-shot circuit generates a pulse signal of approximately 30ns, which enables the internal pull-up PMOS transistor between power supply and output, thereby accelerating the output port from low to high. During this acceleration phase, the output resistance of the driver is reduced from 10kΩ to approximately 60Ω. While detecting the output has been turned up, the one-shot pulse signal is finished and pull-up PMOS transistor is quickly turned off. This architecture reduces the average dynamic power consumption of the chip while allowing it to meet different drive requirements.

Gate Bias

For the bidirectional voltage translator AW39112, a NMOS switch transistor is used between the input and output. When translating high level, the NMOS transistor is turned off, and the input and output terminals are isolated so that they do not impact each other. When the low level is translated, the NMOS switch transistor is fully turned on, so that the output terminal can be quickly pulled down to the low voltage level. Therefore, the gate bias voltage of the NMOS switch transistor is set to a fixed value about VCCA+VTH. It is also because of this architecture that VCCA≤VCCB needs to be guaranteed in the applications.

Enable Control

The AW39112's OE pin can disable the chip by setting OE to low voltage level, allowing all I/O to be pulled to the supply voltage through a 5MΩ internal pull-up resistor. The disable time (t_{dis}) represents the delay time from OE going low to the chip turns to OFF-state. And the enable time (t_{en}) indicates the delay time from OE going high to the chip working in translation state. Meanwhile, OE is recommended to be tied to GND through an external pull-down resistor to ensure the ultra-low power-supply quiescent current. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Input Driver

The rising edge time of the signal (t_{rA}, t_{rB}) and propagation delay time from low to high (t_{PLH}) are determined by the rising edge rate of the input signal, the ONE-SHOT accelerator's pull-up capability, and the capacitive load of the port. The falling edge time of the signal (t_{fA}, t_{fB}) depends on the falling edge rate of the input signal, the output impedance of the external driver, and the capacitive load on the data line. Similarly, t_{PHL} and the maximum data rate also depend on the output impedance of the external driver. So, the test conditions for t_{rA}, t_{rB}, t_{fA}, t_{fB}, t_{PLH}, t_{PHL} and maximum data rate in the data sheet are that the output impedance of the external driver is less than 50Ω.

Output Load

It is recommended that a PCB layout with short PCB layout length:

1. Avoid excessive capacitive load triggers ONE-SHOT circuit falsely;
2. It can ensure that the round trip delay of any reflection is less than a single ONE-SHOT duration;
3. Improve signal integrity.

Meanwhile, the pulse width of the ONE-SHOT circuit is approximately 30 ns, which determines the maximum output load capacitance that the chip can drive. For very heavy output capacitive loads, the one-shot accelerator will time-out before the output is fully pulled to high level, at which case the signal transmission will be distorted. So the ONE-SHOT duration design requires a trade-off between dynamic power consumption, capacitive load driving capability and maximum data rate. The signal tw at the maximum translation rate should be greater than the maximum pulse width of the ONE-SHOT circuit, and the delay caused by the output capacitive load should be less than the maximum pulse width of the ONE-SHOT circuit.

Application Information

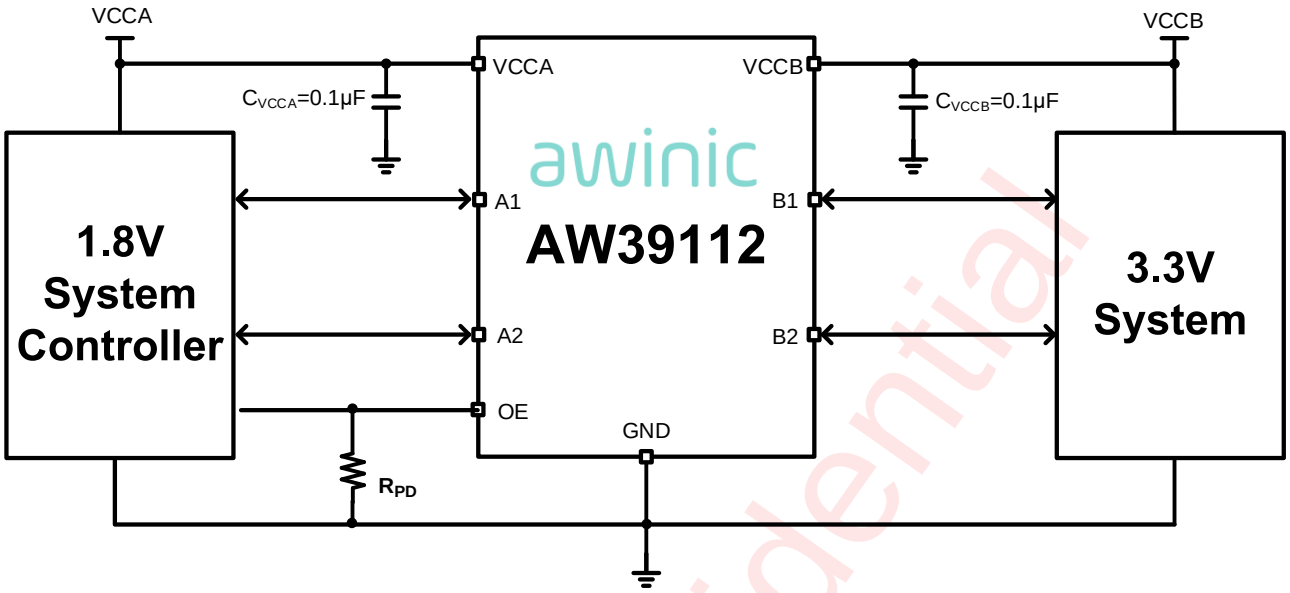


Figure 14 AW39112 Application Circuit

AW39112 is a 2-bit voltage-level translator without direction control signal, which is suitable for interfacing devices or systems operating at different interface voltages with one another. Port A can supports I/O voltages from 1.1 V to 3.6 V, while Port B is able to support I/O voltage range from 1.65 V to 5.5 V. Also, 10kΩ pull-up resistors are integrated in the chip, which ensures the chip not only supports push-pull applications but also can be used in open-drain applications directly.

VCC Capacitor Selection

The device is a 2-bit high-performance voltage-level translator that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, recommend 0.1μF or larger than 0.1μF.

R_{PD} Selection

Driving OE pin HIGH to enable the device. If the voltage level of OE pin is low, all I/O are pulled to the supply voltage through a 5MΩ internal pull-up resistor. OE is recommended to be tied to GND through an external pull-down resistor to ensure the ultra-low power-supply quiescent current. OE pin is high impedance without internal pull down resistor, customer can choose the resistor value based on the source drive capability and current consumption.

PCB Layout Consideration

1. Maintain the integrity of the ground plane and avoid being divided by routing signal lines or power lines on the complete ground plane.
2. The input capacitor of the power supply should be close to the pin of the chip to achieve the best filtering effect. The distance between the input capacitor and the pin of the chip is recommended not to exceed 3mm.
3. In order to maintain the integrity of the transmission signal, the length of the signal transmission line should be as short as possible, parallel routing should be avoided when the signal transmission line is routed across layers, and the input and output paths of the signal should be as symmetrical as possible.

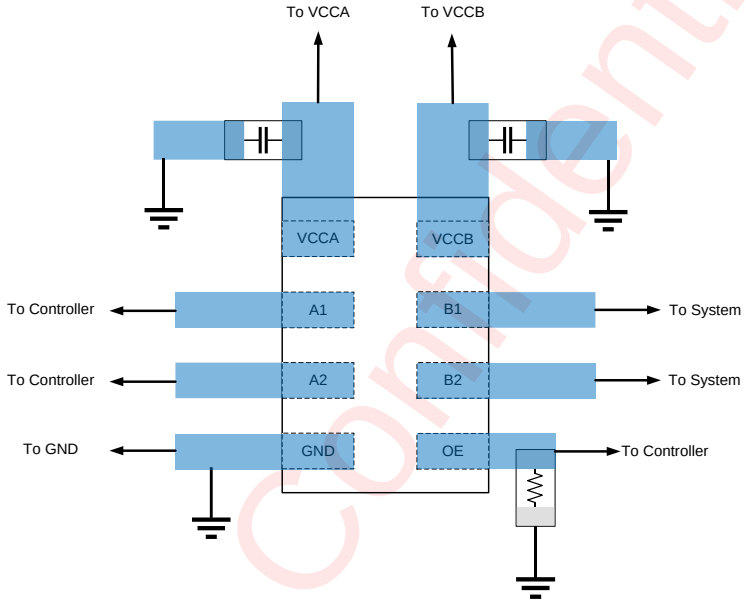


Figure 15 AW39112DNR Layout Example

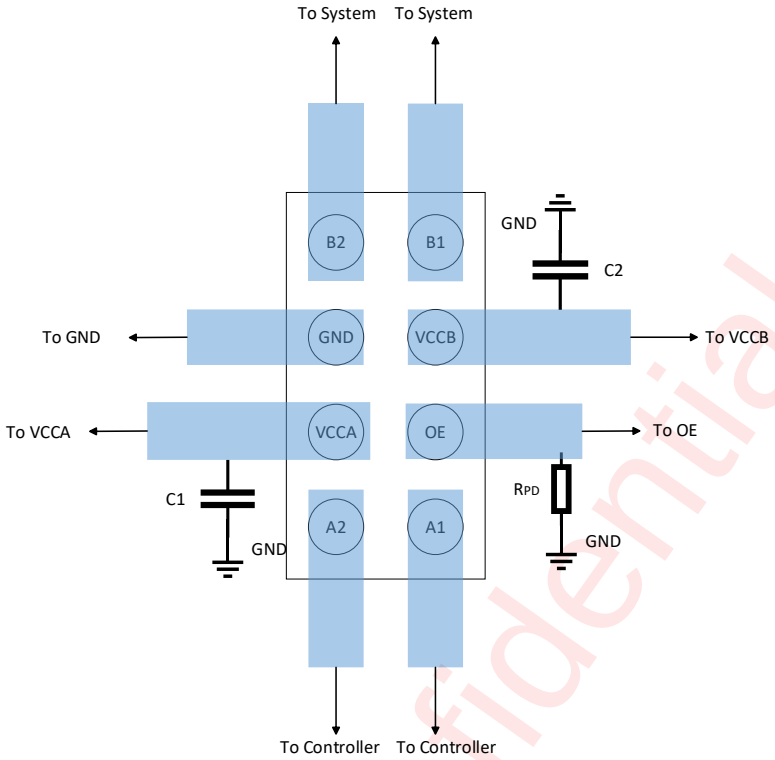
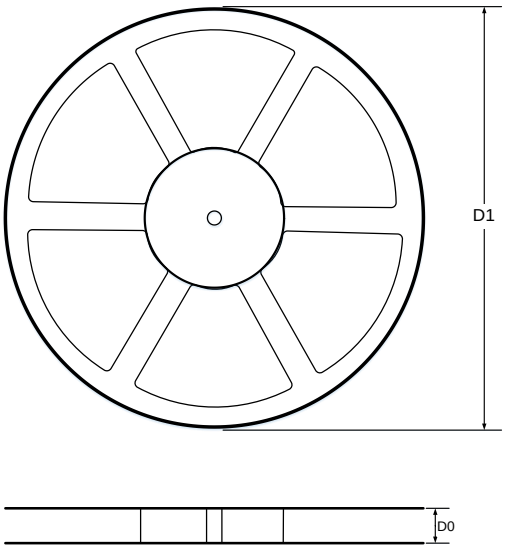


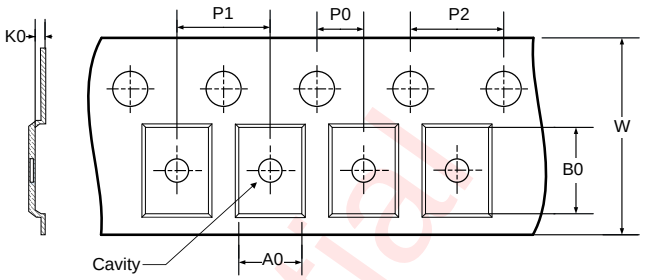
Figure 16 AW39112FOR Layout Example

Tape And Reel Information (DFN)

REEL DIMENSIONS

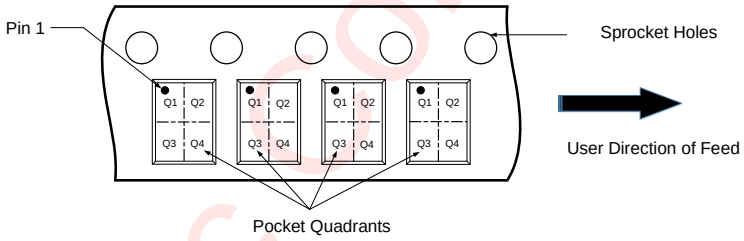


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



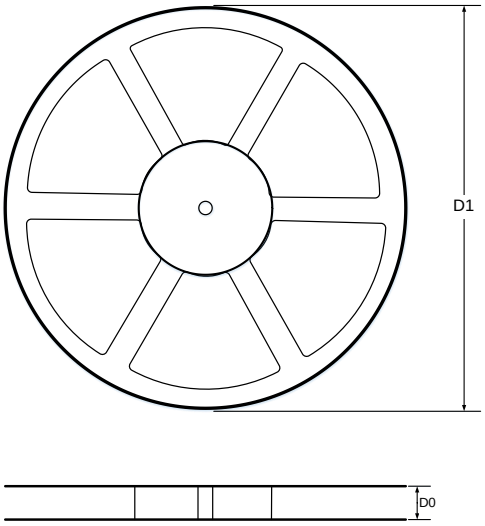
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

All Dimensions are nominal

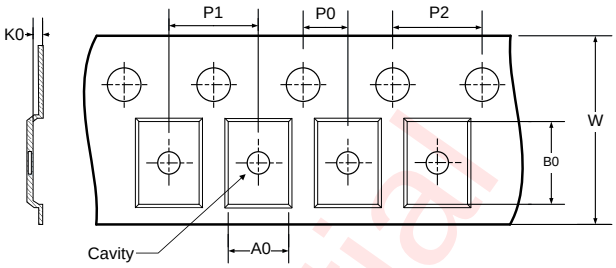
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.2	1.6	0.5	2	4	4	8	Q1

Tape And Reel Information (FOR)

REEL DIMENSIONS

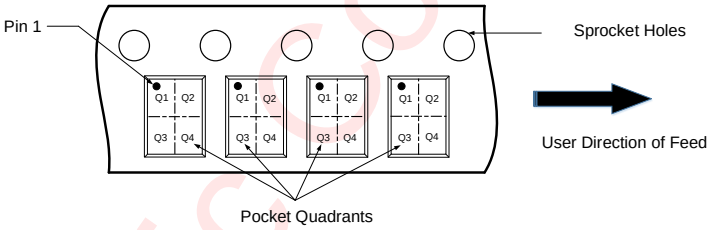


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

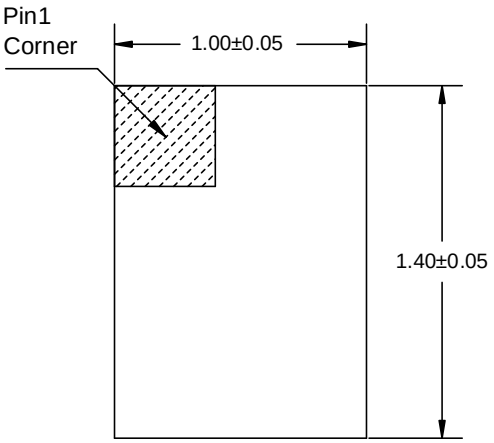


Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

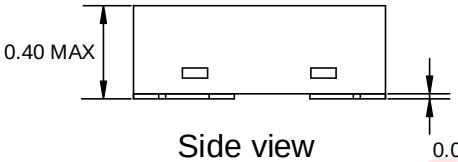
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.03	2.03	0.58	2.00	4.00	4.00	8.00	Q1

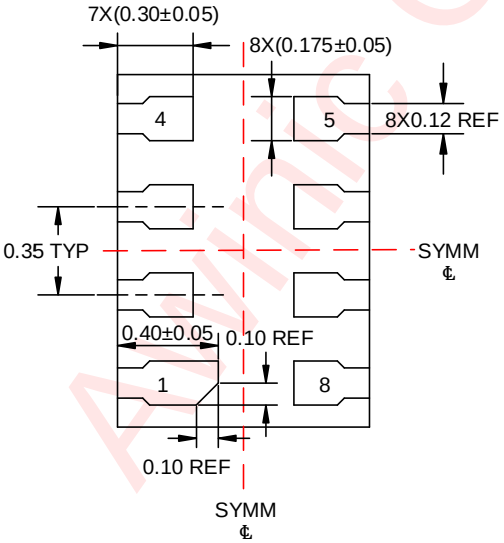
Package Description (DFN)



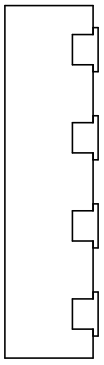
Top view



Side view



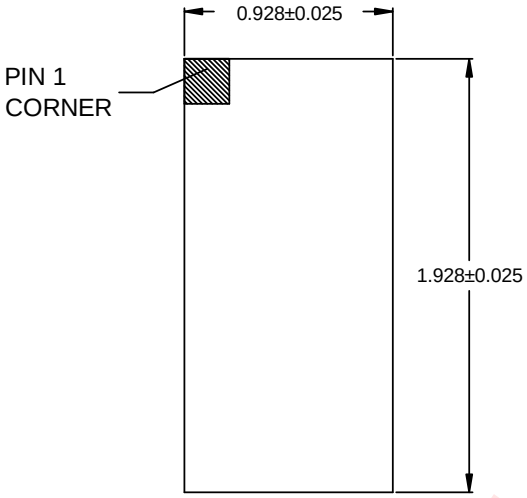
Bottom view



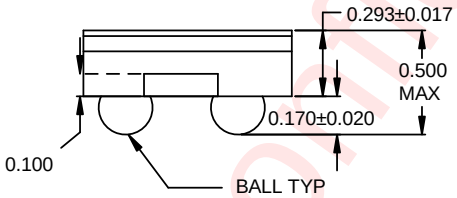
Side view

Unit: mm

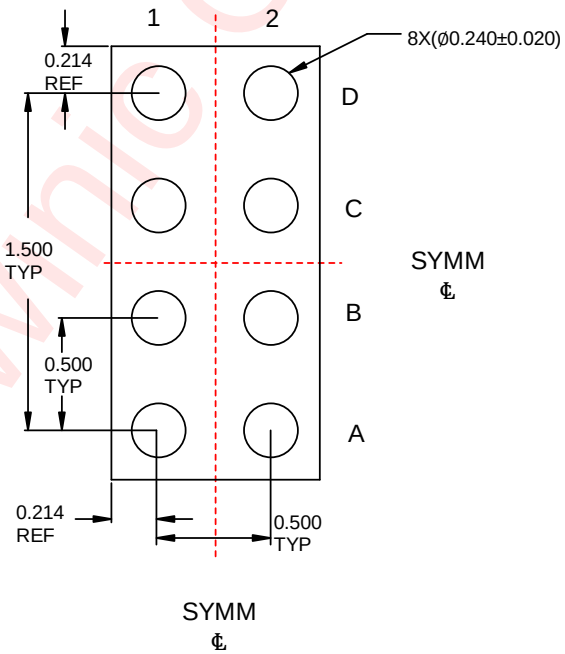
Package Description (FOR)



Top View



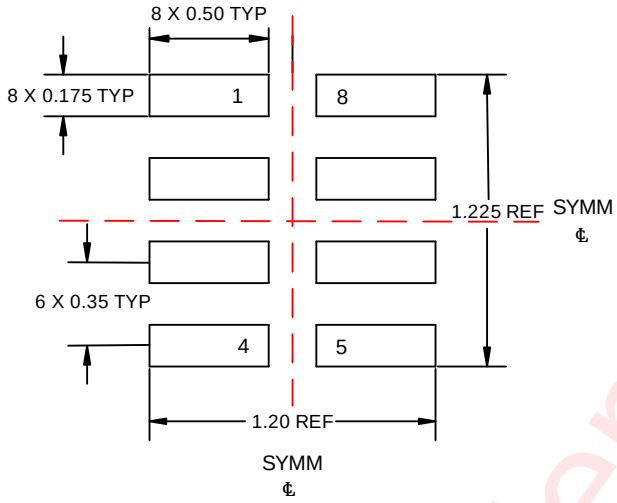
Side View

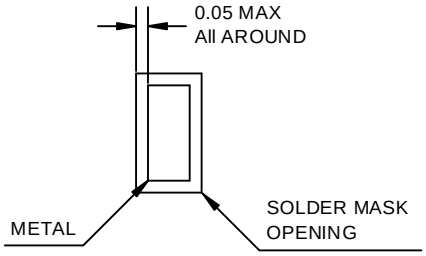


Bottom View

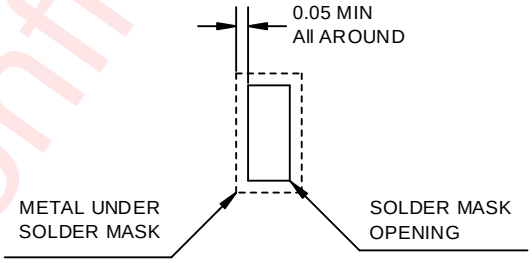
Unit: mm

Land Pattern Data (DFN)





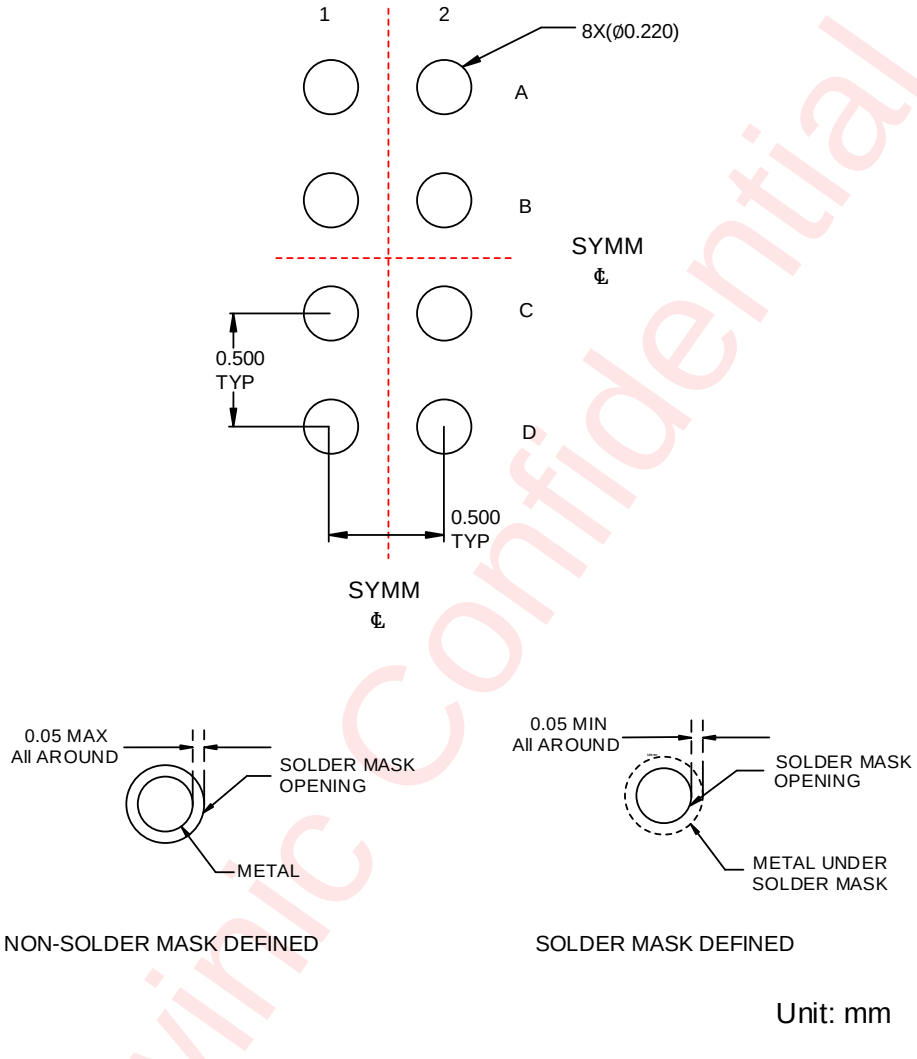
NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Land Pattern Data (FOR)



Unit: mm

Revision History

Version	Date	Change Record
V1.0	Feb. 2021	Official Released
V1.1	Nov. 2021	1. Modified the test condition of R_{NPASS}(Page 8) 2. Modified the test condition of V_{OHA} and V_{OHB} in DC Electrical Characteristics (Page 8) 3. Added I_{IK} and I_{OK} in Absolute Maximum Ratings(Page 6) 4. Modified Package description(POD) (FOR) (Page 23)
V1.2	Apr. 2022	1. Changed the value of V_{IH} for A port (Page 7) 2. Modified some formats
V1.3	Jul. 2022	1. Modified some formats 2. Added PCB layout consideration (Page 18)
V1.4	Aug. 2023	1. Update the dimensioning method (Page 22)
V1.5	Apr. 2025	1. Update Package Description (DFN) (Page 22)

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