1.5A Ultra-small Load Switch with Slew Rate Control

Features

- Integrated P-channel MOSFET load switch
- Input voltage: 1V to 5.5V
- 1.5A maximum continuous switch current
- Switch on-resistance(typ.):
  Rdson=52mΩ at VIN=5.5V
  Rdson=57mΩ at VIN=4.2V
  Rdson=64mΩ at VIN=3.3V
  Rdson=76mΩ at VIN=2.5V
  Rdson=100mΩ at VIN=1.8V
  Rdson=164mΩ at VIN=1.2V
  Rdson=230mΩ at VIN=1V
- Controlled slew rate to limit inrush currents
- Ultra-low shutdown current
- Internal EN pull-down resistor
- Quick Output Discharge(QOD)
- Full time Reverse Current Protection (RCP) for AW35113S
- WLCSP 0.618mm×0.618mm-4B package

Applications

Smartphones and Tablets
Portable Devices
Wearables

General Description

The AW35111S/AW35113S integrates a 64mΩ (typ.) P-channel MOSFET, which can operate over a wide input range of 1V to 5.5V. The AW35111S/AW35113S features output slew rate control, limiting inrush currents during turn-on to protect downstream devices.

In addition, AW35111S/AW35113S has QOD function which can prevent the output from floating when the switch is disabled.

There is a Reverse Current Protection(RCP) function for AW35113S when V_{OUT} is 33mV(typ.) greater than V_{IN}, which can prevent the current to flowing through the P-FET or the body diode.

The AW35111SCSR/AW35113SCSR is available in WLCSP 0.618mm×0.618mm-4B package.

Typical Application Circuit

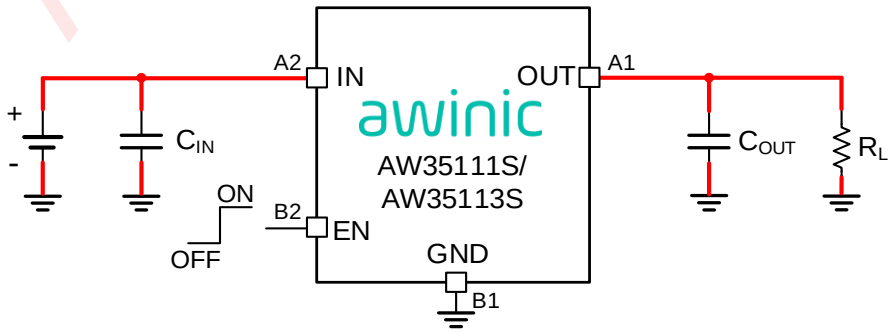


Figure 1 Typical Application Circuit of AW35111S/AW35113S

Pin Configuration And Top Mark

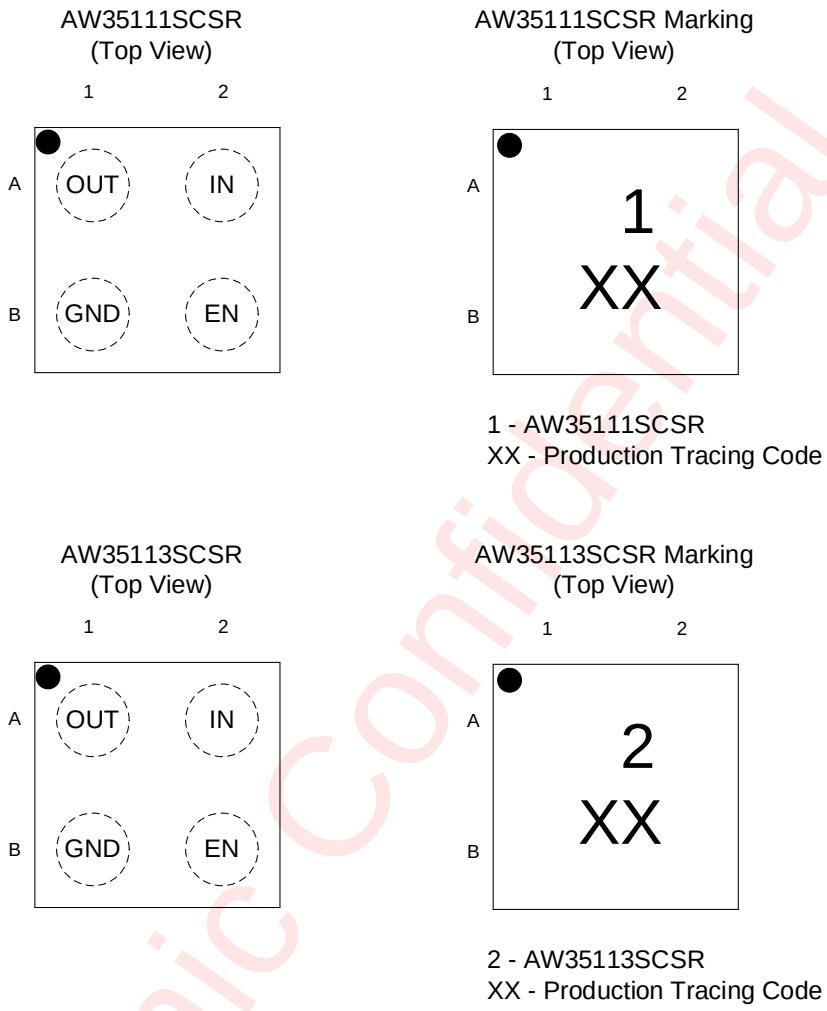


Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
A1	OUT	Switch output
A2	IN	Switch input and power supply
B1	GND	Device ground
B2	EN	Switch control input, active high, internal 7.2MΩ pull down resistor

Functional Block Diagram

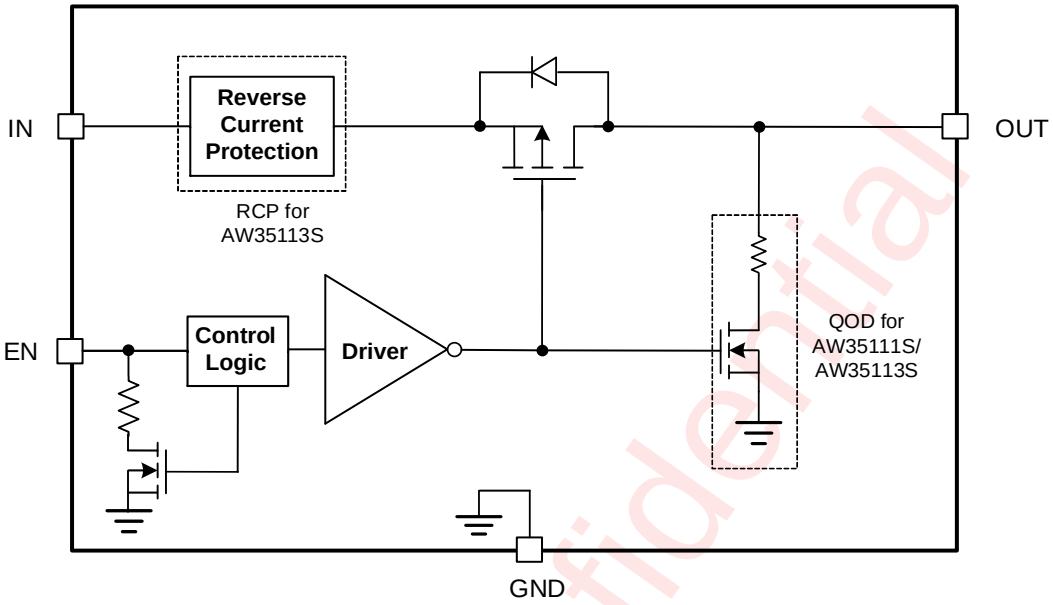


Figure 3 Functional Block Diagram

Typical Application Circuits

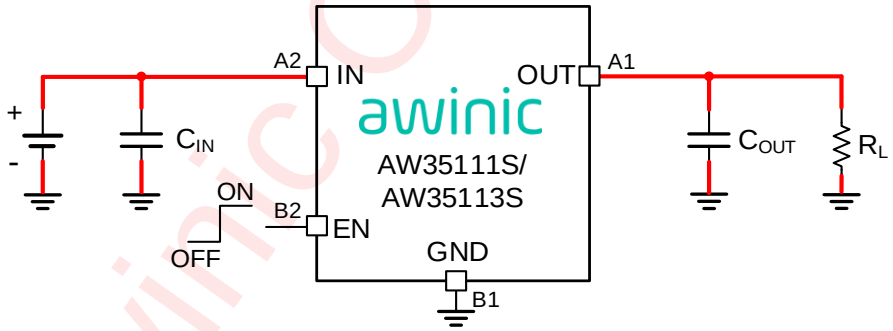


Figure 4 Typical Application Circuit of AW35111S/AW35113S

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35111SCSR	-40°C ~ 85°C	WLCSP 0.618mm×0.618mm-4B	1	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW35113SCSR	-40°C ~ 85°C	WLCSP 0.618mm×0.618mm-4B	2	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 6V
Enable Voltage Range	EN	-0.3V to 6V
Output Voltage Range	OUT	-0.3V to 6V
Maximum Continuous Switch Current V_{IN} ≥ 1.5V		1.5A
Maximum Continuous Switch Current for 1.2V ≤ V_{IN} < 1.5V(NOTE 2)		1A
Maximum Continuous Switch Current for 1V ≤ V_{IN} < 1.2V(NOTE 2)		0.5A
Maximum Peak Switch Current for V_{IN} ≥ 2.5V(NOTE 3)		2A
Operating Free-air Temperature Range		-40°C to 85°C
P_D (Power Dissipation) at T_A=25°C		0.81W
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD		
HBM (Human Body Model) (NOTE 4)		±2kV
CDM(Charged Device Model) (NOTE 5)		±1.5kV
Latch-Up		
Latch-Up (NOTE 6)		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

NOTE3: Limited by thermal design, and tested in 10ms width pulse current.

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2024.

NOTE5: All pins. Test Condition: ANSI/ESDA/JEDEC JS-002-2022.

NOTE6: Test Condition: JESD78F.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	1		5.5	V
V_{EN}	EN Voltage	0		5.5	V
V_{OUT}	Output Voltage	0		V_{IN}	V
C_{IN}	Input capacitance	0.1	1		μF
C_{OUT}	Output load capacitance(NOTE7)	0.1	1		μF

NOTE7: The Output load capacitance is the nominal value.

Electrical Characteristics

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 3.3V, C_{IN} = 1μF, I_{IN}≤ 1.5A.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
INPUT CURRENTS							
I_Q	Input quiescent current	AW35111S	V_{IN}=V_{EN}=3.3V, I_{OUT}=0A, T_A=25°C		2		nA
			V_{IN}=V_{EN}=3.3V, I_{OUT}=0A, T_A=85°C		8		nA
			V_{IN}=V_{EN}=5.5V, I_{OUT}=0A, T_A=25°C		3		nA
			V_{IN}=V_{EN}=5.5V, I_{OUT}=0A, T_A=85°C		15		nA
		AW35113S	V_{IN}=V_{EN}=3.3V, I_{OUT}=0A, T_A=25°C		350		nA
			V_{IN}=V_{EN}=3.3V, I_{OUT}=0A, T_A=85°C		400		nA
			V_{IN}=V_{EN}=5.5V, I_{OUT}=0A, T_A=25°C		610		nA
			V_{IN}=V_{EN}=5.5V, I_{OUT}=0A, T_A=85°C		730		nA
I_{SD}	Shutdown current from IN to GND	AW35111S	V_{IN}=3.3V, V_{EN}=0V, T_A=25°C		16		nA
			V_{IN}=3.3V, V_{EN}=0V, T_A=85°C		1000		nA
			V_{IN}=5.5V, V_{EN}=0V, T_A=25°C		35		nA
			V_{IN}=5.5V, V_{EN}=0V, T_A=85°C		1650		nA
		AW35113S	V_{IN}=3.3V, V_{EN}=0V, T_A=25°C		275		nA
			V_{IN}=3.3V, V_{EN}=0V, T_A=85°C		750		nA
			V_{IN}=5.5V, V_{EN}=0V, T_A=25°C		500		nA
			V_{IN}=5.5V, V_{EN}=0V, T_A=85°C		1550		nA
POWER SWITCH							
I_{LEAKEN}	EN pin leakage current	V_{IN}=0V, V_{EN}=5.5V			700	1000	nA
R_{EN}	EN pin pull down resistor	V_{IN}=5V, V_{EN}=0.4V			7.2		MΩ
R_{DIS}	Output discharge resistance	V_{IN}=5.0V, EN disable, I_{OUT} Sinking 2mA			88		Ω
R_{dson}	Internal switch MOSFET on-state resistance	V_{IN}=5.5V, I_{OUT}=0.2A, T_A=25°C			52		mΩ
		V_{IN}=3.3V, I_{OUT}=0.2A, T_A=25°C			64		
		V_{IN}=1.8V, I_{OUT}=0.2A, T_A=25°C			100		
		V_{IN}=1.2V, I_{OUT}=0.2A, T_A=25°C			164		
		V_{IN}=1V, I_{OUT}=0.2A, T_A=25°C			230		

Electrical Characteristics(Continues)

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 3.3V, C_{IN} = 1μF, I_{IN}≤ 1.5A.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
POWER SWITCH							
t_R	Output rise time	V_{IN}=3.3V, C_{OUT}=0.1μF, R_{OUT}=10Ω for AW35111S V_{IN}=3.3V, C_{OUT}=1μF, R_{OUT}=30Ω for AW35113S	AW35111S		84		μs
			AW35113S		274		
t_{ON}	Switch turn on time		AW35111S		90		μs
			AW35113S		285		
t_{EN}	Enable time		AW35111S		50		μs
			AW35113S		160		
t_F	Output fall time		AW35111S		2		μs
			AW35113S		53		
t_{OFF}	Switch turn off time		AW35111S		2.5		μs
			AW35113S		13		
V_{IH}	EN input high threshold level			1			V
V_{IL}	EN input low threshold level					0.4	V
REVERSE CURRENT PROTECTION (RCP for AW35113S)							
V_{REV}	Reverse current voltage threshold	V_{IN}=3.3V, C_{OUT}=1μF			33		mV
V_{REV_HYS}	Reverse current voltage hysteresis	V_{IN}=3.3V, C_{OUT}=1μF			27		mV
I_{REV_ACT}	Reverse activation current	V_{IN}=3.3V, C_{OUT}=1μF, V_{OUT} > V_{IN}			0.5		A
I_{REV_PRO}	Reverse protection current	V_{OUT} - V_{IN} > V_{REV}			7.5		μA

Timing Diagram

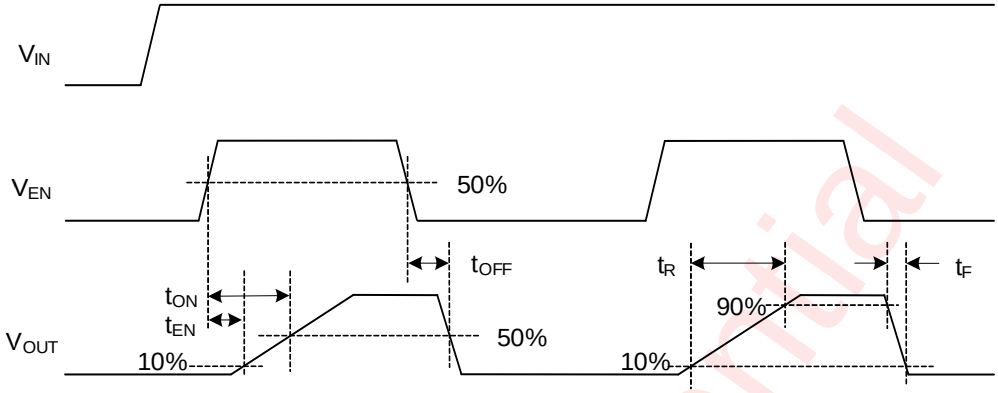


Figure 5 AW35111S/AW35113S Timing Diagram

Typical Characteristics

Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.

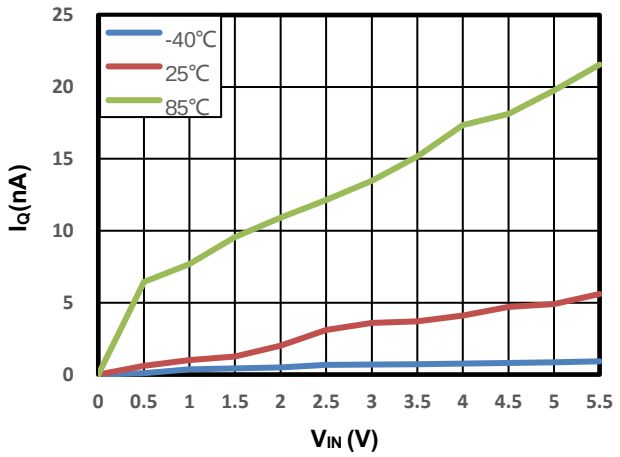


Figure 6 Quiescent Current vs. V_{IN}, No load (AW35111S)

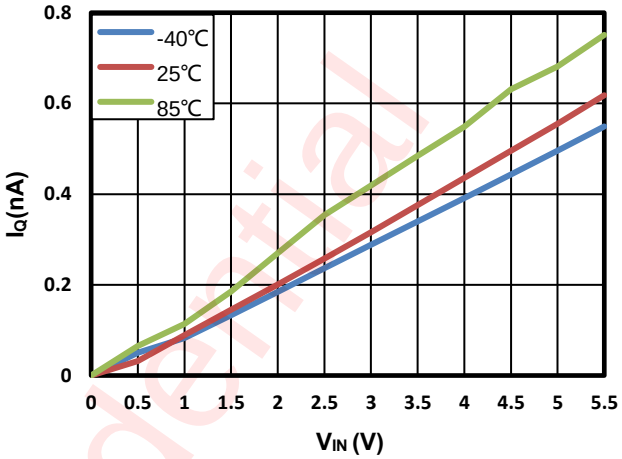


Figure 7 Quiescent Current vs. V_{IN} (AW35113S)

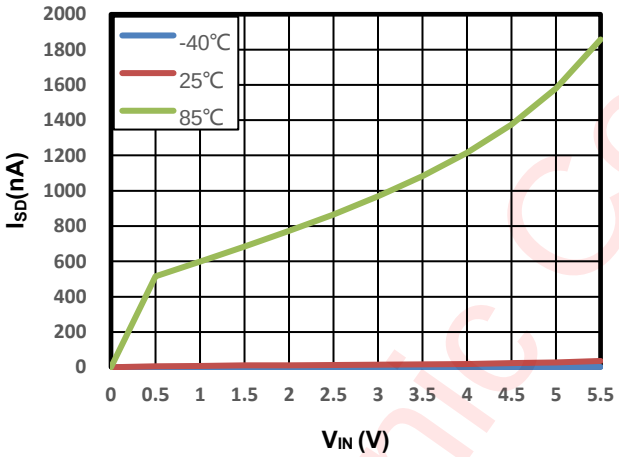


Figure 8 IN Shutdown Current vs. V_{IN} (AW35111S)

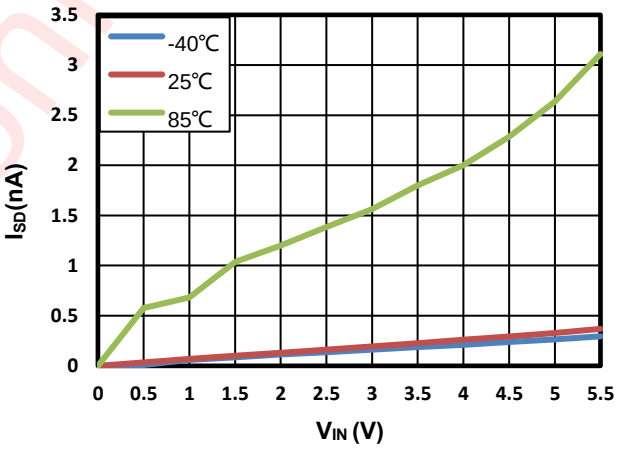


Figure 9 IN Shutdown Current vs. V_{IN} (AW35113S)

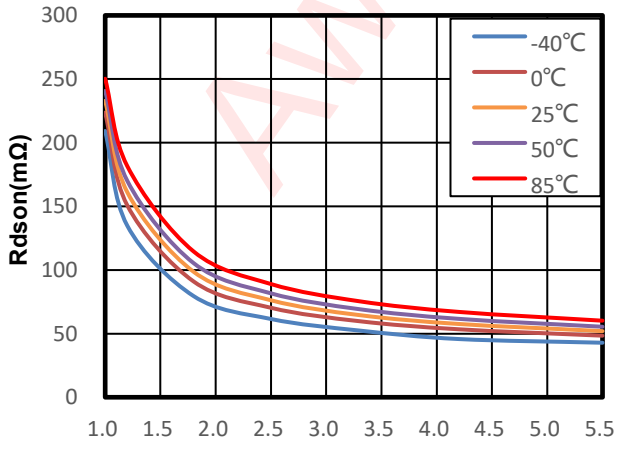


Figure 10 Rdson vs. V_{IN}(I_{OUT}=200mA)

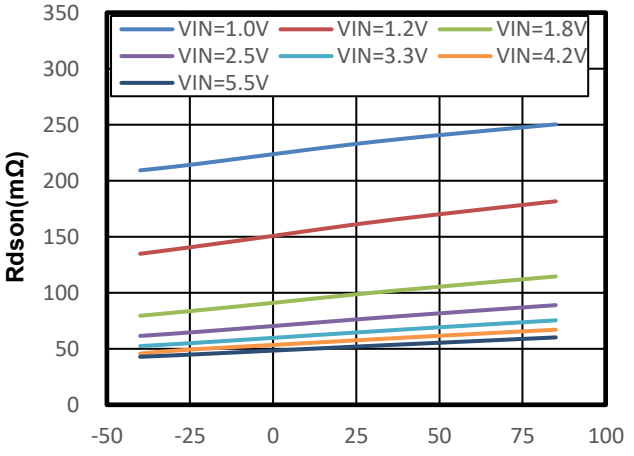


Figure 11 Rdson vs. Temperature(I_{OUT}=200mA)

Typical Characteristics (continued)

Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.

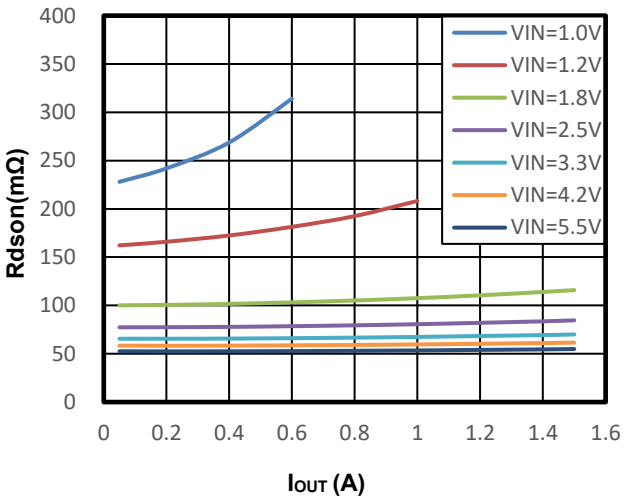
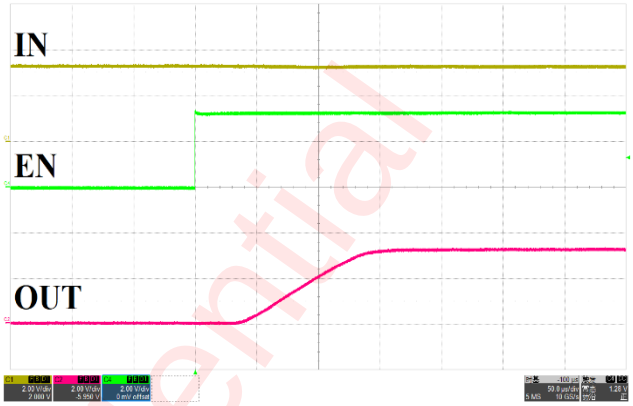


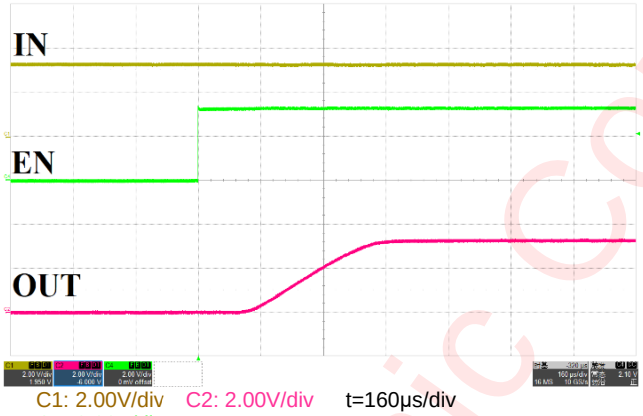
Figure 12 Rdson vs. I_{OUT}



C1: 2.00V/div C2: 2.00V/div t=50μs/div
C4: 2.00V/div

V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=0.1μF，R_{load}=10Ω

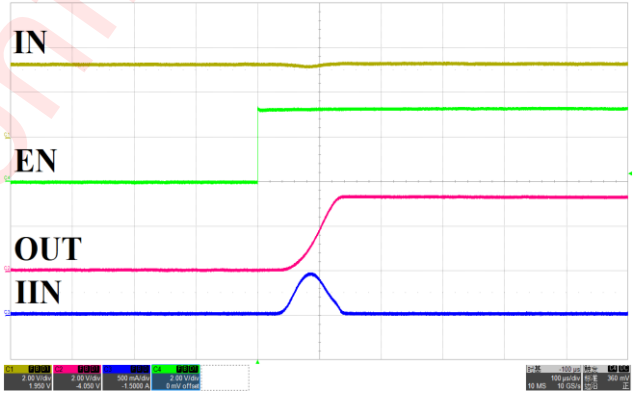
Figure 13 Turn On Response (AW35111S)



C1: 2.00V/div C2: 2.00V/div t=160μs/div
C4: 2.00V/div

V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=30Ω

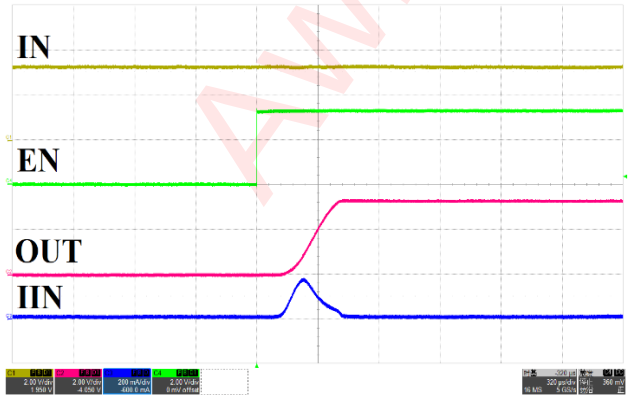
Figure 14 Turn On Response (AW35113S)



C1: 2.00V/div C2: 2.00V/div t=100μs/div
C3:500mA/div C4: 2.00V/div

V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=10μF，no R_{load}

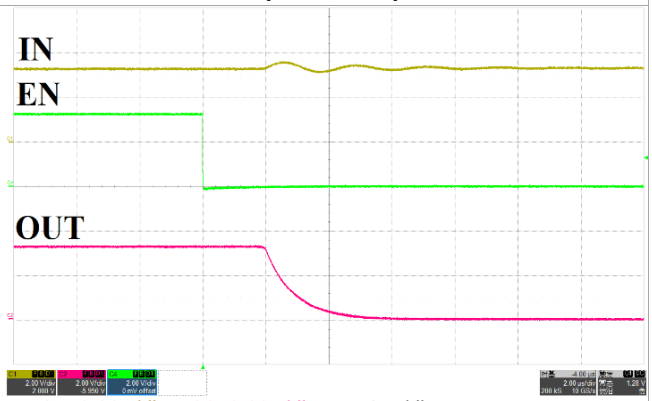
Figure 15 Inrush Current (AW35111S)



C1: 2.00V/div C2: 2.00V/div t=320μs/div
C3:200mA/div C4: 2.00V/div

V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=10μF，no R_{load}

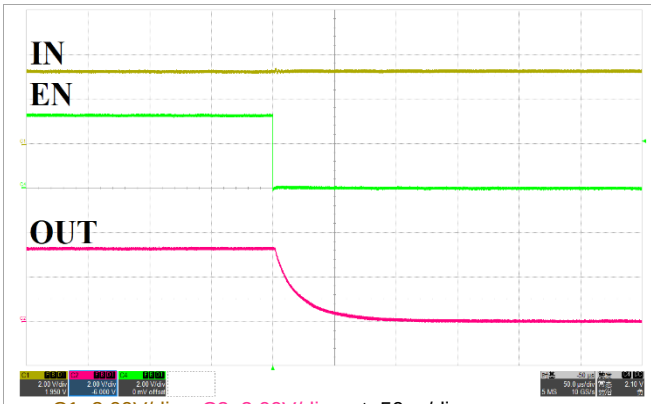
Figure 16 Inrush Current (AW35113S)



C1: 2.00V/div C2: 2.00V/div t=2μs/div
C4: 2.00V/div

V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=0.1μF，R_{load}=10Ω

Figure 17 Turn Off Response (AW35111S)



C1: 2.00V/div C2: 2.00V/div t=50μs/div
C4: 2.00V/div
V_{IN}=3.3V，C_{IN}=1μF，C_{OUT}=1μF，R_{load}=30Ω

Figure 18 Turn Off Response (AW35113S)

Detailed Functional Description

The AW35111S/AW35113S integrates a high side P channel MOSFET, and provides a low on-resistance for a low voltage drop across the device. A controlled slew rate is used in applications to limit the inrush current. The part can be turned on, with a supply voltage from 1V to 5.5V.

Turn On/Off Control

Enable pin is an active high port for AW35111S/AW35113S. The device is closed when EN pin is tied low or pulled down by internal 7.2MΩ resistor, forcing PMOS switch off. The IN/OUT path is activated with a minimum of V_{IN} of 1V and EN forced to high level.

Table 1. Functional Table

	EN	IN to OUT	OUT to GND
AW35111S/AW35113S	Low	OFF	ON
	High	ON	OFF

Slew Rate Control

When the switch is enabled, the device regulates the gate voltage of MOSFET, and controls the V_{OUT} slew rate during t_R to avoid a large input inrush current. The feature reduces the interference to the power supply.

Quick Output Discharge

The AW35111S/AW35113S includes the Quick Output Discharge (QOD) feature, in order to discharge the application capacitor connected on OUT pin. When EN pin is disabled, a discharge resistance with a typical value of 88Ω is connected between the output and ground, pull down the output and prevent it from floating when the device is disabled.

Full-Time Reverse Current Protection

The AW35113S include the Reverse Current Protection(RCP) function, which can prevent the current to flowing through the P-FET or the body diode when V_{OUT} greater than V_{IN}. Whatever the switch is on or off, the AW35113S always have this function. When V_{OUT}-V_{IN} greater than V_{REV}, the internal comparator quickly turns off the switch, in order to prevent large reverse current from V_{OUT} to V_{IN}. The switch will return to normal operation once the reverse voltage scenario disappeared.

The I_{REV_ACT} parameter in the Figure 19 can be calculated by the following formula

$$I_{REV\_ACT} = \frac{V_{REV}}{R_{dson}}$$

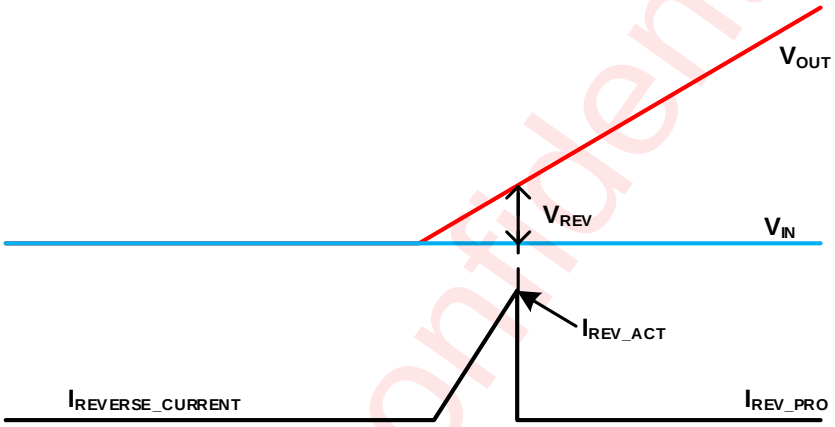


Figure 19 Reverse Current Test

Application Information

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device, the actual capacitance should be optimized for the particular application. For all applications, a 1μF or greater ceramic bypass capacitor between V_{IN} and GND is recommended as close to the device as possible. This precaution reduces ringing on the input due to power supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

PCB Layout Consideration

The AW35111S/AW35113S is low ON-Resistance load switch, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW35111S/AW35113S) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW35111S/AW35113S) and close to OUT pin.

2. The AW35111S/AW35113S integrates an up to 1.5A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R\theta_{JA}$ of the package can be decreased, allowing higher power dissipation. Blue bold paths in Figure 20 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

3. Use rounded corners on the power trace from the power supply connector to AW35111S/AW35113S to decrease EMI coupling.

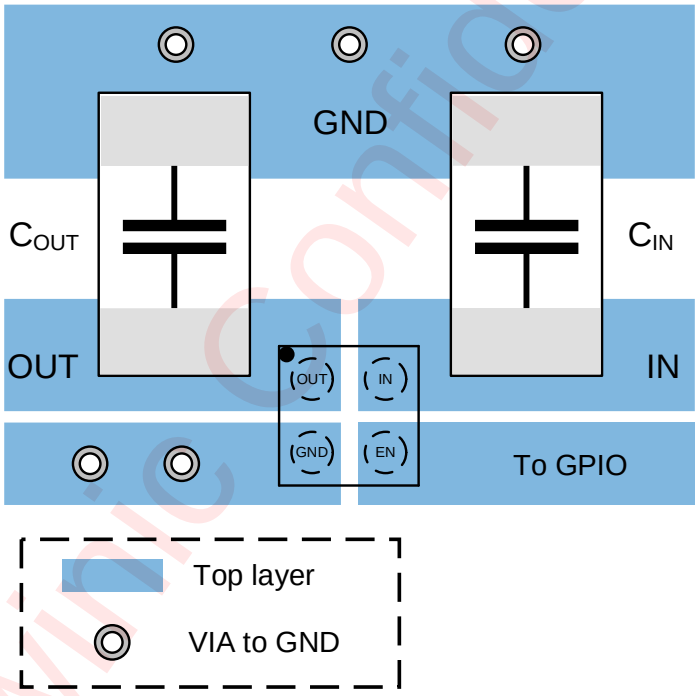
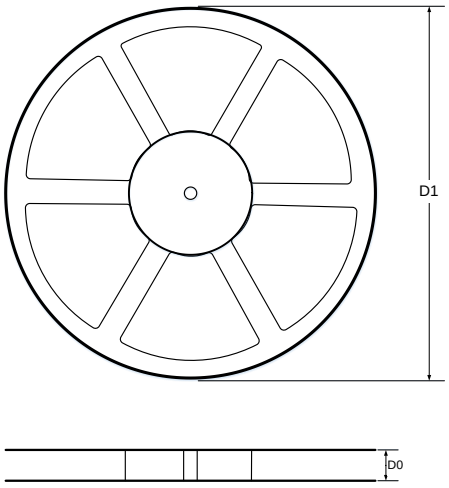


Figure 20 PCB layout example

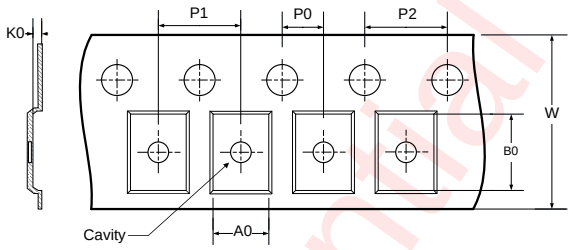
Tape And Reel Information

WLCSP 0.618mm*0.618mm-4B

REEL DIMENSIONS

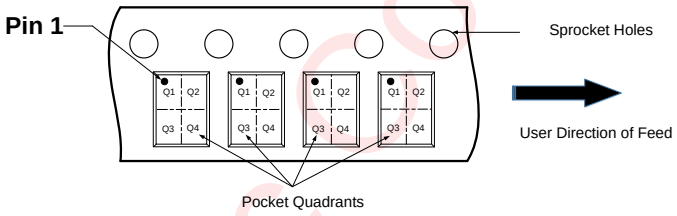


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

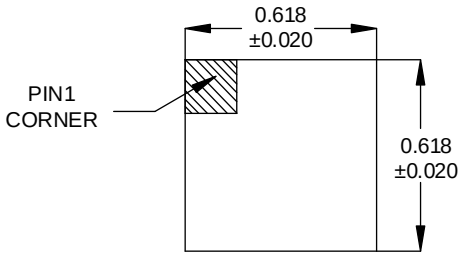
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180.0	8.6	0.71	0.71	0.52	2.00	4.00	4.00	8.00	Q1

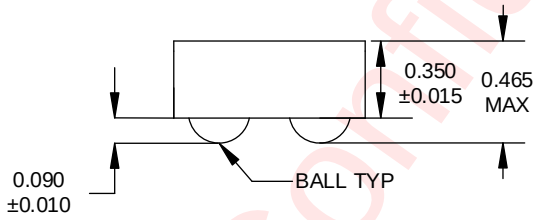
All dimensions are nominal

Package Description

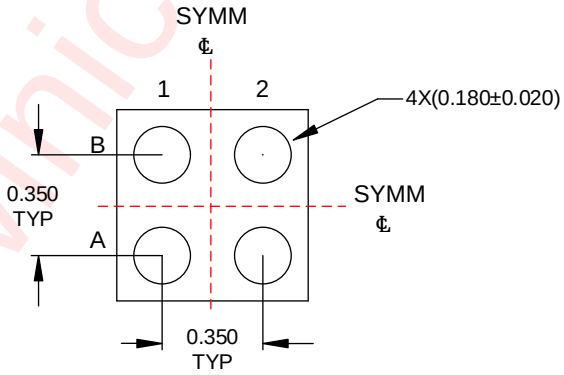
WLCSP 0.618mm*0.618mm-4B



Top View



Side View

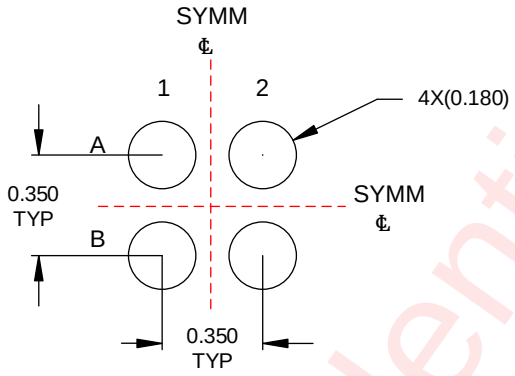


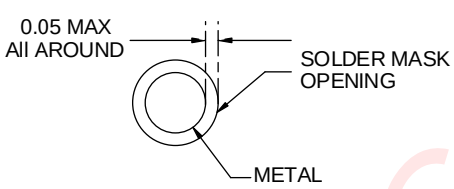
Bottom View

Unit：mm

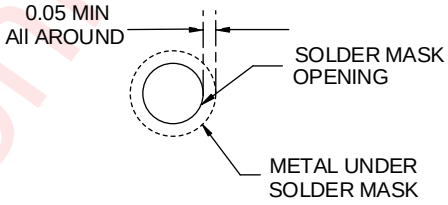
Land Pattern Data

WLCSP 0.618mm*0.618mm-4B





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Apr. 2025	Officially released

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