8-Channel Capacitive Wear Detection and Touch Key Controller

Features

- 8-channel capacitive sensor
  - Self/Mutual capacitive sensing
  - Capacitance resolution down to 1aF
  - Automatic Offset Tuning (AOT)
  - Adaptive Temperature Compensation
  - Effective waterproof
  - Independent configuration per channel
- Built-in gesture/event recognition:
  - Click/Wear detection
  - Linear slide detection
  - Wheel slide detection
  - Capacitive force detection
- 400kHz I2C interface
  - Default address: 0x12
  - Address can be modified through CS2 pin
- External interrupt pin INTN, open-drain output
- Built-in brown-out reset(BOR)
- Power consumption
  - Active mode: 27.5μA
  - Doze mode: 12μA
  - Sleep mode: 10μA
  - Deep Sleep mode: 6.5μA
- 2.7V~3.6V power supply
- QFN 3×3-24L

Applications

Mobile phones, Tablets, Laptops

Wearable devices

Desk lamps, Smart door locks

General Description

AW93208QNR is an 8-channel capacitive proximity and touch controller mainly used for wear detection, touch key, linear slider, wheel slider, etc. The chip can realize accurate position detection for lamp dimming, volume adjustment, etc.

AW93208QNR can recognize various gestures, such as single/double/triple click, short/long press, linear slide and wheel slide with the high-resolution capacitive sensing. The chip integrates mutual capacitive technology and dedicated algorithm, which greatly improve the waterproof performance for touch key.

The built-in ultra-low-power MCU and 16KB flash realize AFE sampling control, signal filtering, RF noise suppression, adaptive temperature compensation, baseline tracking, touch/wearing status determination, etc. The chip can flexibly customize the program and support online upgrade function.

Typical Application Circuit

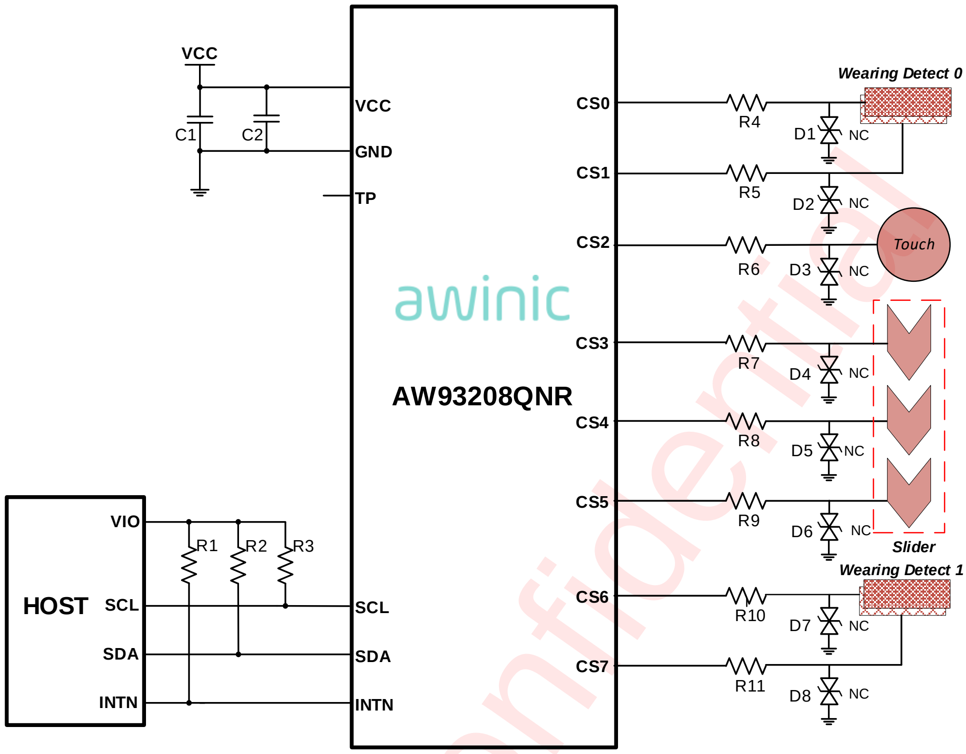


Figure 1 AW93208QNR Typical Application Circuit (touch, wear and slide)

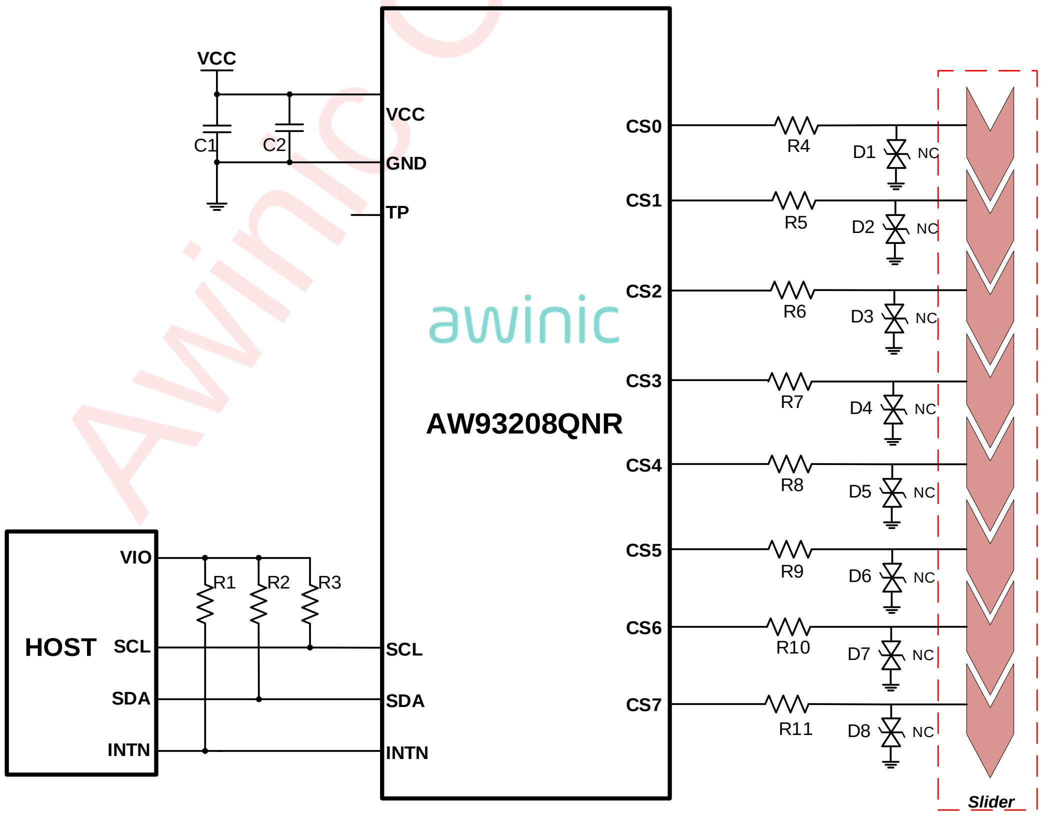
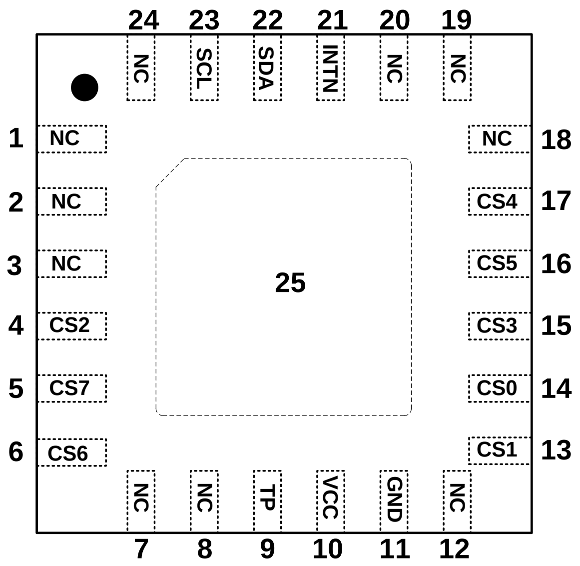


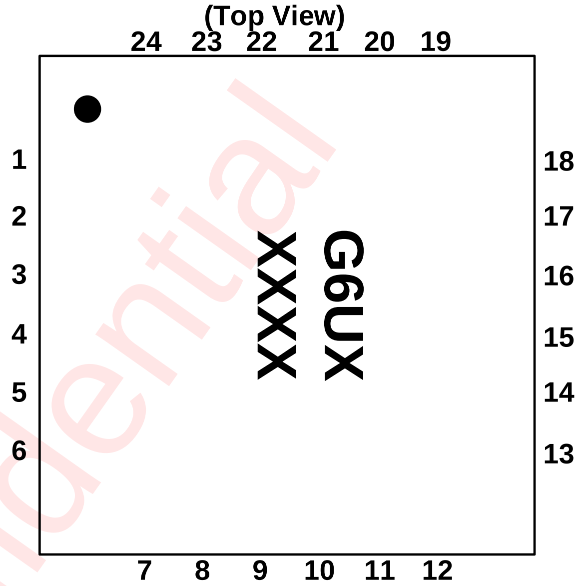
Figure 2 AW93208QNR Typical Application Circuit (slide)

Pin Configuration and Top Mark

AW93208QNR
(Top View)



AW93208QNR
Marking
(Top View)



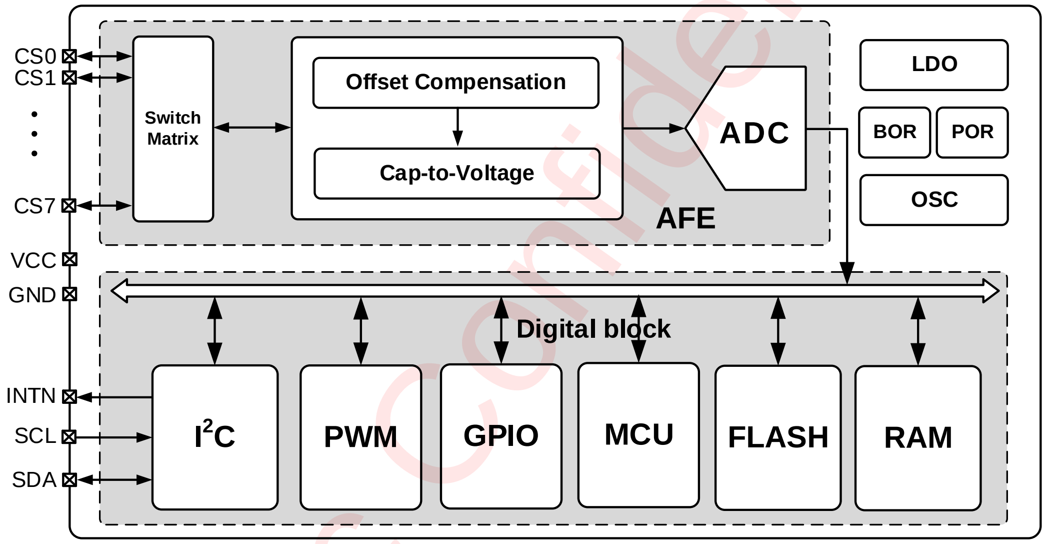
G6UX - AW93208QNR
XXXX - Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
1	NC	No connection
2	NC	No connection
3	NC	No connection
4	CS2	Capacitive sensor input/shield/digital I/O or I^2C address select Input (Floating:0x12, GND:0x13, VCC:0x14)
5	CS7	Capacitive sensor input/shield/digital I/O
6	CS6	Capacitive sensor input/shield/digital I/O
7	NC	No connection
8	NC	No connection
9	TP	Test pin, floating
10	VCC	Chip power supply(2.7V~3.6V),requires decoupling capacitor
11	GND	Ground
12	NC	No connection
13	CS1	Capacitive sensor input/shield/digital I/O
14	CS0	Capacitive sensor input/shield/digital I/O
15	CS3	Capacitive sensor input/shield/digital I/O
16	CS5	Capacitive sensor input/shield/digital I/O
17	CS4	Capacitive sensor input/shield/digital I/O

18	NC	No connection
19	NC	No connection
20	NC	No connection
21	INTN	Interrupt output (open drain)
22	SDA	Serial data I/O for I^{2}C interface
23	SCL	Serial clock input for I^{2}C interface
24	NC	No connection
25	Thermal pad	Connected to GND

Functional Block Diagram



Notes: AFE means Analog Front-End.

Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW93208QNR	-40°C~85°C	QFN 3×3-24L	G6UX	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC		-0.5V to 3.6V
Input voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Output voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Operating free-air temperature range		-40°C to 85°C

Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including HBM CDM)(NOTE 2)	
HBM	±8kV
CDM	±1.5kV
Latch-Up	
Test condition: according to JESD78E	+IT：350mA -IT：-350mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method: ESDA/JEDEC JS-001-2017 ,the CDM test method: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

PARAMETERS	SYMBOL	MIN	MAX	UNIT
Supply voltage	VCC	2.7	3.6	V
Pull-up voltage	VIO	1.1	3.6	V
Ambient temperature	T_A	-40	85	°C

Electrical Characteristics

Note:Typical values are given for T_A = +25°C, VCC=2.8V unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CHIP CURRENTS						
$I_{DEEPSLEEP}$	Deep Sleep Mode Current	LDO on, OSC off I²C listening		6.5		μA
I_{SLEEP}	Sleep Mode Current	LDO on, OSC on I²C listening		10		μA
I_{DOZE}	Doze Mode Current	SCANPERIOD = 400ms FREQ = 100kHz CDCRES = 6 CHEN = b000001 Digital filter features OFF I²C listening. No load		12		μA
I_{ACTIVE}	Active Mode Current	SCANPERIOD = 30ms FREQ = 100kHz CDCRES = 6 CHEN = b000001 Digital filter features OFF I²C listening. No load		27.5		μA
CAPACITANCE SENSING						

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{RANGE}	Measurement Range		±0.55	±2.2	±9.9	pF
N_{BIT}	Measurement Resolution			21		bits
C_{RES}			1			aF
F_{OSC}	Nominal OSC Frequency			4		MHz
F_{Trim}	OSC Trim Accuracy	Around Nominal Value, Ta=25°C, VCC=2.8V	-4		4	%
F_{Temp}(NOTE3)	OSC Temp. Dependency	Around Nominal Value, Full Ta range, VCC=2.8V	-1		1	%
F_{VCC}(NOTE3)	OSC VCC Dependency	Around Nominal Value, Ta=25°C, Full VCC range	-0.6		0.6	%
Fs	Nominal Sampling Freq	Programmable with FREQ	F_{OSC} /1024		F_{OSC} / 16	kHz
C_{DCEXT}	External DC Cap. to GND per Measurement Phase	One CSx as measured input			220	pF
R_{FILTIN}	Input driving Res		0		30	kΩ
R_{INT}	Compensation Res		125		1000	Ω
I²C INTERFACE						
I_{OL} （SDA，INTN）	Output low current	V_{OL}≤0.4V	8			mA
V_{IH}	Input high level	SCL, SDA	0.84		3.6	V
V_{IL}	Input low level	SCL, SDA	-0.5		0.36	V
t_{DEG_SDA}	SDA deglitch time	SDA		88		ns
t_{DEG_SCL}	SCL deglitch time	SCL		77		ns

NOTE3: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

I²C Interface Timing

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency			400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
T_{LOW}	Low level width of SCL	1.3			μs
T_{HIGH}	High level width of SCL	0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6			μs
$T_{HD:DAT}$	Data hold time	0			μs
$T_{SU:DAT}$	Data setup time	0.1			μs
T_R	Rising time of SDA and SCL			0.3	μs

PARAMETER		MIN	TYP	MAX	UNIT
T_F	Falling time of SDA and SCL			0.3	μs
$T_{SU:STO}$	Stop condition setup time	0.6			μs
T_{BUF}	Time between start and stop condition	1.3			μs

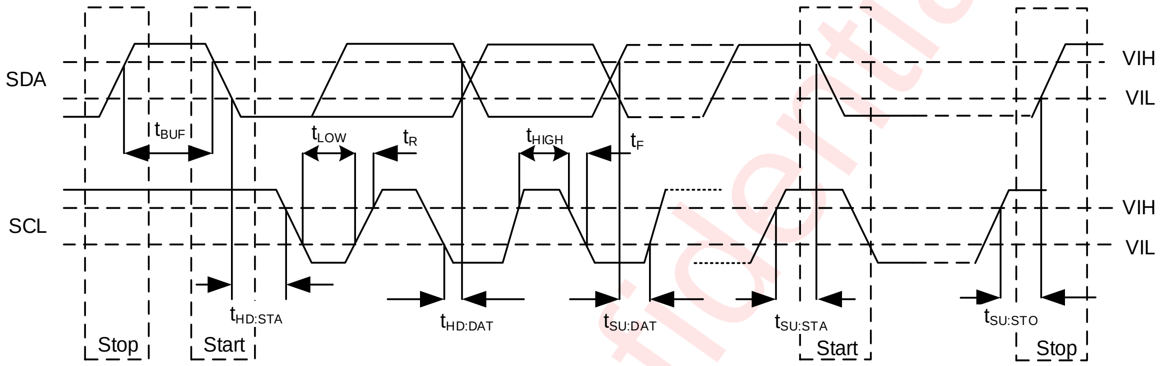


Figure 4 I²C Interface Timing

Capacitive Sensor Basics

When a conductive object, such as a finger, comes in contact or close proximity with the sensing electrode, the capacitance of one or more sensors changes. The figure below shows the basic structure and equivalent model of a capacitive sensor. The top layer is the front-panel, and the middle green area below is a copper sensor pad. The sensor is usually surrounded by ground, resulting in a parasitic capacitance(C_{PARA}).

There are two main operational modes in the capacitance sensing circuits: self-capacitance sensing and mutual capacitance sensing. An electric field is created around the sensor when system is working. In the self-capacitance sensing mode, with target object approaching, some of the electric field lines couple to the target object and add a small amount of finger capacitance (C_{PROX}) to the existing C_{PARA}. This feature can be used to detect proximity or touch action.

At least two electrodes are needed in the mutual capacitance sensing mode: one is a transmitter (Tx) and the other is a receiver (Rx). Tx and ground will form a capacitance (C_{PARAT}); Rx and ground will form a capacitance (C_{PARAR}); Tx and Rx will form a capacitance (C_M). When target object approaches, Tx and Rx will form a capacitance ($C_{M'}$) which is less than C_M.

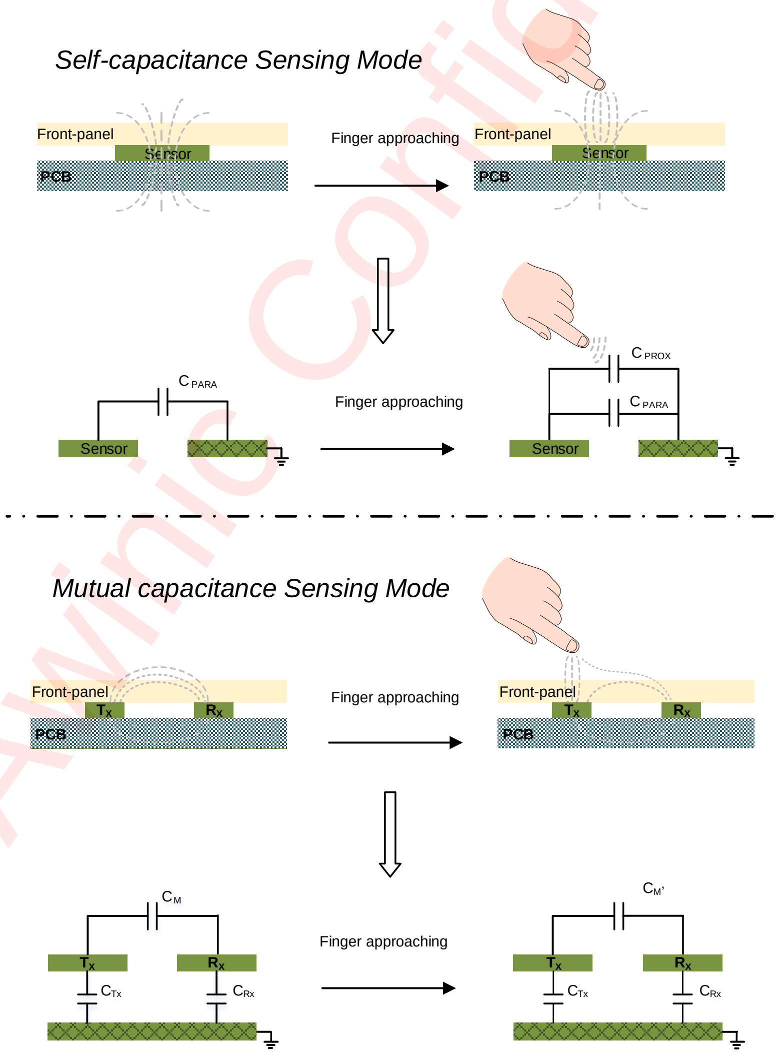


Figure 5 Capacitive Sensor Structure

Detailed Functional Description

Overview

AW93208QNR is a capacitive in-ear detection and touch key controller with a built-in ultra-low-power MCU. Each sensor channel can be configured as mutual capacitance detection or self-capacitance detection. AW93208QNR is composed of AFE, MCU, FLASH, RAM, OSC, I^2C, etc. AFE is mainly used to drive the sensor and shield electrodes, and convert the capacitance of sensor to digital data. MCU executes the algorithm program in the FLASH, and performs basic operations such as signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency(RF) noise suppression, proximity detection, etc. It is able to accurately identify single/double/triple click, short/long press, linear slide and wheel slide, etc.

Capacitive Sensing Techniques

The proximity sensing system consists of three parts: capacitive sensor, AFE and DSP. Among them, the function of AFE is to drive the capacitive sensor and the shield electrode, and convert the sensor capacitance into digital data. The function of DSP is to process the data from AFE and transmit the sensor capacitance value (CapDiff, CapValid) together with proximity status (status) to the host. When the target object is approaching or moving away, the proximity sensing system will transmit key information to the host after dedicated processing.

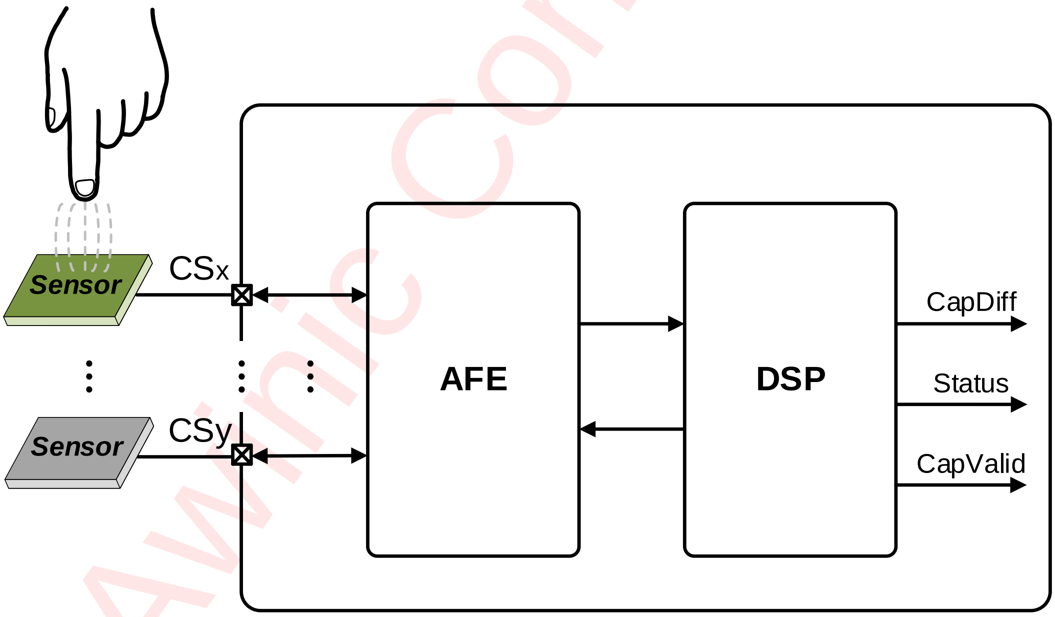


Figure 6 Proximity Sensor Operation Overview

AFE Description

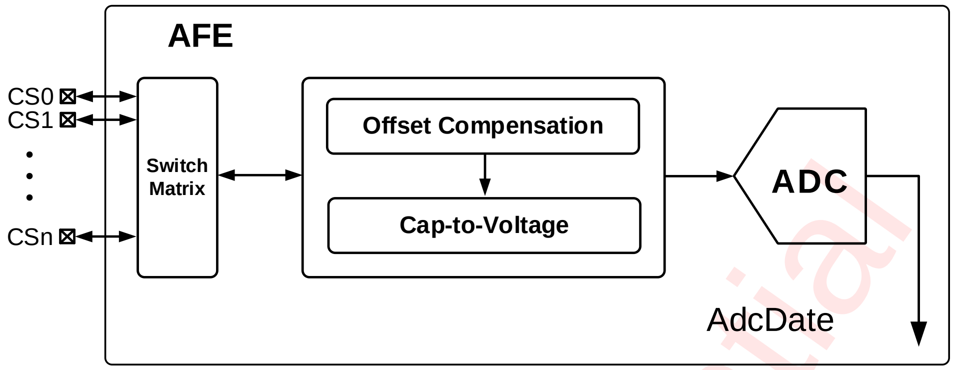


Figure 7 AFE Block Diagram

※ Block Switch Matrix selects pin CSx as capacitance measurement input.

※ Cap-to-Voltage integrates a charge amplifier, it detects the sensor capacitance with a charge-transfer method. The capacitance is converted into a voltage signal, which is the input of ADC.

※ Offset Compensation measures parasitic capacitance(C_{PARA}), which is compensated during the process of charge transferring of Cap-to-Voltage. Thus, the input capacitance of Cap-to-Voltage is nearly C_{PROX} alone.

※ ADC converts voltage signals obtained by Cap-to-Voltage or Temp Sensor into AdcData.

DSP Description

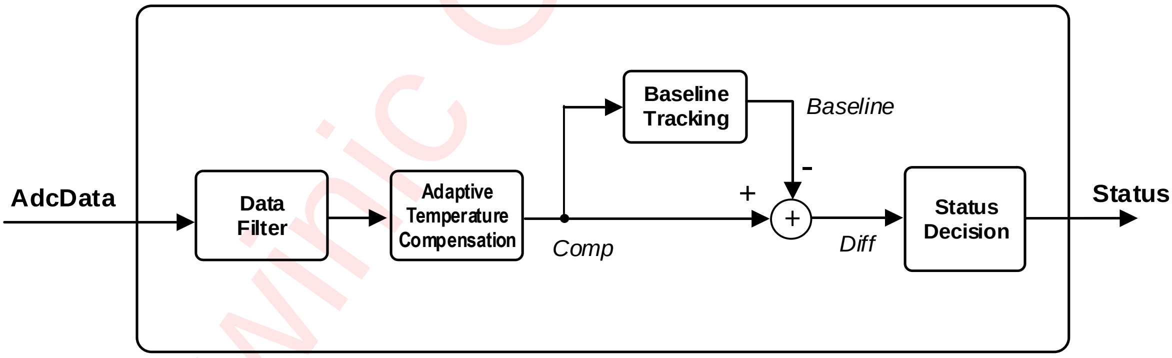


Figure 8 Digital Signal Processing Diagram

※ DSP processes the AdcData from the AFE, and finally outputs a series of reliable proximity status.

※ Data Filter effectively filters the high-frequency noise and interference, which greatly improves the signal-to-noise ratio(SNR).

※ The adaptive temperature compensation module can automatically compensate for environmental drift in real time, especially temperature drift. Thereby it can be ensured that the final proximity status will not be misjudged due to temperature drift.

※ The role of the Baseline is to further track the slowly varying data caused by the residual temperature compensation or other gradual environmental drift.

※ Finally, the Status Decision module outputs a certain and reliable proximity status based on the Diff data and the proximity threshold etc.

Scan Period

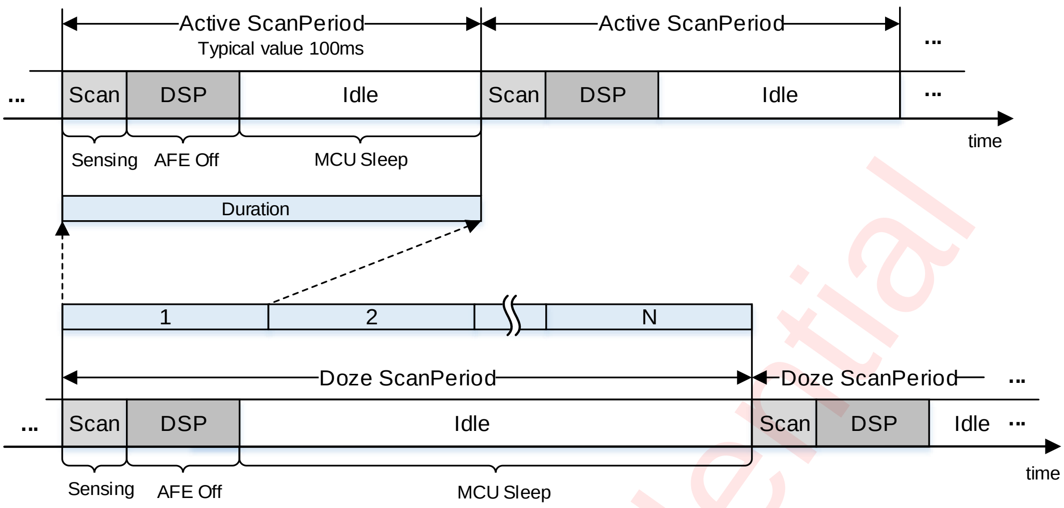


Figure 9 Active Mode and Doze Mode Scan Period

Each scan period can be divided into three stages. In the first stage, the selected sensor channel is scanned and AdcData is generated. In the second stage, the AFE is closed and the AdcData obtained by the DSP module is processed. In the last stage, all data processing has been completed and the chip enters idle status, in order to reduce power consumption, neither AFE nor MCU will work.

The figure above shows the composition and meaning of the active mode and doze mode scan periods. The scan period of active mode and doze mode can be configured by register SCANCTRL1(Address: 0x1A04) and AFECFG3_CHx (x=0,…,7). Generally, doze mode consumes much lower power than active mode.

Clock

The AW93208QNR uses a built-in 4MHz OSC clock.

Reset

Power On Reset (POR)

Reset operation is triggered during power up. When nRST released, the initialization process starts to perform and it will last for about 20ms. INTN will be set to low when the initialization process is completed, then I^{2}C can communicate normally.

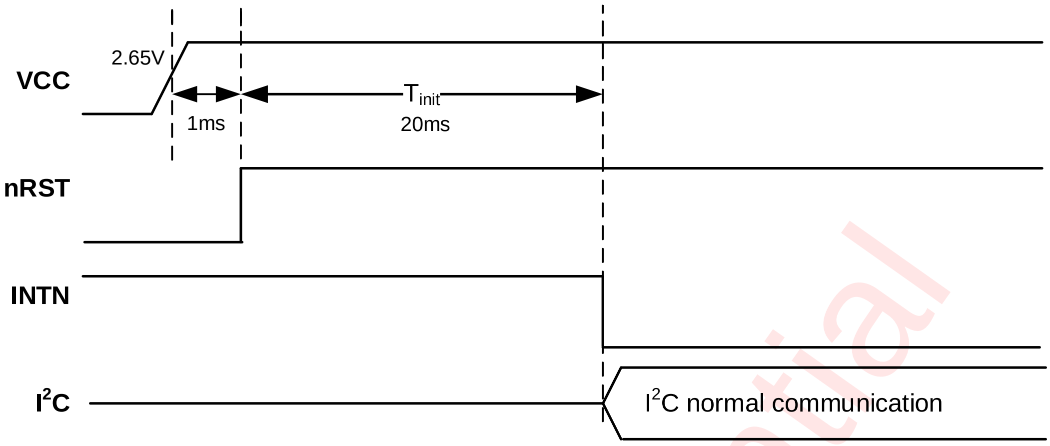


Figure 10 Power On Timing

Brown Out Reset (BOR)

Reset operation is triggered when VCC drop to the threshold of BOR. After the reset operation, all the registers will be reset to the default value. The chip returns to normal operation mode until the power supply rises to a normal value.

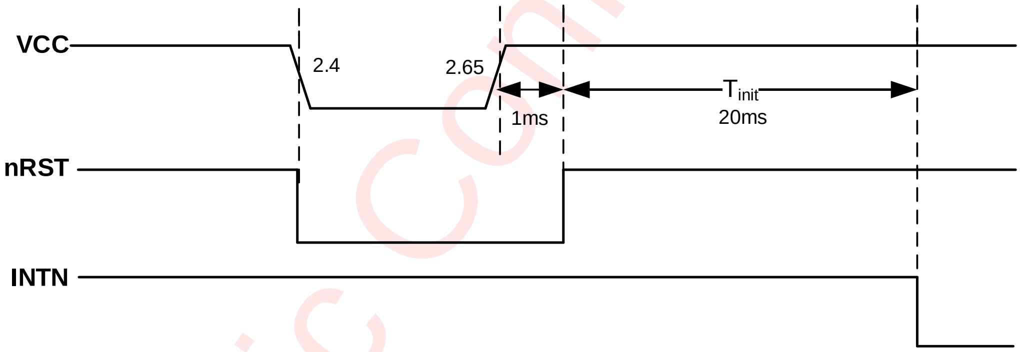


Figure 11 Brown Out Timing

Soft Reset

The soft reset operation can be triggered by writing “0x3C” to the soft reset register (Address: 0xFF18). After the reset operation is completed, all the registers will be reset to the default value.

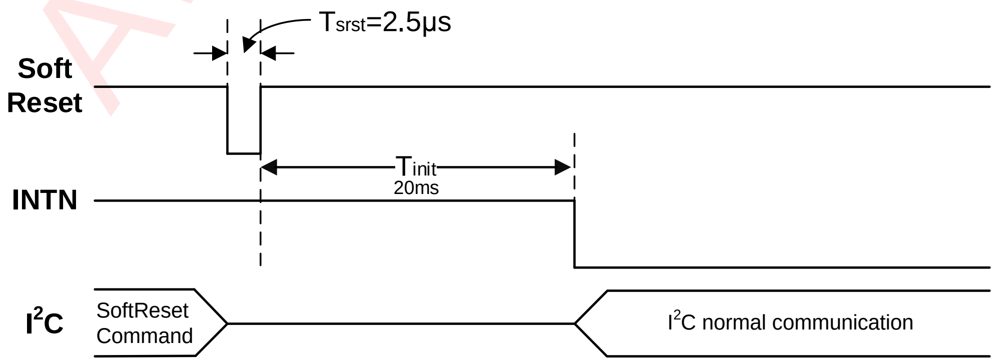


Figure 12 Soft Reset Timing

Initialization

After power on, OSC runs normally, and MCU starts to execute the initialization program in FLASH. It performs the following operations.

- Read information from NVM Flash
- Set I^2C device address according to CS2 pin status
- Issue an interrupt after initialization and then enters into sleep mode.

Operation Mode

There are four operation modes in the AW93208QNR: Deep Sleep, Sleep, Active and Doze.

Deepsleep

The device power consumption is lowest in this mode. OSC and AFE are closed, CPU is sleeping, only I^2C interface is active.

Sleep

The device is in a low power state. OSC is on, AFE is off, and CPU is sleeping, waiting for interrupt to wake up.

Active

The device works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When no touch or proximity has been detected for some time, it will automatically switch to Doze mode. In this mode the external HOST can send Sleep command to switch the device into sleep mode.

Doze

The scan period is long, MCU and AFE work intermittently. During the large part of period, most modules are in idle state. So the average power consumption is lower.

Once a proximity is detected in doze mode, it will automatically return to active mode. The external HOST can also send Sleep command to switch the device to sleep mode.

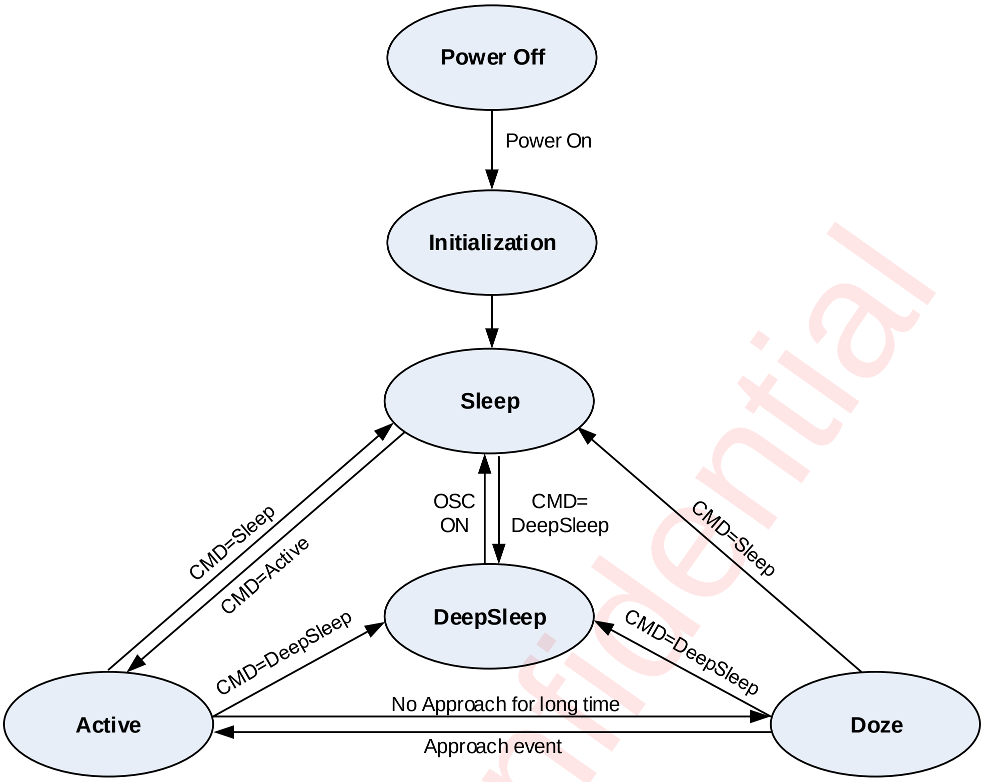


Figure 13 Operation Mode Switching

Interrupt

The AW93208QNR reports the interrupt signal to the host through the INTN pin. Register IRQSRC (Address: 0x4410) stores interrupt information, including the completion of parasitic capacitance calibration, scan cycle completion, and so on. Register IRQSRC is cleared after host read. Each specified interrupt triggered or not can be configured by register IRQEN (Address: 0x4414).

I²C Interface

AW93208QNR supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW93208QNR can support different high level of the I²C interface. Additionally, the I²C device supports continuous read and write operations. The I²C register address is 16-bit and register data is 32-bit, and the data transmission is in big-endian mode.

Device Address

I²C device address configuration

CS2 Connection	Device Address
Floating	0x12
GND	0x13
VCC	0x14

The I²C device address (7-bit, followed by the R/W bit(Read=1/Write=0)) of AW93208QNR depends on the CS2 pin status. The default value of I²C device address is 0x12, connecting pad CS2 to GND or VCC (Chip supply voltage) will change the device address as showed in table above. Note that when pad CS2 is connected to GND or VCC, it can't be used as sensor pad. The power supply of the pin of CS2 and the chip power need to use the same power supply.

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

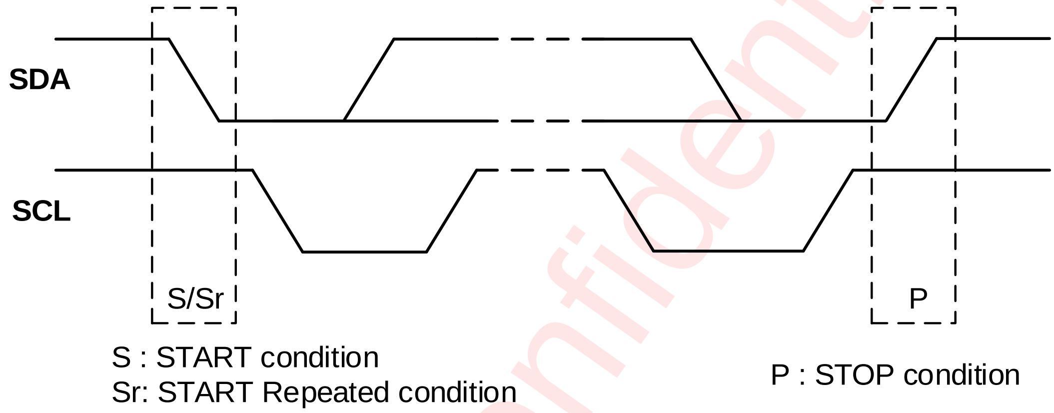


Figure 14 I²C Start/Stop Condition Timing

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

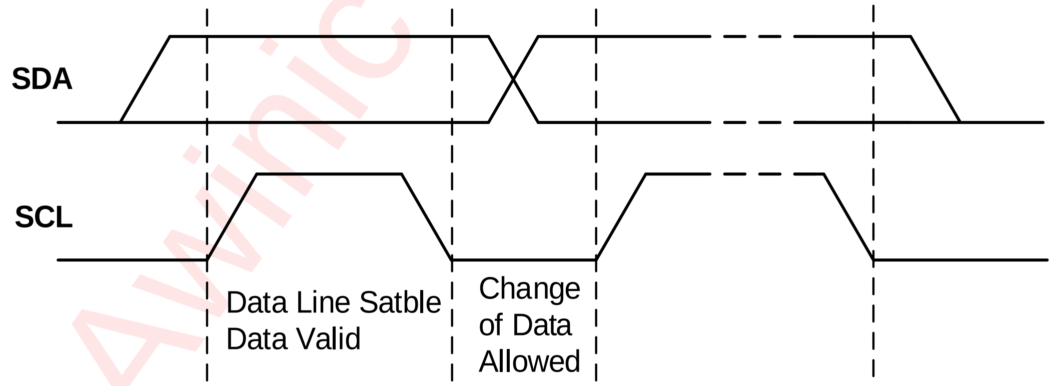


Figure 15 Data Validation Diagram

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

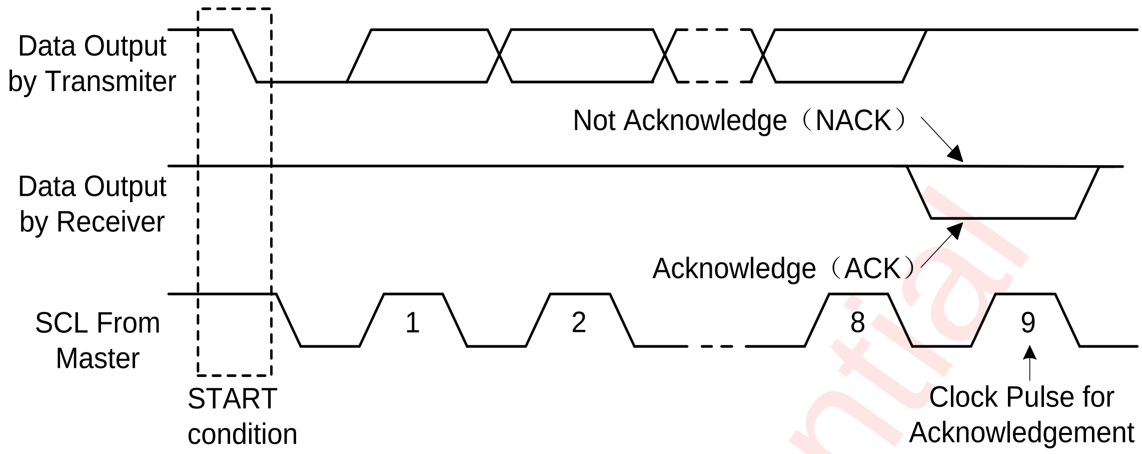


Figure 16 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 16-bit and register data is 32-bit. Note that I²C also support 8-bit data transfer. Writing process of I²C is showed as below picture.

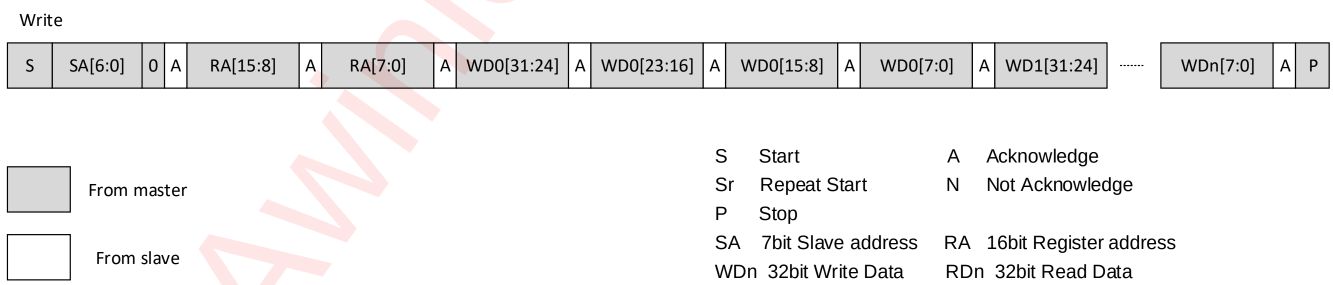


Figure 17 I²C Write Byte Cycle

Read Cycle

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is showed as below picture.

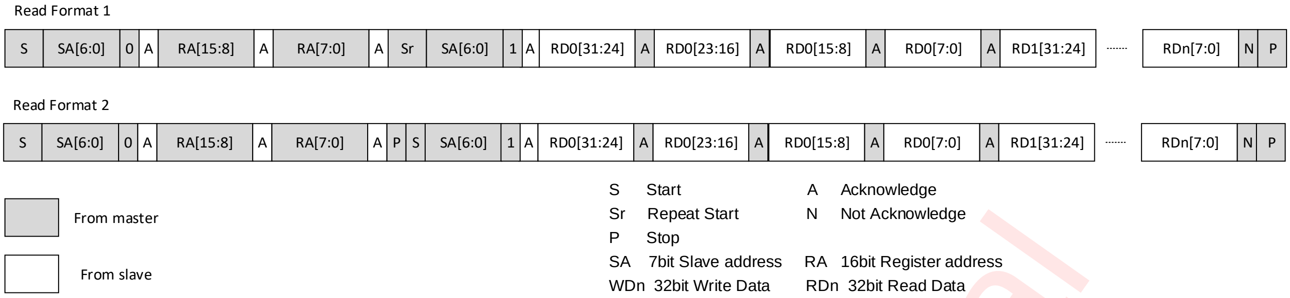


Figure 18 I²C Read Byte Cycle

Gestures

AW93208QNR can implement several gestures on the button and slider, including **single-click**, **double-click, triple-click**, **short-press**, **long-press** and **slide**.

Single-click

Single-click refers to a quick tap event, when a touch is triggered and then released in the same location within a short period of time. The *clickth* and *intervalth* threshold can be adjusted according to practical application requirements. **Single-click** event is based on the following conditions:

> 1st condition: The time of the touch state must be less than the *clickth*.

> 2nd condition: The time between two touch states must be more than the *intervalth.*

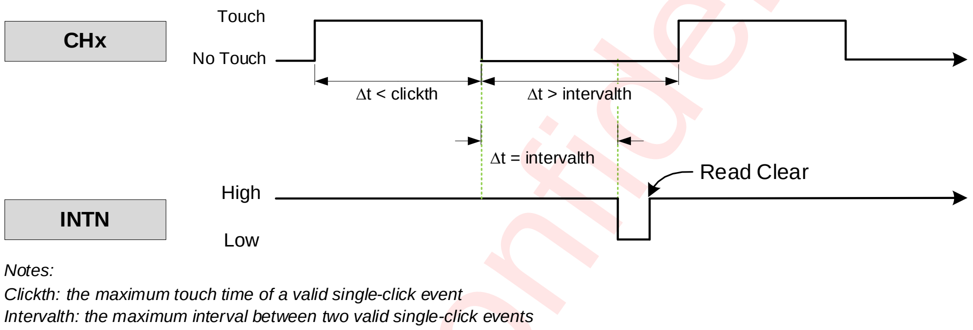


Figure 19 Single-click Sequence Diagram

Double-click and Triple-click

Double-click refers to two quick tap events and **triple-click** refers to three quick tap events. The definition of **triple-click** and **double-click** are different in the number of taps. **Double-click** and **triple-click** events are based on the following conditions:

> 1st condition: The time of the touch state must be less than the *clickth*.

> 2nd condition: The time between two adjacent touch states must be less than the *intervalth.*

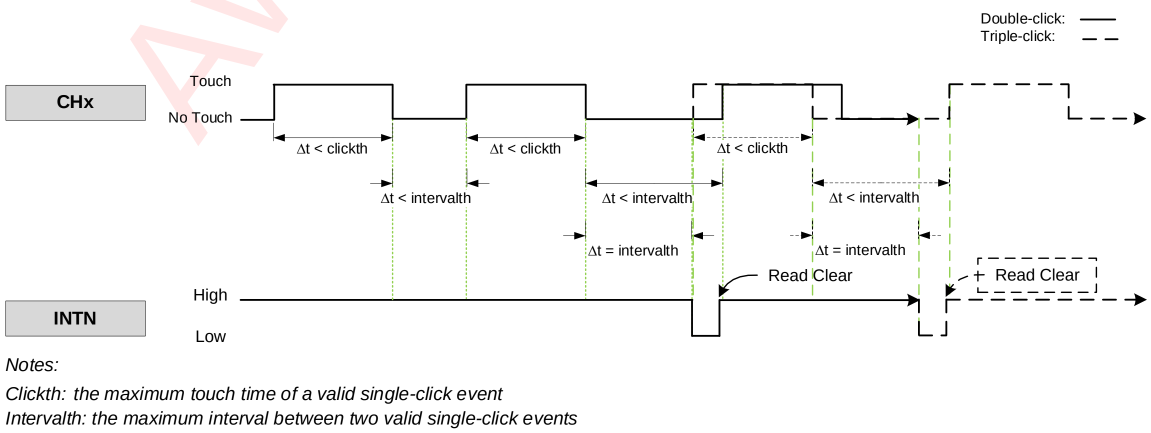


Figure 20 Double-click and Triple-click Sequence Diagram

Short-press

Short-press refers to a short time touch event, **Short-press** gesture is based on the following condition: The time during the touch state must be less than the *longpressth* and more than *shortpressth*.

Short-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch state is released.

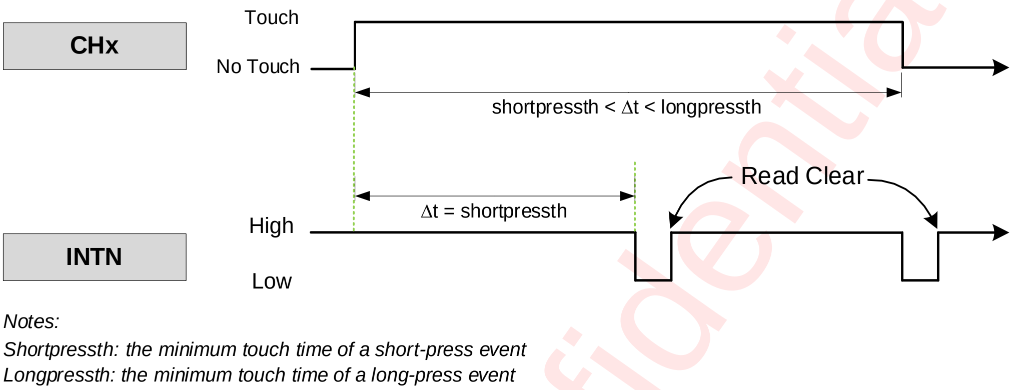


Figure 21 Short-press Sequence Diagram

Long-press

Long-press refers to a long time touch event. **Long-press** is based on the following condition: The time during the touch state must be more than the *longpressth*.

Long-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch time reaches the *longpressth* threshold.

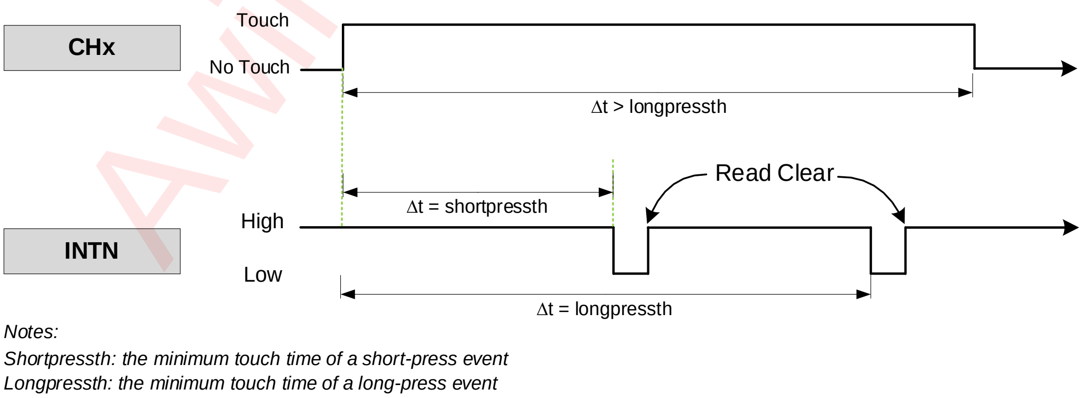


Figure 22 Long-press Sequence Diagram

Slide

Slide is based on the following condition: The coordinate change during the touch state must be more than the *slideth*(the minimum slip distance of a slide event).

A click(or press) is more difficultly recognized as a **slide** with a higher *slideth*. A **slide** is more difficultly recognized as a click(or press) with a lower *slideth*.

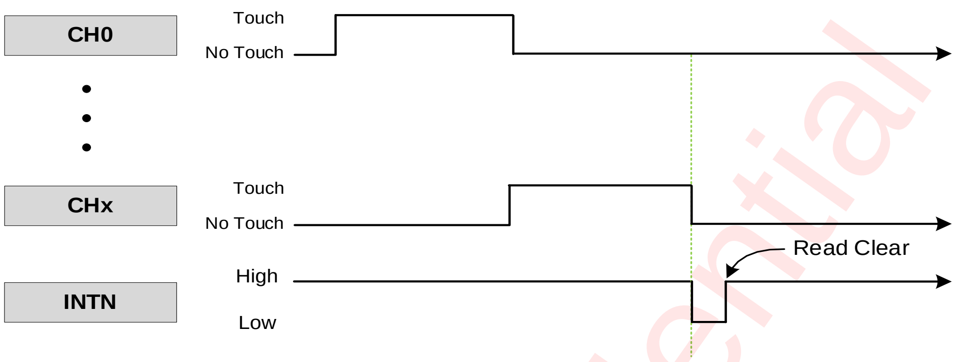


Figure 23 Slide Sequence Diagram

Single sliding definition: The finger touches the slide bar, slide for distance on the slide bar, and the sliding event is reported after the finger leaves. There are two slide speed levels: fast sliding and slow sliding.

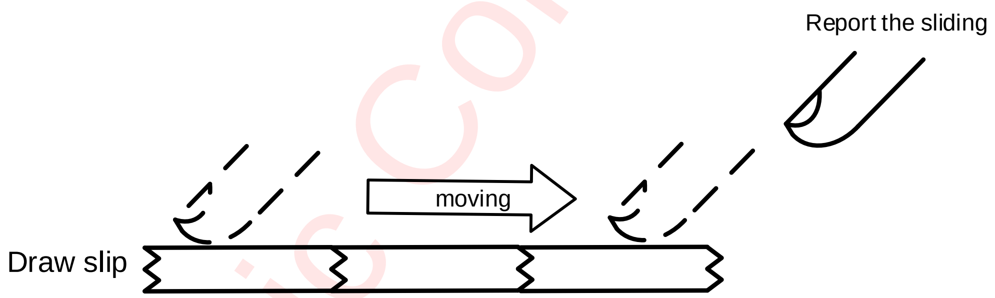


Figure 24 Single Sliding Diagram

Continuous sliding definition: The finger touches the slider without leaving the hand, sliding events will be reported every time the finger slide a certain distance (configurable).

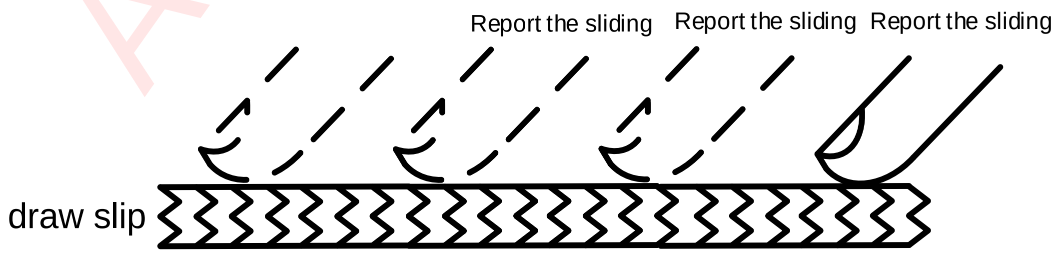


Figure 25 Continuous Sliding Diagram

The parameters of wheel sliders include **SlidePosition**, **MoveDistance**, **MoveDir**, **CircleCnt**, and **CircleDir**. **SlidePosition** means the touch position; **MoveDistance** means the distance between the start position and the end position; **MoveDir** means the relationship between the start position and the end position of the slide; **CircleCnt** means the number of turns a finger can make on the wheel slider; **CircleDir** means the direction of the sliding number of turns, such as counterclockwise or clockwise.

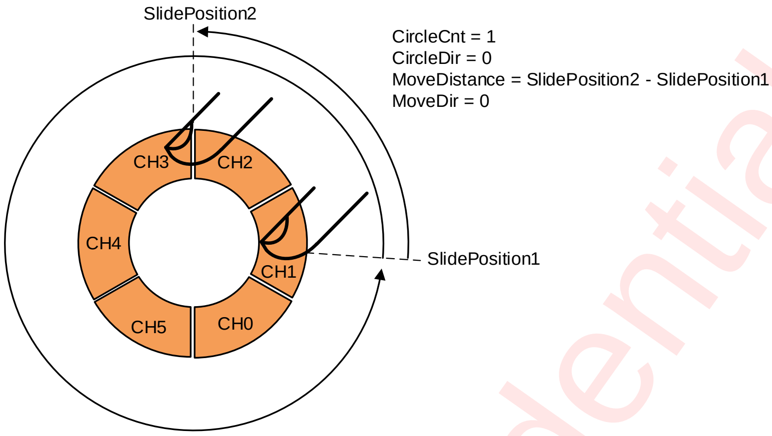


Figure 26 Counterclockwise Diagram

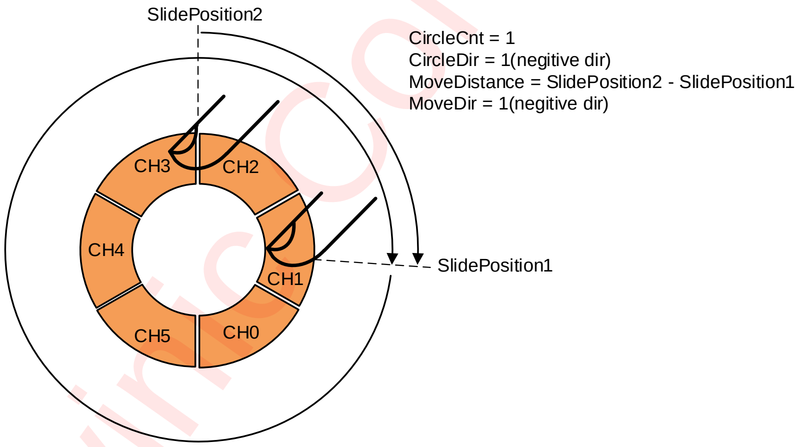


Figure 27 Clockwise Diagram

Application Information

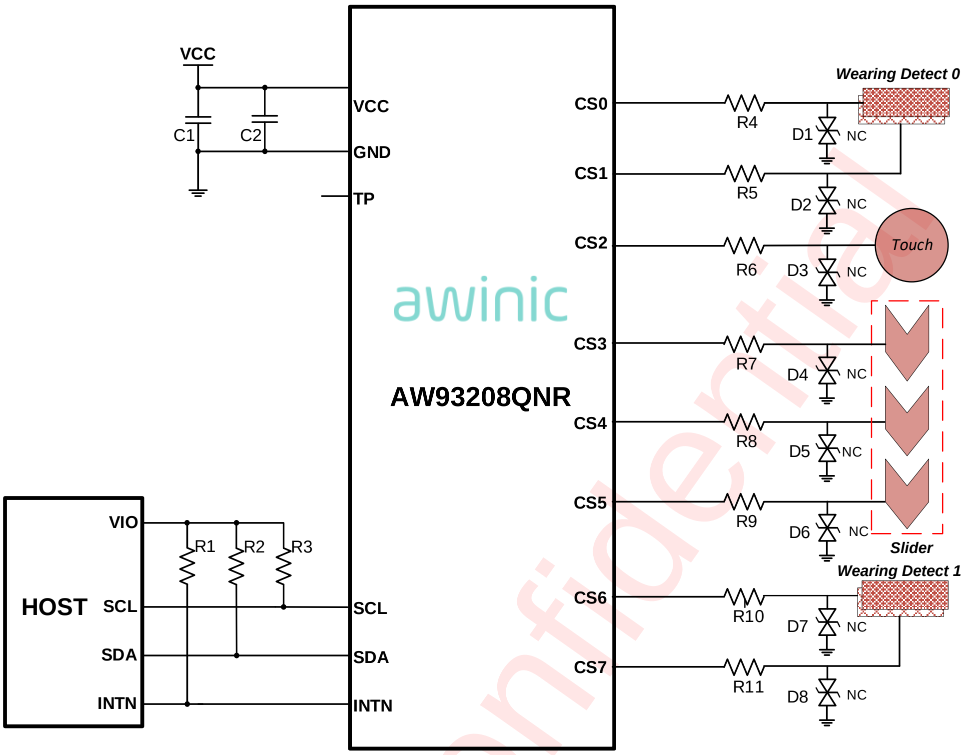


Figure 28 AW93208QNR Typical Application Circuit (touch, wear and slide)

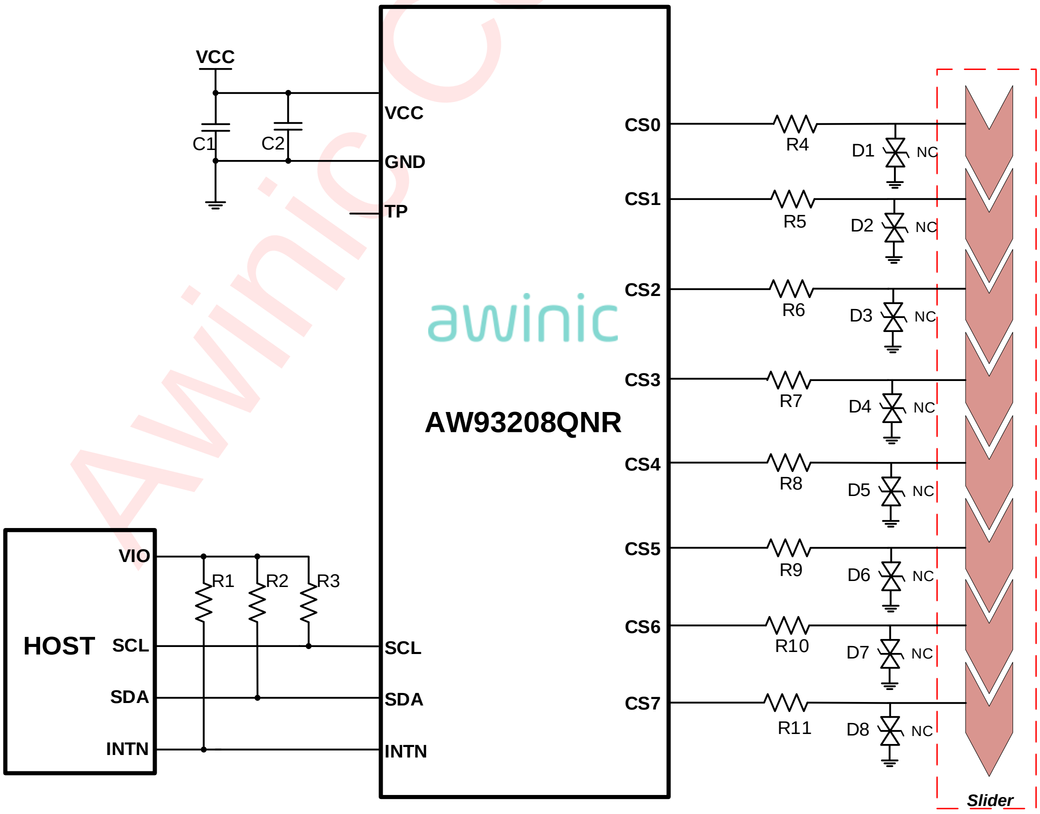


Figure 29 AW93208QNR Typical Application Circuit (slide)

Capacitors Selection

The recommended value of the capacitance C1 is 1μF and C2 is 0.1μF.

Resistor Selection

The recommended values of the resistor R1~R3 , which were applied in SCL,SDA and INTN pins, are 4.7kΩ. The recommended values of the resistor R4~R11, which were applied in CS0~7 pin, are 1kΩ.

Recommended Components List

Component	Name	Description	TYP.	Unit
C	C1	-	1	μF
	C2	-	0.1	μF
R	R1~R3	5% resolution	4.7	kΩ
	R4~R11	5% resolution	1	kΩ

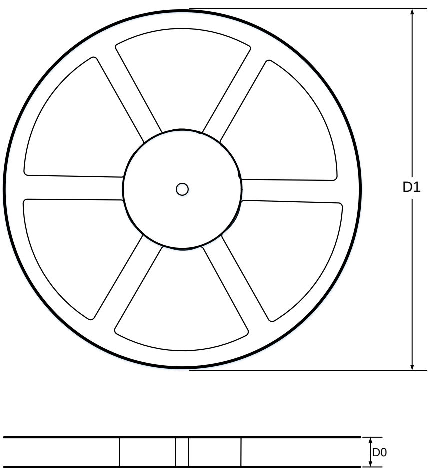
PCB Layout Consideration

AW93208QNR is a 8-channel capacitive wear detection and touch key controller, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

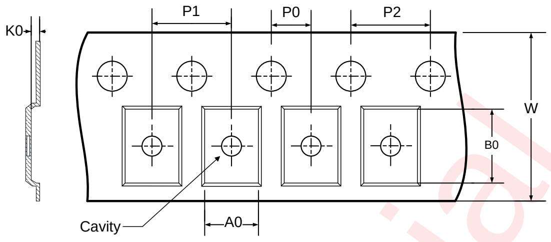
1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC.
2. Place the chip close to capacitive sensor and make trace as short as possible.
3. Make sure the sensor and traces be away from mic, earphone line in case of disturbing audio line.
4. Place reference channel(in Figure 28, pins CS0, CS1 and CS6, CS7 as shown) along with sensor channel to get better performance.
5. In-ear detection channel and differential channel is recommended to use the differential lines.
6. Use LDO for VCC supply.

Tape And Reel Information

REEL DIMENSIONS

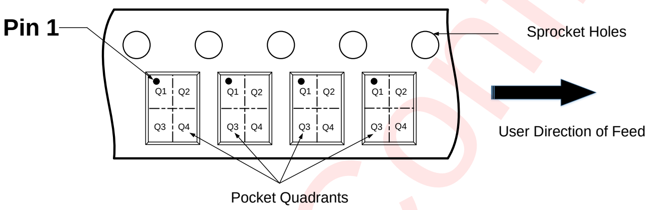


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



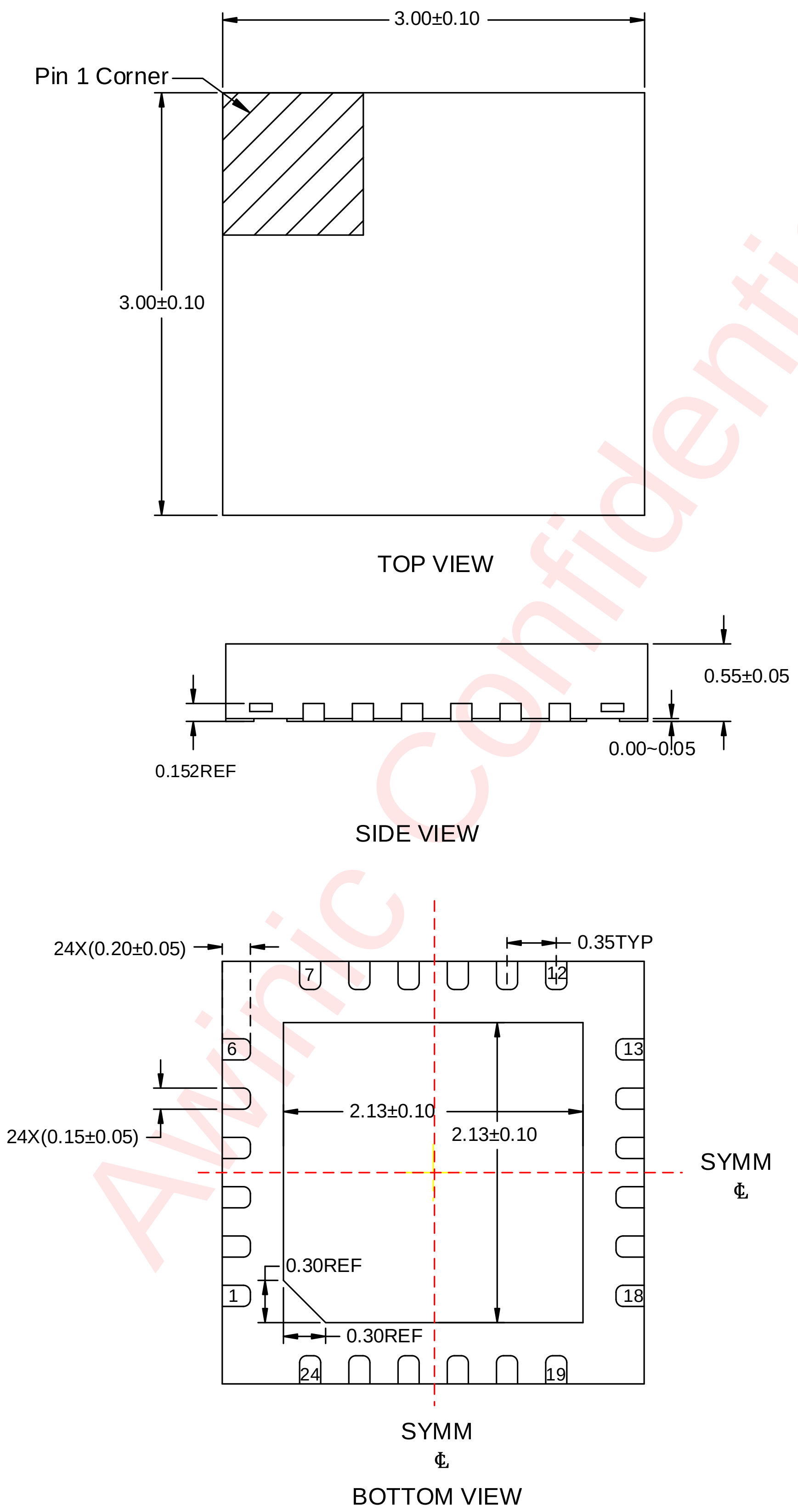
Note: The above picture is for reference only. Please refer to the value in the table below for te actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	3.30	3.30	0.80	2.00	8.00	4.00	12.00	Q1

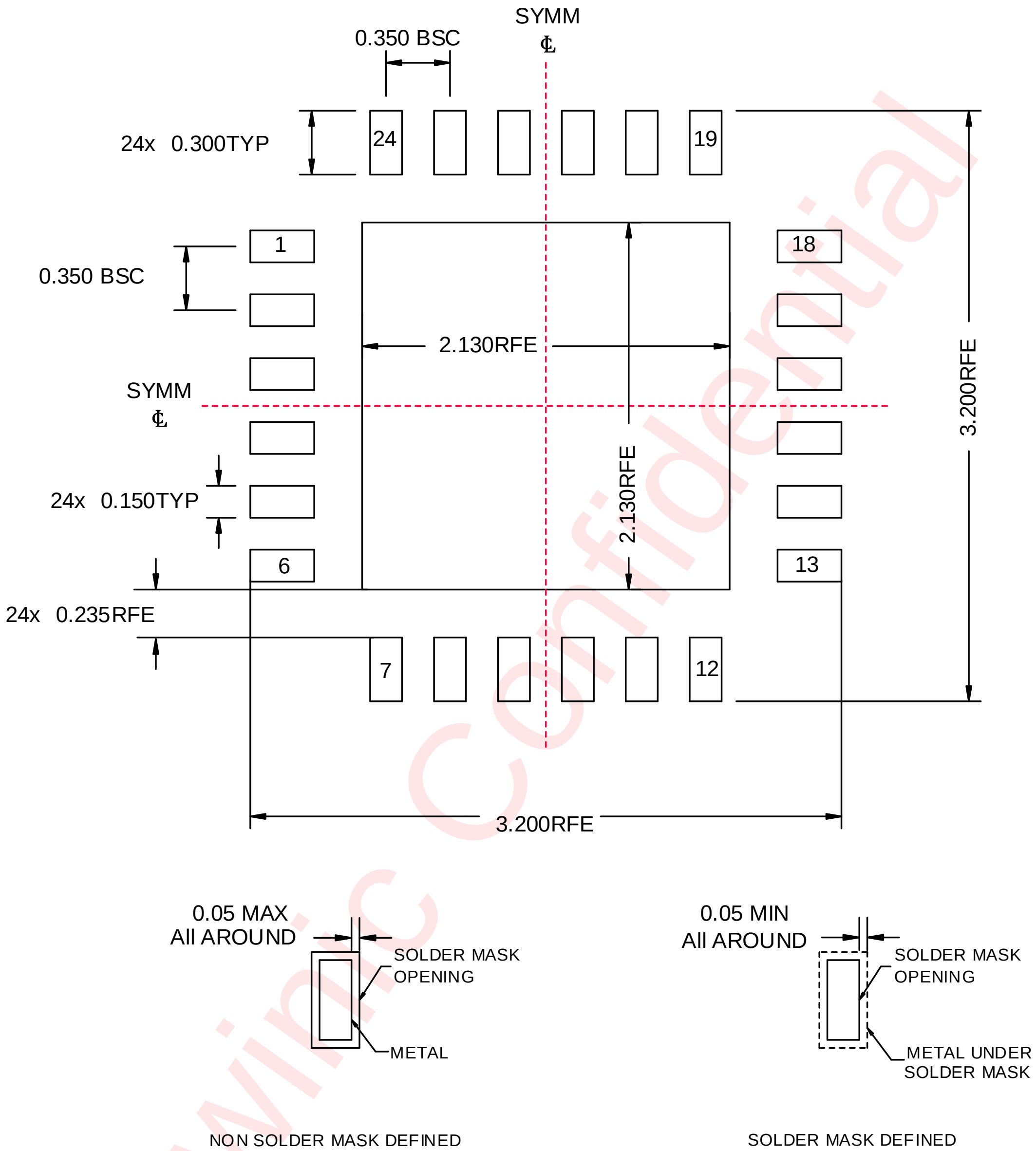
All dimensions are nominal

Package Description



Unit: mm

Land Pattern Data



Dimensions are all in millimeters

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun.2021	Officially released.
V1.1	Apr.2022	Modif gesture definitions.
V1.2	Nov.2023	1 Modify the package Definitions. (P1 and P4) 2 Modify the operating range. (P4~P6) 3 Modify the note of the figure 6. (P9) 4 Modify the value of the resistor (P23)
V1.3	Mar.2025	1 Update ordering information. 2 Update electrical characteristics. 3 Update I2C address extension voltage requirements.
V1.4	Jul.2025	Modify VIO voltage range. (P5)

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