0.1-5 GHz SP8T TRX Switch with MIPI

Features

- Broadband frequency range: 0.1 to 5 GHz
- Low insertion loss: 0.55dB typical @ 2.7 GHz
- High isolation: 35dB typical @ 2.7 GHz
- P0.1dB @ 38.5dBm
- MIPI RFFE V2.1 interface
- No DC blocking capacitors required (unless external DC is applied to the RF ports)
- QFN 1.65X1.65-16L package

General Description

The AW13508PQNR is a SP8T switch with low insertion loss and high isolation. It can be used to support band switching and mode switching in antenna transmit and receive systems for 2G/3G/4G/5G, data cards and tablets.

The AW13508PQNR is perfectly compatible with MIPI RFFE V2.1 control interface. It is provided in a compact QFN 1.65X1.65-16L package.

Applications

- Cellular 2G/3G/4G/5G TRx
- Cellular modems , tablets and USB Devices
- Other RF front-end modules

Typical Application Circuit

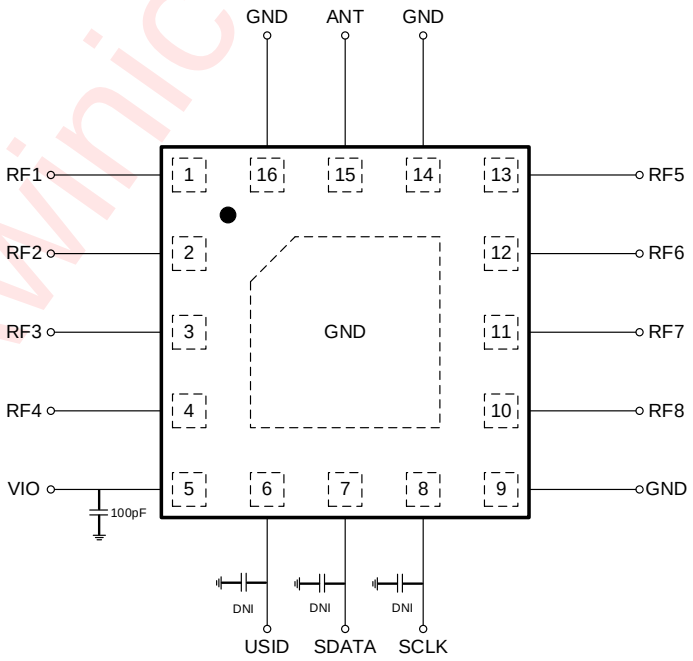
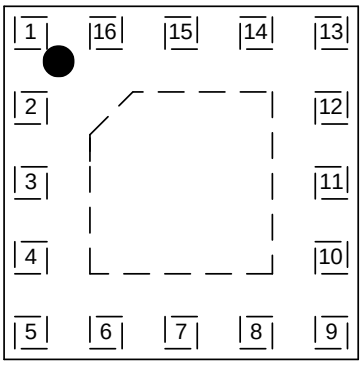


Figure 1 Typical Application Circuit of AW13508PQNR

Pin Configuration And Top Mark

AW13508PQNR
(Top View)



AW13508PQNR Marking
(Top View)

9S76 - AW13508PQNR
XXXX - Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	RF1	RF1 port
2	RF2	RF2 port
3	RF3	RF3 port
4	RF4	RF4 port
5	V_{IO}	Power supply
6	USID	MIPI used select port
7	SDATA	MIPI data input/output
8	SCLK	MIPI clock
9	GND	GND
10	RF8	RF8 port
11	RF7	RF7 port
12	RF6	RF6 port
13	RF5	RF5 port

No.	NAME	DESCRIPTION
14	GND	GND
15	ANT	Antenna port
16	GND	GND

Functional Block Diagram

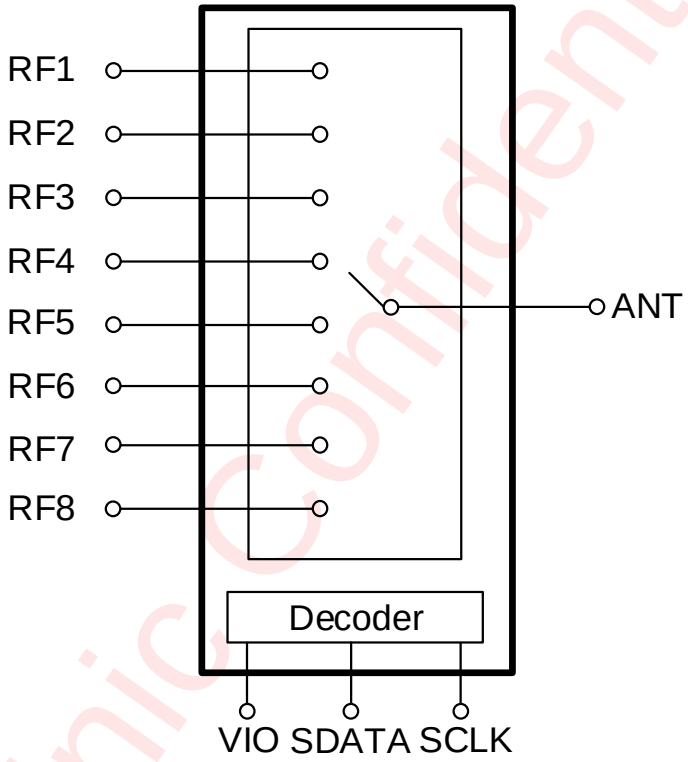


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13508PQNR	-40°C~105°C	QFN 1.65X1.65-16L	9S76	MSL1	RoHS+HF	4500 units/Tape and Reel

Absolute Maximum Ratings (NOTE 1)

PARAMETERS	RANGE
Interface Supply Voltage Range V_{IO}	-0.3V to 2.5V
Interface Control Voltage Range SDATA, SCLK	-0.3V to 2.5V
RF input power (RF1 to RF8) 25%DC,VSWR=1:1	40dBm
Operating Free-air Temperature Range	-40°C to 105°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM(Human Body Model)(NOTE 2)	±1000V
CDM (Charged Device Model) (NOTE 3)	±1000V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2022.

Electrical Characteristics

V_{IO}=1.8V, P_{IN}=0dBm, VSWR=1:1,Temp=25°C. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
V_{IO}	Supply Voltage		1.65	1.8	1.95	V
I_{VIO}	V_{IO} Supply Current	Active Mode		55	80	μA
		Low Power Mode		5	10	μA
V_{IH}	SDATA,SCLK Control Voltage High	Must not exceed V_{IO} voltage	0.8* V_{IO}	V_{IO}	1.95	V
V_{IL}	SDATA,SCLK Control Voltage Low	Must not exceed V_{IO} voltage	0	0	0.3*V_{IO}	V
T_{ON}	Wakeup Time	From end of Low Power State 50% SCLK to 90% of final RF power		10	20	μs
T_{SW}	Switching Speed One RF port to another	50% SCLK to 90% RF		0.8	2	μs
RF Specifications						
IL	Insertion loss (ANT pin to RF pins)	100-960MHz		0.35	0.45	dB
		960-2200MHz		0.47	0.65	dB
		2300-2700MHz		0.55	0.75	dB
		3300-3800MHz		0.75	0.95	dB
		3800-4200MHz		0.85	1.05	dB
		4400-5000MHz		1.15	1.4	dB
RL[1]	Return loss (ANT pin to RF pins)	100-960MHz	20	24		dB
		960-2200MHz	14	18		dB
		2300-2700MHz	13	16		dB
		3300-3800MHz	9	12		dB
		3800-4200MHz	8	11		dB
		4400-5000MHz	7	10		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ISO[1]	Isolation (ANT pin to RF pins, include adjacent port and non-adjacent port)	100-960MHz	37	47		dB
		960-2200MHz	30	37		dB
		2300-2700MHz	28	35		dB
		3300-3800MHz	23	32		dB
		3800-4200MHz	21	30		dB
		4400-5000MHz	19	26		dB
ISO	Isolation (RF pins to RF pins, include adjacent port and non-adjacent port)	100-960MHz	31	53		dB
		960-2200MHz	24	42		dB
		2300-2700MHz	22	39		dB
		3300-3800MHz	20	35		dB
		3800-4200MHz	18	34		dB
		4400-5000MHz	17	32		dB
$2f_0$	Second Harmonics (ANT pin to RF pins)	Freq@900MHz, P_{IN}=+35dBm,CW		-50	-40	dBm
$3f_0$	Third Harmonics (ANT pin to RF pins)	Freq@900MHz, P_{IN}=+35dBm,CW		-53	-43	dBm
$2f_0$[1]	Second Harmonics (ANT pin to RF pins)	Freq@1900MHz, P_{IN}=+33dBm,CW		-55	-45	dBm
$3f_0$[1]	Third Harmonics (ANT pin to RF pins)	Freq@1900MHz, P_{IN}=+33dBm,CW		-56	-45	dBm
$P_{0.1dB}$[1]	0.1dB Compression Point (ANT pin to RF pins)	0.1-5GHz		38.5		dBm

[1] Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Timing Diagram (Power On and Off Sequence)

1. Once V_{IO} is powered down to 0 V, wait at least 10 μs to reapply power to V_{IO}.

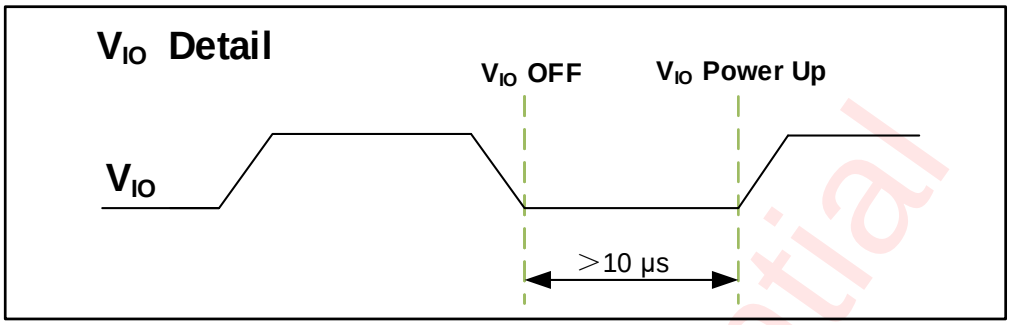


Figure 4 Digital Supply Detail

2. Before applying RF power , V_{IO} must be turned on for at least 20 μs.

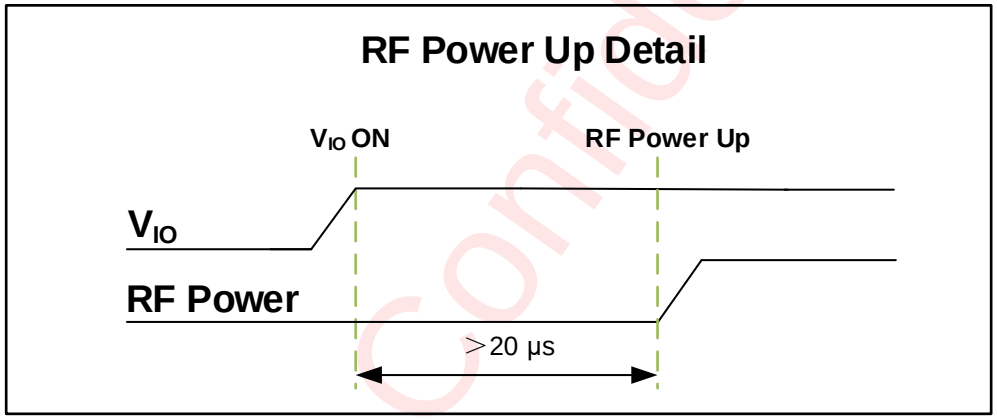


Figure 5 RF Power-Up Detail

3. Before sending SDATA/SCLK , V_{IO} must be applied for at least 800 ns to ensure correct data transmission. And after the RFFE bus is idle, wait at least 20 μs to apply the RF signal.

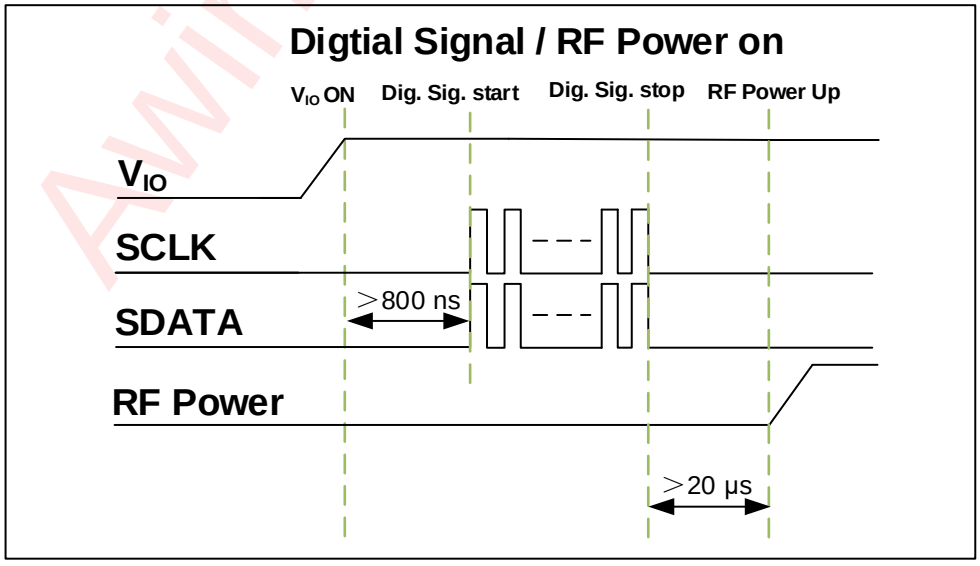


Figure 6 Digital Signal / RF Power-On Detail

4. There shall be no RFFE bus operations during RF Signal active to protect the device. So RF input signal shall be applied after RFFE bus operations being finished and be removed before RFFE bus operations being started.

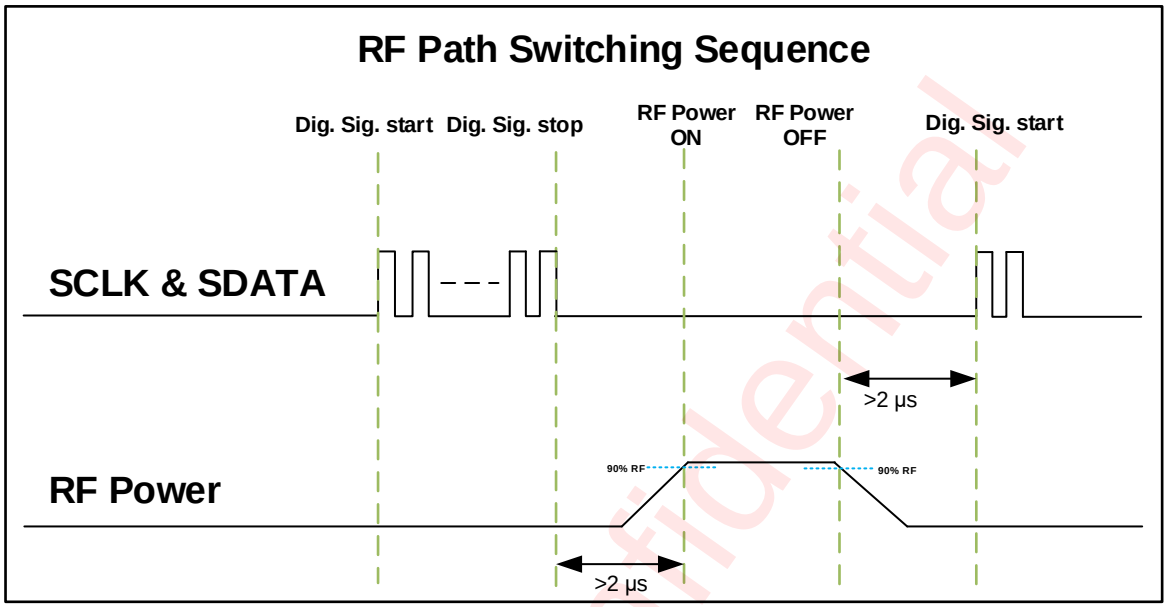


Figure 7 RF Path Switching Sequence

5. If “Lower Power Mode” is used, there must be a 10 µs delay before exiting “Lower Power Mode”.

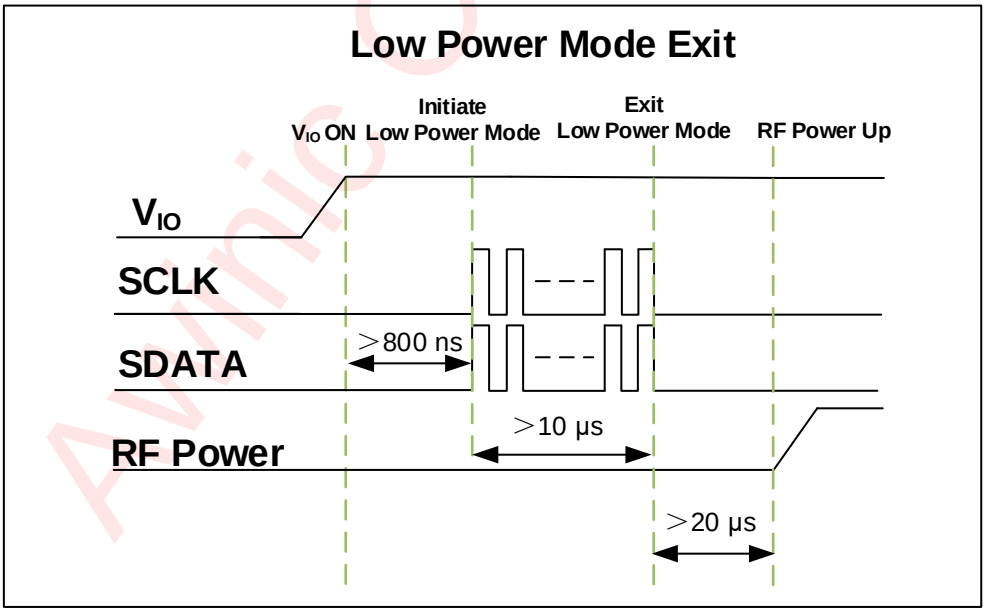


Figure 8 Lower Power Mode Exit Timing

MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

TABLE1: MIPI FEATURES

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	No	

TABLE2: Start-up Behavior

Feature	State	Comment
Power status	Low power mode	Low power mode after start-up
Trigger function	Enable	Enable after start-up. Programmable via register

MIPI Read and Write Timing

Register 0 Write:

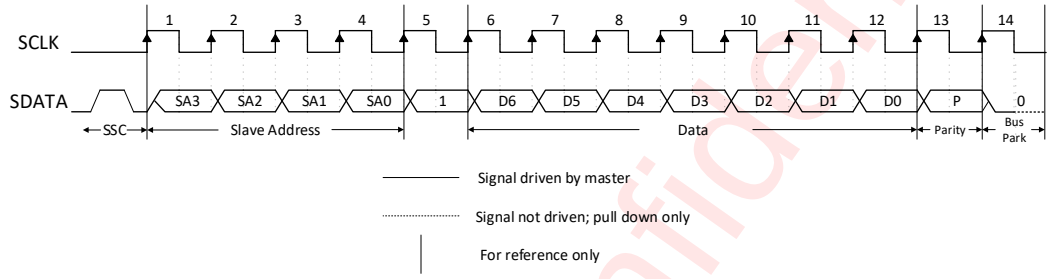


Figure 9 Register 0 Write Command Sequence

Register Write:

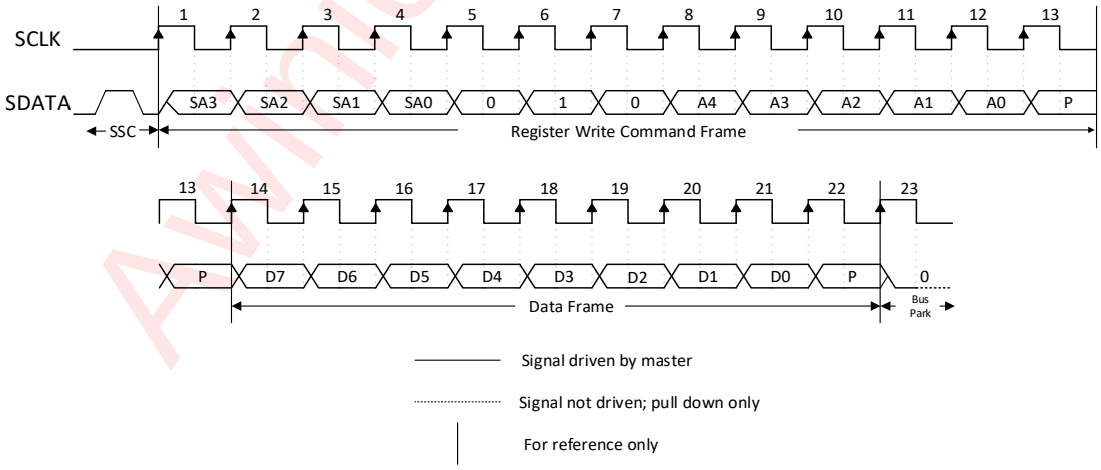


Figure 10 Register Write Command Sequence

Register Read:

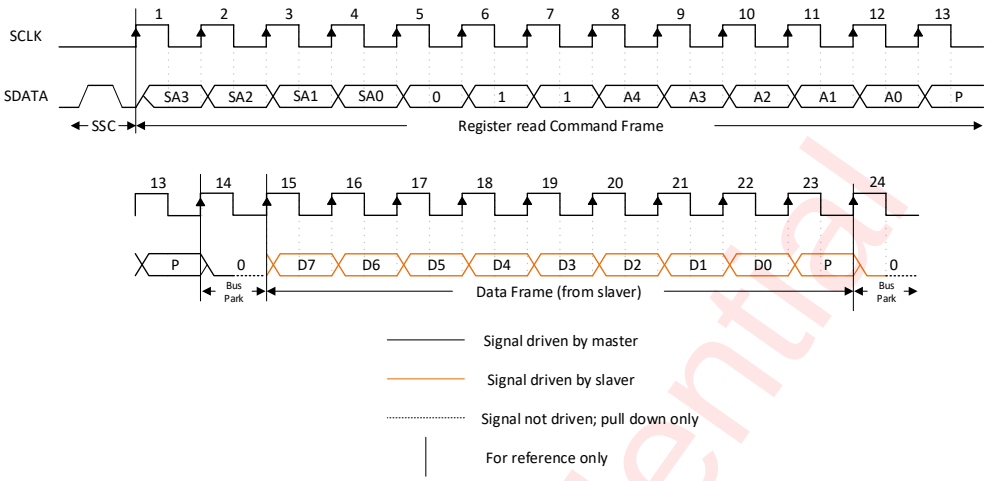


Figure 11 Register Read Command Sequence

Extended Register Write:

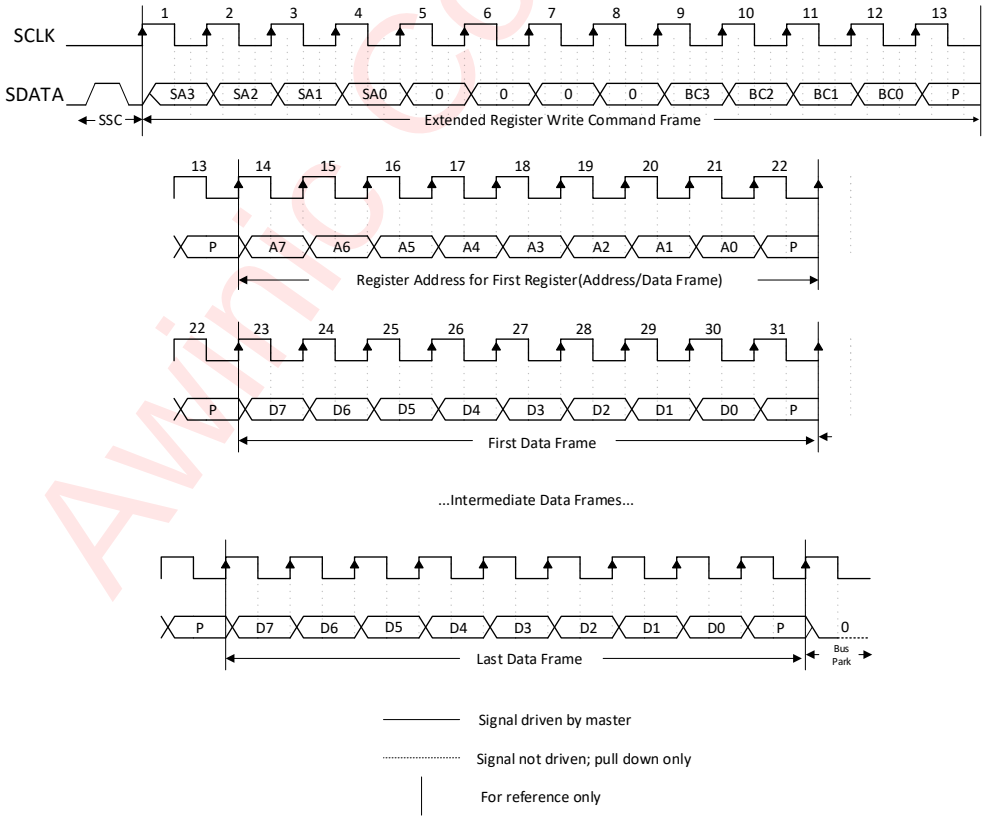


Figure 12 Extended Register Write Command Sequence

Extended Register Read:

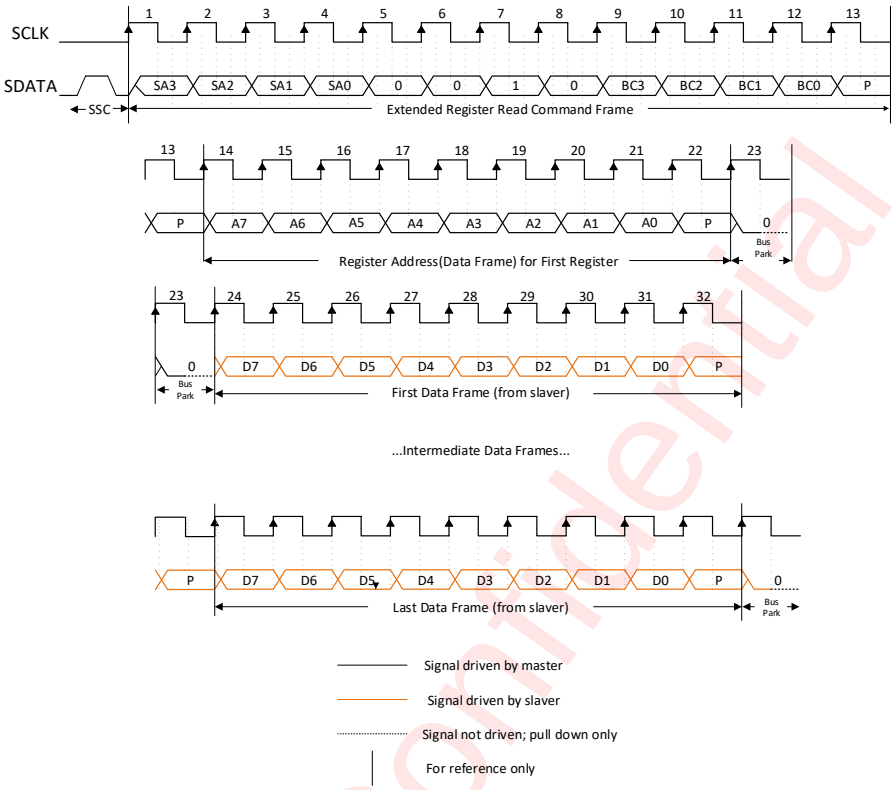


Figure 13 Extended Register Read Command Sequence

Masked Write:

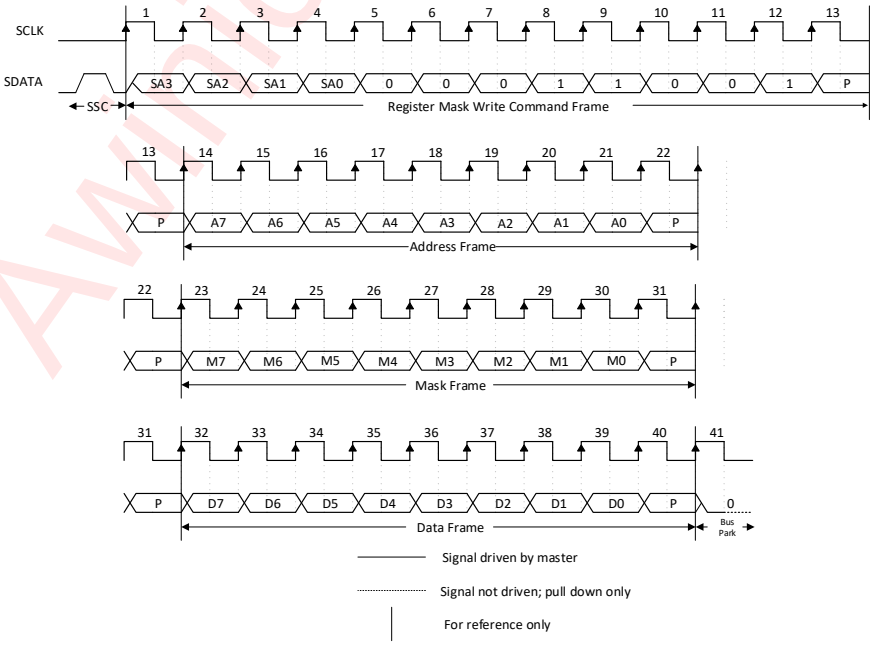


Figure 14 Masked Write Command Sequence

Register Configuration

Register Detailed Description

REGISTER_1：Mode Control Register(Address 0001h)

		Register_1 Bits							
State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
1	RF1 ON	×	×	×	×	×	×	×	1
2	RF2 ON	×	×	×	×	×	×	1	×
3	RF3 ON	×	×	×	×	×	1	×	×
4	RF4 ON	×	×	×	×	1	×	×	×
5	RF5 ON	×	×	×	1	×	×	×	×
6	RF6 ON	×	×	1	×	×	×	×	×
7	RF7 ON	×	1	×	×	×	×	×	×
8	RF8 ON	1	×	×	×	×	×	×	×
9	ALL OFF	0	0	0	0	0	0	0	0

RFFE_STATUS：RFFE Status Register(Address 001Ah)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal operation 1: software reset	W	No	No	0
6	CMD_FR_P_ERR	Command Frame received with a parity error	RW	No	No	0
5	CMD_LEN ERR	Command Sequence received with an incorrect length	RW	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	RW	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	RW	No	No	0
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	RW	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	RW	No	No	0
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	RW	No	No	0

GSID0_1：Group ID 0-1 Register(Address 001Bh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID0	Group Slave ID0	RW	No	No	0000
3:0	GSID1	Group Slave ID1	RW	No	No	0000

PM_TRIG：Pwr_mode and Trig Register(Address 001Ch)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	PWR_MODE[1]	0: normal operation 1: low power	RW MW	Yes	No	1
6	PWR_MODE[0]	0: active 1: start up – Reset all register to default	RW MW	Yes	No	0
5:3	TRIGGER_MASK	Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register	RW MW	No	No	000
2:0	TRIGGER	Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register	RW MW	Yes	No	000

PRODUCT_ID：Product ID Register(Address 001Dh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Lower eight bits of Product ID	R	No	No	0x1F

MANUFACTURER_ID：Manufacture ID Register(Address 001Eh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	MFG_ID	Lower eight bits of Manufacturer ID	R	No	No	0x49

MAN_USID：User ID Register(Address 001Fh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	MFG_ID	Upper four bits of Manufacturer ID	R	No	No	0000
3:0	USID	USID pin connected to GND	RW	No	No	0001
		USID pin floated				0001
		USID pin connected to VIO				0011

EXT_PRODUCT_ID：Extend Product ID Register(Address 0020h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Upper eight bits of Product ID	R	No	No	0x00

REVISION_ID：Revision ID Register(Address 0021h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	REV_ID	Revision ID	R	No	No	0x00

GSID2_3：Group ID 2-3 Register(Address 0022h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID2	Group Slave ID2	R/W	No	No	0000
3:0	GSID3	Group Slave ID3	R/W	No	No	0000

UDR_RST：UDR Reset Register(Address 0023h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal 1: software reset	R/W	Yes	No	0
6:0	RESERVED	Reserved	R/W	No	No	0x00

ERR_SUM：Error Command Status Register(Address 0024h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	SPARE	Reserved for future use	R/W	No	No	0
6	COM_FR_P_ERR	Command Frame received with a parity error	R/W	No	No	0
5	COM_LEN_ERR	Command Sequence received with an incorrect length	R/W	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	R/W	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	R/W	No	No	0
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	R/W	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	R/W	No	No	0
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	R/W	No	No	0

BUS_LD：SDATA Driver Strength Register(Address 002Bh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:1	reserved	reserved	R/W	No	No	0x00

0	BUS_LD	SDATA drive strength 0: 50pf 1: 80pf	R/W	No	No	0

EXT_TRIG_MASK：Extend Trig Mask Register(Address 002Dh)

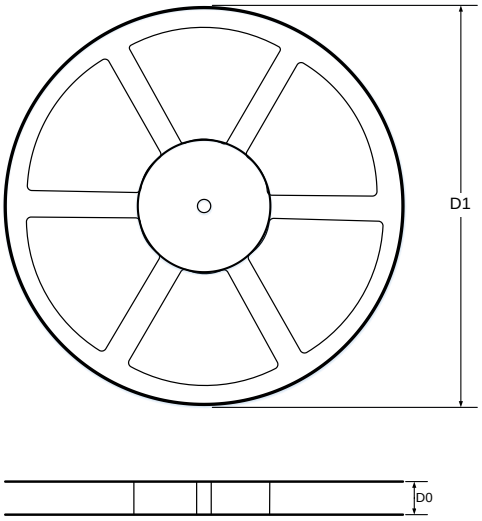
Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	EXT_TRIG_MASK	Setting bit EXT_TRIG_MASK[n] disables EXT_TRIG[n]	RW MW	No	No	0xFF

EXT_TRIG：Extend Trig Register(Address 002Eh)

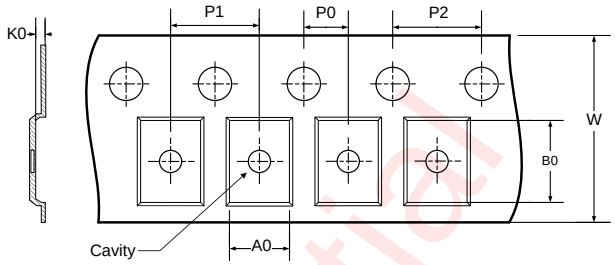
Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	EXT_TRIG	Setting bit EXT_TRIG[n] loads EXT_TRIG[n]'s associated register	R/W MW	Yes	No	0x00

Tape And Reel Information

REEL DIMENSIONS

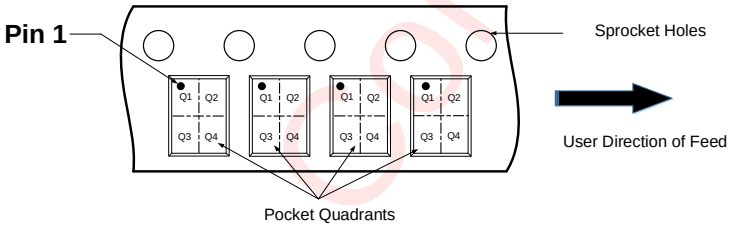


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	8.6	1.8	1.8	0.7	2	4	4	8	Q1

All dimensions are nominal

Figure 15 Tape and Reel

Package Description

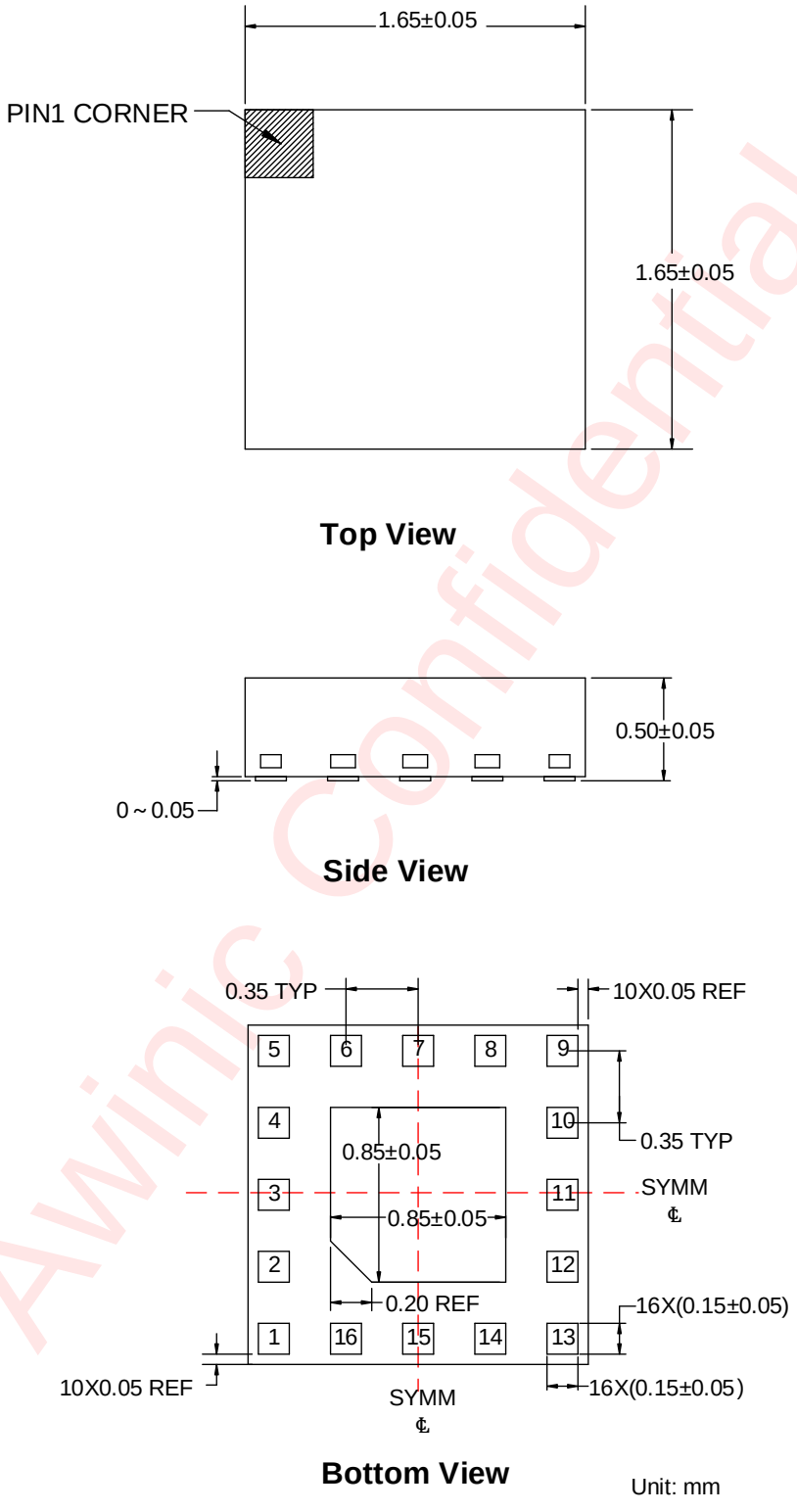


Figure 16 Package Outline

Land Pattern Data

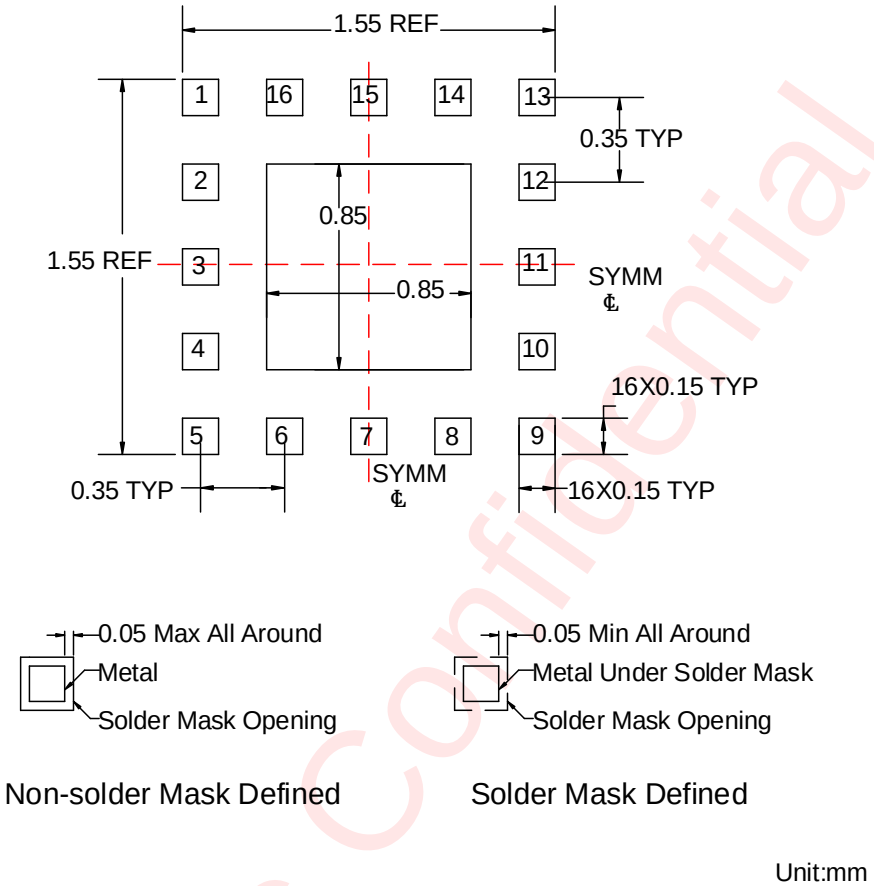


Figure 17 Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Jul 2025	Officially Released

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