7-Channel LDO PMIC For Camera Applications

Features

- VIN12 input voltage range: 0.6V to 3V
- LDO1/2 output voltage range: 0.496V~1.512V@8mV/step
- LDO1/2 dropout voltage: 120mV@1.2V, 1.5A
- LDO1/2 output drive capability: 1.5A
- LDO1/2 PSRR to VINx: typical 78dB (I_{OUT}=150mA, freq=1kHz)
- LDO1/2 PSRR to VSYS: typical 80dB (I_{OUT}=150mA, freq=1kHz)
- VIN34~VIN7 input voltage range: 1.8V to 5.5V
- LDO3~7 output voltage range: 1.504V~3.544V@8mV/step
- LDO3/4/6 dropout: 100mV@2.8V, 300mA
- LDO5/7 dropout: 135mV@2.8V, 600mA
- LDO3/4/6 output drive capability: 400mA
- LDO5/7 output drive capability: 700mA
- LDO3~7 PSRR to VSYS: typical 95dB (I_{OUT}=100mA, freq=1kHz)
- LDO3~7 PSRR to VINx: typical 92dB (I_{OUT}=100mA, freq=1kHz)
- LDO3~7 noise: typical 10μVrms (I_{OUT}=20mA, BW=10Hz to 100kHz)
- VSYS input voltage range: 2.5V to 5.5V
- Fault Interrupt
- Built-in OCP, OTP, UVP and UVLO protection
- Programmable power up sequence
- WLCSP 1.821mm×1.405mm-20B package

Applications

Digital camera

Smart phone

Camera module

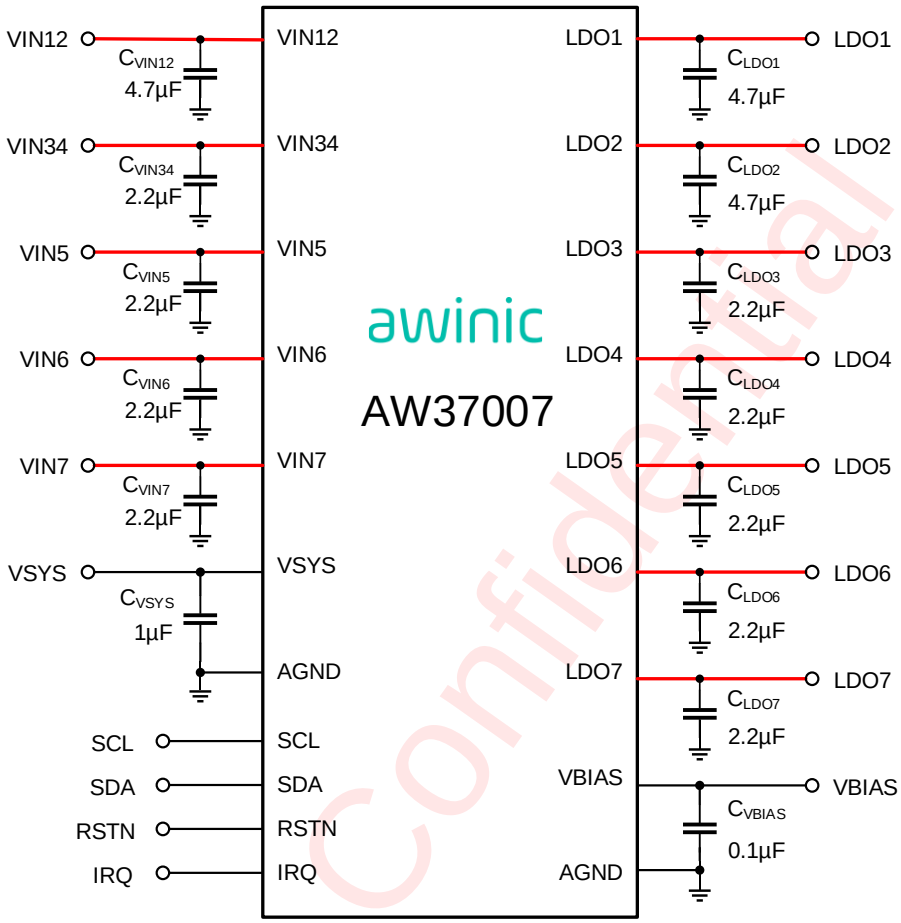
General Description

AW37007 is a 7-ch integrated LDO PMIC for camera applications. The PMIC has 2 low dropout LDOs for high current DVDD and 5 high PSRR LDOs for noise-sensitive power rails. The AW37007 has 5 independent input pins for individual LDOs; VIN12 is for LDO1 and LDO2; VIN34 is for LDO3 and LDO4; VIN5 for LDO5, VIN6 for LDO6 and VIN7 for LDO7. The AW37007 has a separate system input, VSYS, which is the bias pin for the LDOs.

The output voltage and power-up sequence of LDOs can be set through the I^2C interface. The AW37007 also integrates the fault monitoring features with interrupt indication.

The 7-bit I^2C address of the device is 011 0101 by default but can be reprogrammed so that multiple devices can be connected to the same I^2C bus. The AW37007 is available in WLCSP 1.821mm × 1.405mm-20B package.

Typical Application Circuit



Typical Application Circuit

Note:

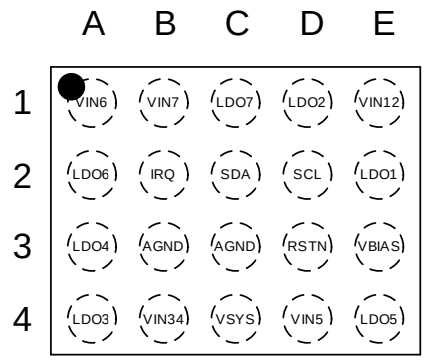
1. The recommended output capacitor is 4.7μF for C_{LDO1-2} and 2.2μF for C_{LDO3-7}. Considering capacitance changes with temperature, DC bias and package size, the minimum effective capacitance for C_{LDO1-2} is 2μF, and the minimum effective capacitance for C_{LDO3-7} is 0.7μF.

2. Select a minimum input capacitance of 4.7μF for C_{VIN12} and 2.2μF for $C_{VIN34-7}$.

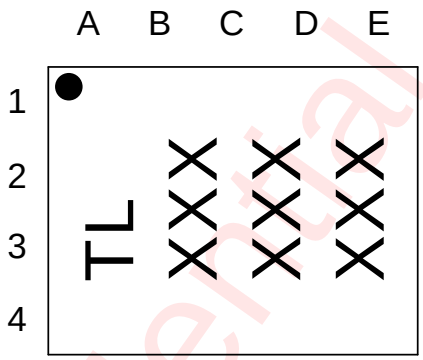
3. Select a minimum input capacitance of 1μF for C_{VSYS}. A capacitance of 1μF or higher can satisfy the requirement of all levels of V_{IN}, V_{OUT}, and load.

Pin Configuration And Top Mark

AW37007CSR
(Top View)



AW37007CSR Marking
(Top View)



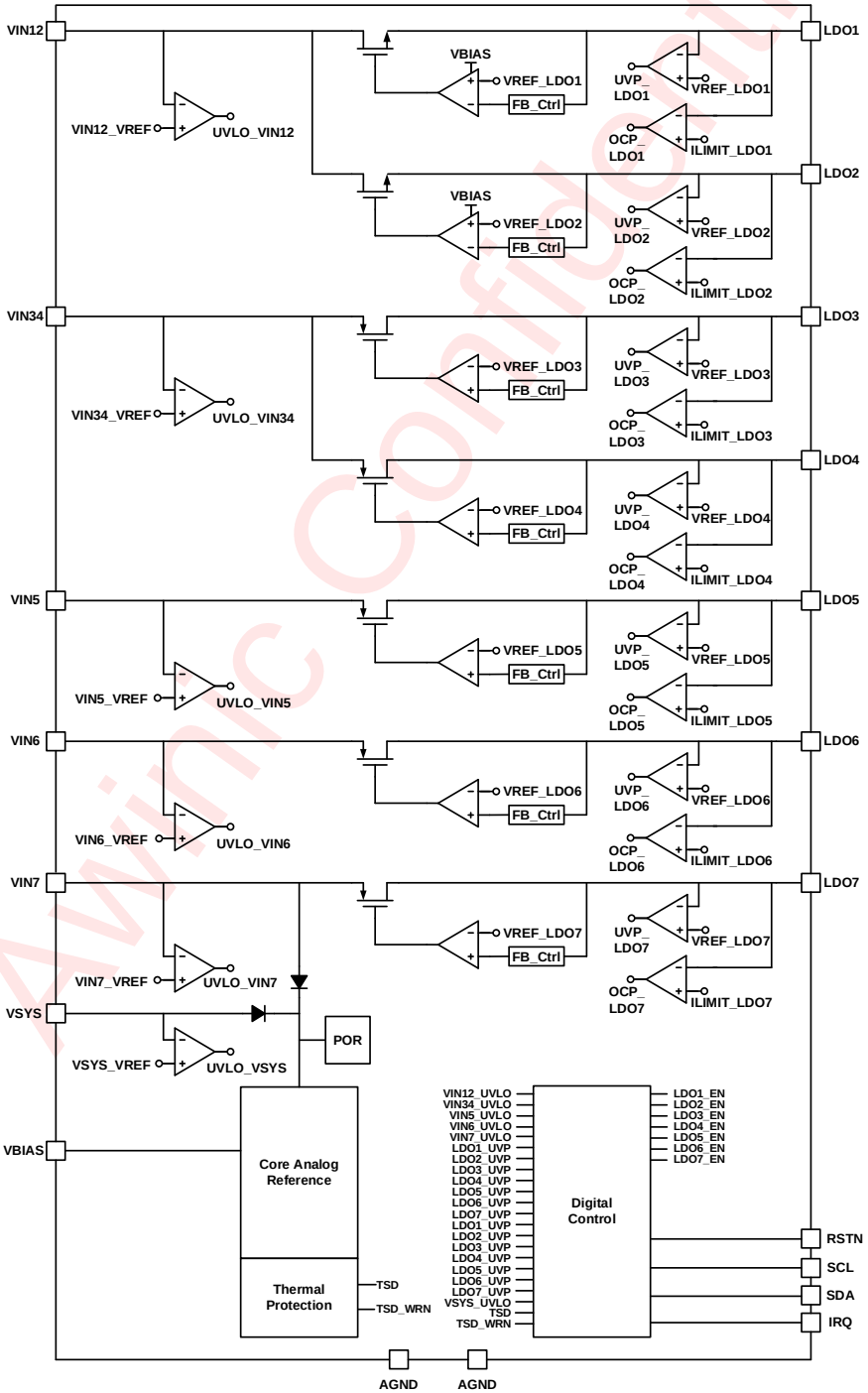
TL - AW37007CSR
XXX/XXX/XXX - Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
A1	VIN6	LDO6 input. Connecting a 2.2μF or more ceramic capacitor at the input pin.
A2	LDO6	LDO6 output. Connecting a 2.2μF or more ceramic capacitor at the output pin.
A3	LDO4	LDO4 output. Connecting a 2.2μF or more ceramic capacitor at the output pin.
A4	LDO3	LDO3 output. Connecting a 2.2μF or more ceramic capacitor at the output pin.
B1	VIN7	LDO7 input. Connecting a 2.2μF or more ceramic capacitor at the input pin.
B2	IRQ	Fault interrupt pin is active high indicating an interrupt event has occurred. This pin returns to low when all I^2C interrupt bits equal 0.
B3	AGND	Ground
B4	VIN34	LDO3 and LDO4 input. Connecting a 2.2μF or more ceramic capacitor at the input pin.
C1	LDO7	LDO7 output. Connecting a 2.2μF or more ceramic capacitor at the output pin.
C2	SDA	I^2C data pin. Node should be tied high through a pull up resistor.
C3	AGND	Ground
C4	VSYS	VSYS input. Connecting a 1μF or more ceramic capacitor at the input pin.
D1	LDO2	LDO2 output. Connecting a 4.7μF or more ceramic capacitor at the output pin.
D2	SCL	I^2C clock pin. Node should be tied high through a pull up resistor.
D3	RSTN	RSTN pin is used to enable basic circuits necessary for controlling the PMIC. The pin has an internal 10MΩ (typ.) pull-down and should always be connected to a logic high or low.
D4	VIN5	LDO5 input. Connecting a 2.2μF or more ceramic capacitor at the input pin.

E1	VIN12	LDO1 and LDO2 input. Connecting a 4.7μF or more ceramic capacitor at the input pin.
E2	LDO1	LDO1 output. Connecting a 4.7μF or more ceramic capacitor at the output pin.
E3	VBIAS	Bias bypass pin. Connect a 0.1μF ~0.47μF capacitor between this pin and analog ground.
E4	LDO5	LDO5 output. Connecting a 2.2μF or more ceramic capacitor at the output pin.

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37007CSR	-40°C ~ 85°C	WLCSP 1.821mm× 1.405mm-20B	TL	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Input voltage range VSYS	-0.3V to 6.5V
Input voltage range VIN12	-0.3V to 4V
Input voltage range VIN34~VIN7	-0.3V to 6.5V
Control Pin (SCL, SDA, IRQ, RSTN) voltage range	-0.3V to V_{SYS} & V_{IN7}
Output voltage range	-0.3V to V_{INX}+0.3V, max. 6.5V
Junction-to-ambient thermal resistance θ_{JA}(NOTE2)	39.77°C/W
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model)(NOTE3)	±2kV
CDM(Charged device model) (NOTE4)	±1.5kV
Latch-Up	
Latch-Up(NOTE5)	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2023.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2022.

NOTE5: Test Condition: JESD78F.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{SYS}	VSYS Input Voltage Range	2.5		5.5	V
V_{IN12}	VIN12 Input Voltage Range	0.6		3	V
V_{IN34}, V_{IN5}, V_{IN6}, V_{IN7}	VIN3 to VIN7 Input Voltage Range	1.8		VSYS	V
T_J	Operating junction temperature	-40		125	°C
T_A	Operating free-air temperature range	-40		85	°C

Electrical Characteristics

V_{SYS}=2.5V to 5.5V, V_{IN12}=0.6V to 3V & V_{IN12}≥$V_{LDO1/2}$ + 200mV; $V_{IN34/5/6/7}$=1.8V to 5.5V & $V_{IN34/5/6/7}$≥ $V_{LDO3/4/5/6/7}$ + 300mV respectively. T_A=-40°C~85°C unless otherwise noted. Typical values are at T_A = 25°C; V_{SYS}=3.8V, V_{IN12}=1.5V, V_{IN34}=V_{IN5}=V_{IN6}=V_{IN7}=3.6V, $V_{LDO1/2}$=1.2V, $V_{LDO3/4/5/6/7}$=2.8V. C_{VIN12}=4.7μF, C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=2.2μF, C_{VSYS}=1μF, C_{LDO1}=C_{LDO2}=4.7μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=2.2μF.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{SYS}	System Input Voltage Range		2.5		5.5	V
V_{IN12}	VIN12 Input Voltage Range		0.6		3	V
V_{IN34} V_{IN5} V_{IN6} V_{IN7}	VIN34~VIN7 Input Voltage Range		1.8		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy	$V_{LDO1/2}$=1.2V, T_A=25°C	-0.5		0.5	%
		$V_{LDO3/4/5/6/7}$=2.8V, T_A=25°C	-0.5		0.5	%
V_{VSYS_UVLO}	VSYS Under Voltage Lock-out	Rising			2.35	V
		Falling	2.1			V
V_{VIN12_UVLO}	VIN12 Under Voltage Lock-out	Rising			0.6	V
		Falling	0.4			V
$V_{VIN34/5/6/7\_UVLO}$	VIN34,5,6,7 Under Voltage Lock-out	Rising			1.8	V
		Falling	1.5			V
I_{GND}	Quiescent Current	RSTN=5.5V, all channels are OFF		44		μA
		LDO1 is "ON"		57		μA
		LDO1&2 are "ON"		73		μA
		LDO1,2&3 are "ON"		92		μA
		LDO1,2,3&4 are "ON"		110		μA
		LDO1,2,3,4&5 are "ON"		128		μA
		LDO1,2,3,4,5&6 are "ON"		145		μA
		LDO1,2,3,4,5,6&7 are "ON"		163		μA
		RSTN=5.5V, Disable IC through I^2C		2.5		μA
I_{SD}	Shutdown Current	RSTN=0V		1.5		μA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
LDO1,2	Output Voltage Range	When V_{IN12}≥V_{OUT}+0.2V, V_{SYS}≥2.5V & V_{SYS}≥V_{OUT}+1.6V	0.496		1.512	V
LDO3,4,5,6		When $V_{IN34/5/6}$≥V_{OUT}+0.3V & $V_{IN34/5/6}$≥1.8V, V_{SYS}≥2.5V & V_{SYS} ≥ $V_{IN34/5/6}$	1.504		3.544	V
LDO7		When V_{IN7}≥V_{OUT}+0.3V & V_{IN7}≥1.8V. V_{SYS}≥2.5V				
$Vdrop_{LDO1,2}$	Dropout Voltage	I_{OUT}=1500mA, V_{OUT_SET}=1.2V, V_{SYS}=3.6V, V_{OUT}=0.98*V_{OUT_SET}		120		mV
$Vdrop_{LDO3,4,6}$		I_{OUT}=300mA, V_{OUT_SET}=2.8V, V_{SYS}=3.6V, V_{OUT}=0.98*V_{OUT_SET}		100		mV
$Vdrop_{LDO5,7}$		I_{OUT}=600mA, V_{OUT_SET}=2.8V, V_{SYS}=3.6V, V_{OUT}=0.98*V_{OUT_SET}		135		mV
$I_{CL\_LDO1,2}$	Output Current Limit	V_{OUT}=90%V_{OUT_SET}, 0x02 Bit[0 or 1]=0	1200			mA
		V_{OUT}=90%V_{OUT_SET}, 0x02 Bit[0 or 1]=1	1500			
$I_{CL\_LDO3,4,6}$		V_{OUT}=90%V_{OUT_SET}, 0x02 Bit[2 or 3 or 5]=0	400			mA
		V_{OUT}=90%V_{OUT_SET}, 0x02 Bit[2 or 3 or 5]=1	600			
$I_{CL\_LDO5,7}$		V_{OUT}=90%V_{OUT_SET}, 0x02 Bit[4 or 6]=0	500			mA
		V_{OUT}=90%V_{OUT_SET}, 0x02 Bit[4 or 6]=1	700			
$I_{SC\_LDO1,2}$	Short Current Limit	0x02 Bit[0 or 1]=0		340		mA
		0x02 Bit[0 or 1]=1		450		
$I_{SC\_LDO3,4,6}$		0x02 Bit[2 or 3 or 5]=0		290		mA
		0x02 Bit[2 or 3 or 5]=1		437		
$I_{SC\_LDO5,7}$		0x02 Bit[4 or 6]=0		335		mA
		0x02 Bit[4 or 6]=1		470		
Line_Reg_ $VSYS_{LDO1,2}$	Line Regulation of VSYS	V_{OUT_SET}=1.2V, I_{OUT}=1mA , V_{IN12}=1.5V, V_{SYS}=3.5V~5.5V		0.5	6	mV
Line_Reg_ $VSYS_{LDO3,4,5,6,7}$		V_{OUT_SET}=2.8V, I_{OUT}=1mA, V_{INX}=3.3V, V_{SYS}=3.5V~5.5V		0.1	6	mV
Line_Reg_ $VIN_{LDO1,2}$	Line Regulation of VIN	V_{OUT_SET}=1.2V, I_{OUT}=1mA, V_{SYS}=5.5V, V_{IN12}=1.5V~3V		0.2	6	mV
Line_Reg_ $VIN_{LDO3,4,5,6,7}$		V_{OUT_SET}=2.8V, I_{OUT}=1mA, V_{SYS}=5.5V, V_{IN12}=3.5V~5.5V		0.1	6	mV

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
Load_Reg LDO1,2	Load Regulation	I_{OUT}=1mA~1000mA			4		mV
Load_Reg LDO3,4,5,6,7		I_{OUT}=1mA~300mA			2		mV
$T_{ON\_LDO1,2}$	Turn-On Time	From assertion of Enable Signal to 5% V_{OUT}	V_{OUT}=1.2V, C_{OUT}=4.7μF		75		μs
$T_{ON\_LDO3,4,6}$			V_{OUT}=2.8V C_{OUT}=2.2μF		220		μs
$T_{ON\_LDO5,7}$			V_{OUT}=2.8V C_{OUT}=2.2μF		135		μs
$T_{R\_LDO1,2}$	Soft Start Time	V_{OUT} from 5% to 90% V_{OUT}	V_{OUT}=1.2V, C_{OUT}=4.7μF		180		μs
$T_{R\_LDO3,4,6}$			V_{OUT}=2.8V C_{OUT}=2.2μF		75		μs
$T_{R\_LDO5,7}$			V_{OUT}=2.8V C_{OUT}=2.2μF		70		μs
$V_{N\_LDO1,2}$	Output noise	I_{OUT}=20mA, BW=10Hz to 100kHz	V_{IN12}=1.5V, V_{OUT}=1.2V		80		μVrms
$V_{N\_LDO3,4,5,6,7}$			V_{IN}=3.6V, V_{OUT}=2.8V		10		μVrms
$PSRR_{LDO1,2}$	Power Supply Ripple Rejection on VSYS	LDO1,2 (V_{SYS} to V_{OUT}) V_{IN12}=1.5V, V_{SYS}=3.8V+0.2V_{PP}, I_{OUT}=150mA, C_{OUT}=4.7uF	f=100Hz		73		dB
			f=1kHz		78		
			f=10kHz		75		
			f=100kHz		54		
			f=1MHz		60		
	Power Supply Ripple Rejection on VIN12	LDO1,2 (V_{IN12} to V_{OUT}) V_{IN12}=1.5V+0.2V_{PP}, V_{SYS}=3.8V, I_{OUT}=150mA, C_{OUT}=4.7uF	f=100Hz		75		dB
			f=1kHz		78		
			f=10kHz		60		
			f=100kHz		46		
			f=1MHz		38		
$PSRR_{LDO3,4,6}$	Power Supply Ripple Rejection on VSYS	LDO3,4,6 (V_{SYS} to V_{OUT}) V_{IN12}=1.5V, $V_{IN34,6}$=3.6V,	f=100Hz		95		dB
			f=1kHz		95		
			f=10kHz		85		

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
		V_{SYS}=3.8V+0.2V_{PP}, I_{OUT}=100mA, C_{OUT}=2.2uF	f=100kHz		70		
			f=1MHz		56		
	Power Supply Ripple Rejection on VIN34,6	LDO3,4,6 ($V_{IN34,6}$ to V_{OUT}) $V_{IN34,6}$=3.6V+0.2V_{PP}, V_{SYS}=3.8V, I_{OUT}=100mA, C_{OUT}=2.2uF	f=100Hz		90		dB
			f=1kHz		92		
			f=10kHz		85		
			f=100kHz		70		
			f=1MHz		50		
$PSRR_{LDO5,7}$	Power Supply Ripple Rejection on VSYS	LDO5,7 (V_{SYS} to V_{OUT}) V_{IN12}=1.5V, $V_{IN5,7}$=3.6V, V_{SYS}=3.8V+0.2V_{PP}, I_{OUT}=100mA, C_{OUT}=2.2uF	f=100Hz		95		dB
			f=1kHz		95		
			f=10kHz		84		
			f=100kHz		70		
			f=1MHz		60		
	Power Supply Ripple Rejection on VIN5,7	LDO5,7 ($V_{IN5,7}$ to V_{OUT}) $V_{IN5,7}$=3.6V+0.2V_{PP}, V_{SYS}=3.8V, I_{OUT}=100mA, C_{OUT}=2.2uF	f=100Hz		86		dB
			f=1kHz		95		
			f=10kHz		85		
			f=100kHz		70		
			f=1MHz		51		
$R_{DISC\_LDO1,2}$	Auto Discharge Resistance				122		Ω
$R_{DISC\_LDO3,4,5,6,7}$					125		Ω
T_{WRN}	Thermal warning	Temperature Rising			115		°C
T_{SD}	Thermal Shutdown	Temperature Rising			155		°C
T_{HYS}	Thermal hysteresis for T_{SD} and T_{WRN}				25		°C
RSTN Logic Inputs							
R_{RSTN}	RSTN Pull Down Resistance				10		MΩ
V_{IH}	Input High Voltage			0.84			V

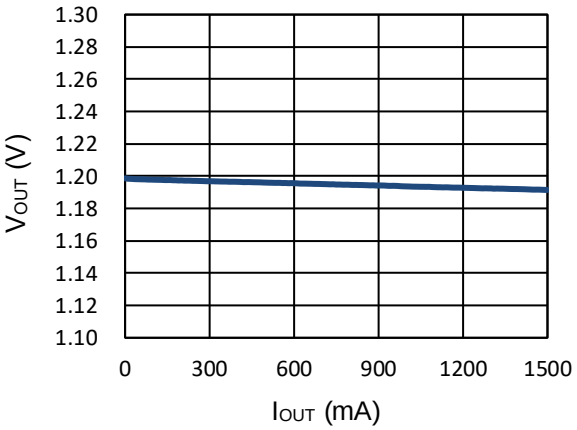
PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage					0.36	V
IRQ Logic Inputs							
V_{OH}	Output High Voltage for Push-pull Mode	I_{OUT}=5mA	0x12 Bit7=1		1.15		V
			0x12 Bit7=0		1.81		V
V_{OL}	Output Low Voltage for Open-drain Mode	I_{OUT}=5mA				0.3	V
I^2C Logic(1)							
I_{LEAK}	Input Leakage				0.1	0.2	μA
V_{IH}	Input High Voltage			0.84			V
V_{IL}	Input Low Voltage					0.36	V
f_{SCL}	Interface clock frequency			100	400	1000	kHz

Note1:Minimun and maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Typical Characteristics

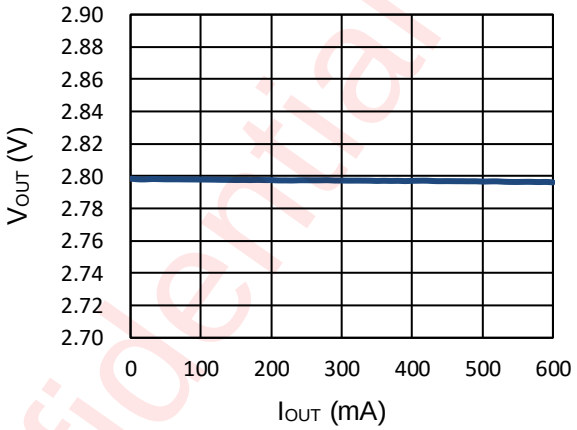
V_{SYS}=3.8V, V_{IN12}=1.5V, V_{IN34}=V_{IN5}=V_{IN6}=V_{IN7}=3.6V, $V_{LDO1/2}$=1.2V, $V_{LDO3/4/5/6/7}$=2.8V. C_{VIN12}=4.7μF, C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=2.2μF, C_{VSYS}=1μF, C_{LDO1}=C_{LDO2}=4.7μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=2.2μF, T_A=25°C, unless otherwise noted.

LDO1/2



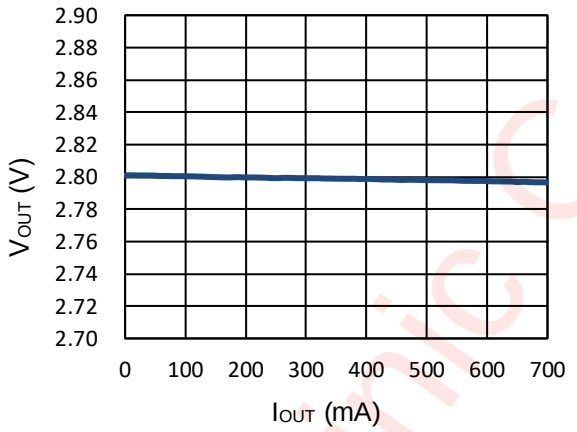
Output Voltage vs Output Current

LDO3/4/6



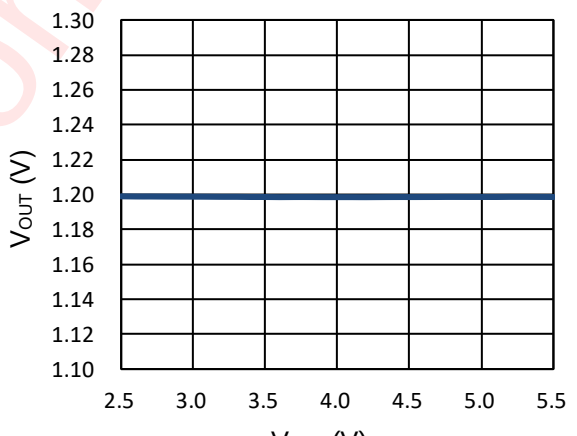
Output Voltage vs Output Current

LDO5/7



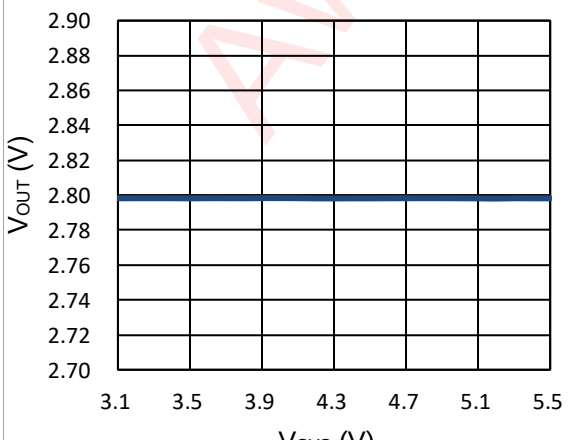
Output Voltage vs Output Current

LDO1/2



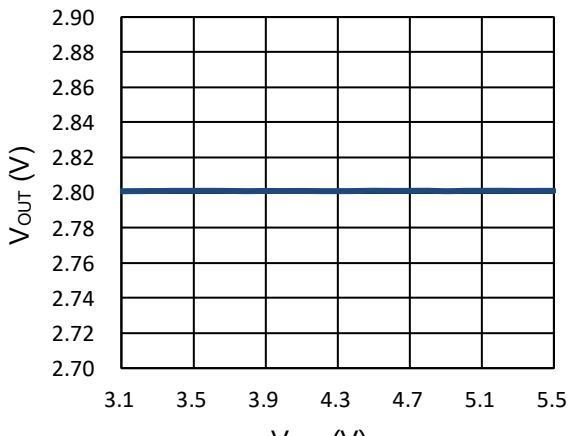
Output Voltage vs VSYS Voltage

LDO3/4/6



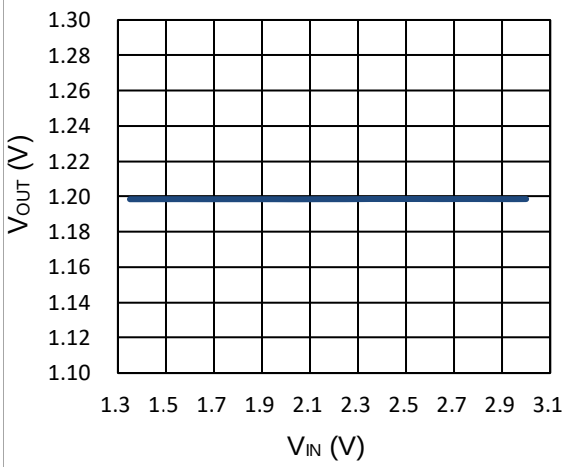
Output Voltage vs VSYS Voltage

LDO5/7



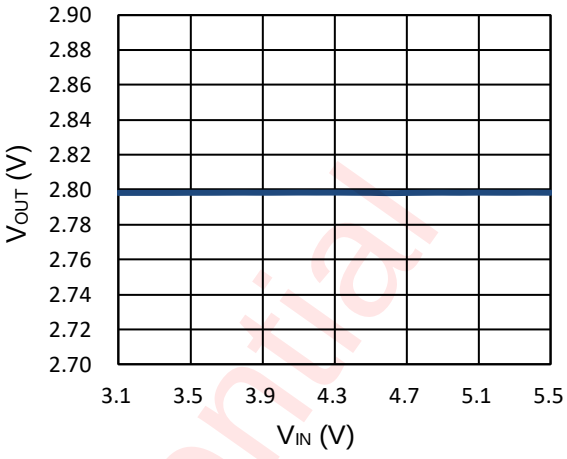
Output Voltage vs VSYS Voltage

LDO1/2



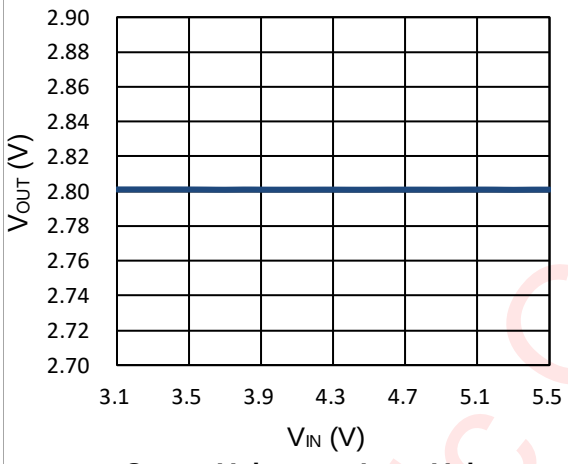
Output Voltage vs Input Voltage

LDO3/4/6



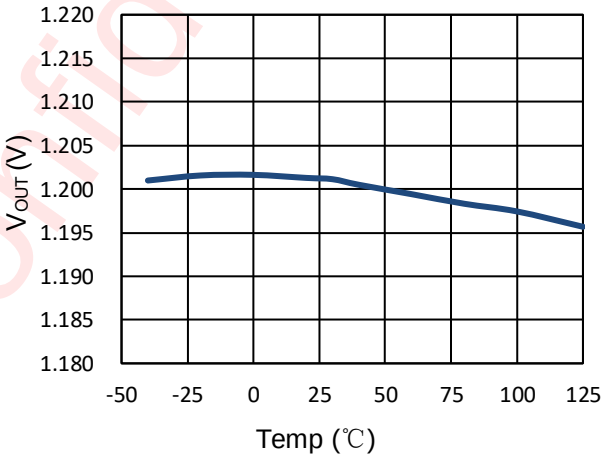
Output Voltage vs Input Voltage

LDO5/7



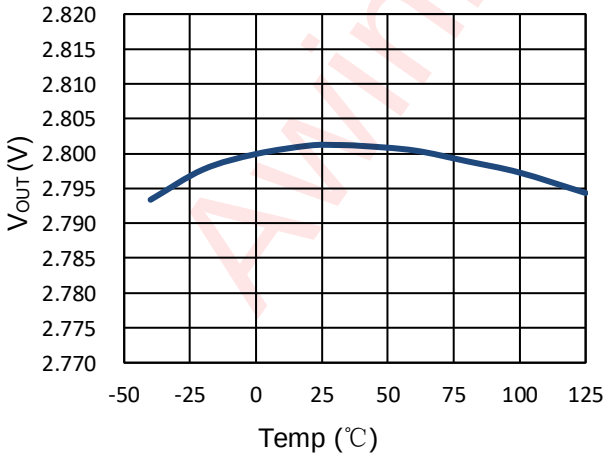
Output Voltage vs Input Voltage

LDO1/2



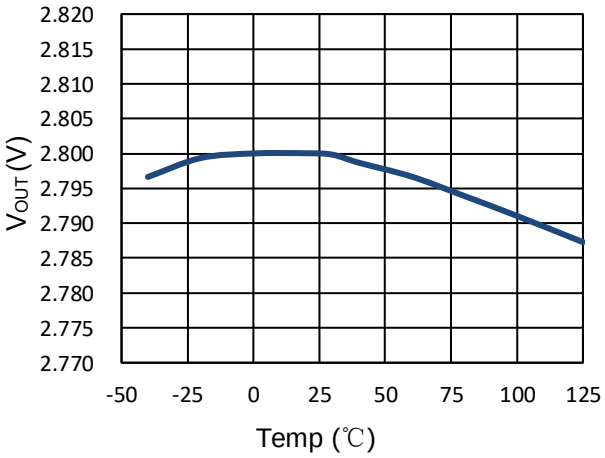
Output Voltage vs Temperature

LDO3/4/6



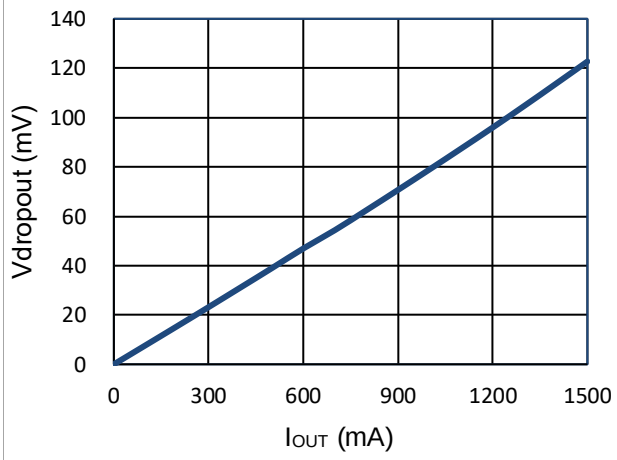
Output Voltage vs Temperature

LDO5/7



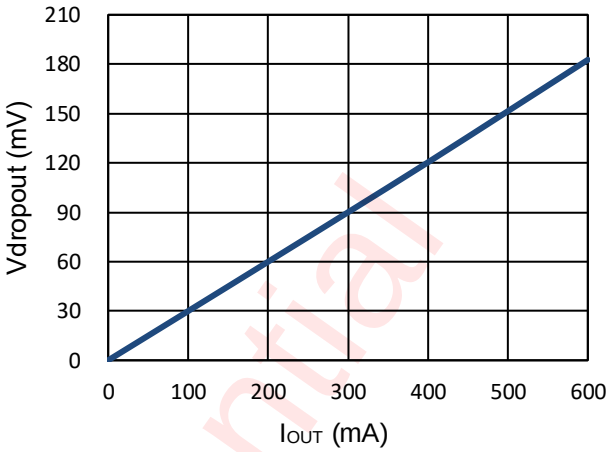
Output Voltage vs Temperature

LDO1/2



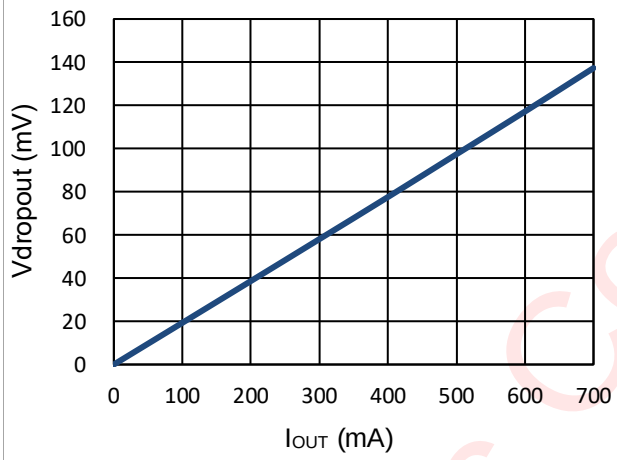
Dropout Voltage vs Output Current

LDO3/4/6



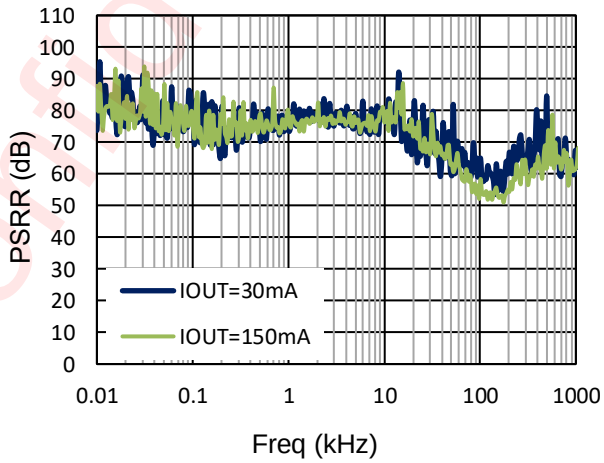
Dropout Voltage vs Output Current

LDO5/7



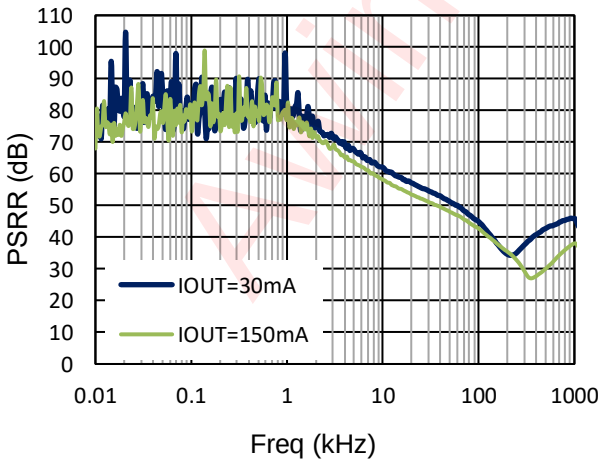
Dropout Voltage vs Output Current

LDO1/2



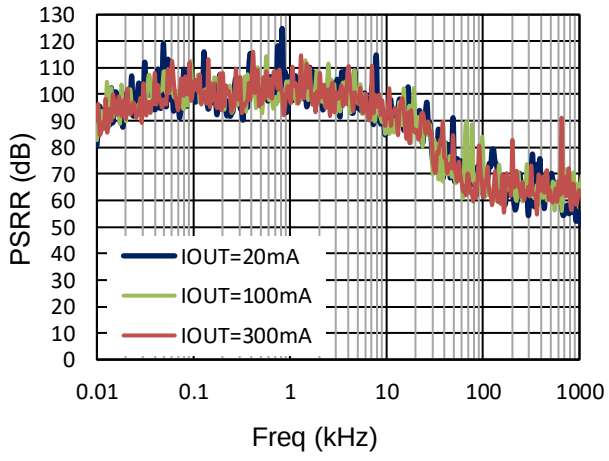
VSYS PSRR vs Frequency

LDO1/2



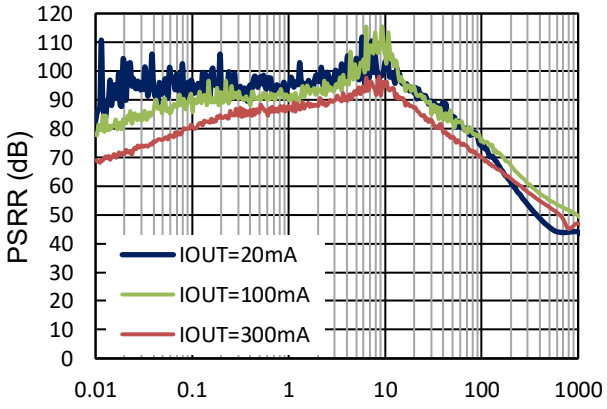
VINx PSRR vs Frequency

LDO3/4/6



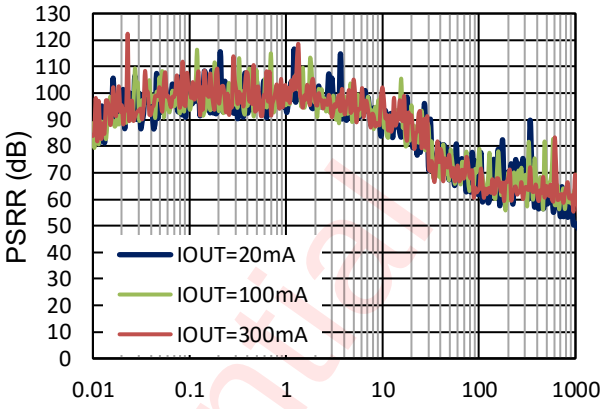
VSYS PSRR vs Frequency

LDO3/4/6



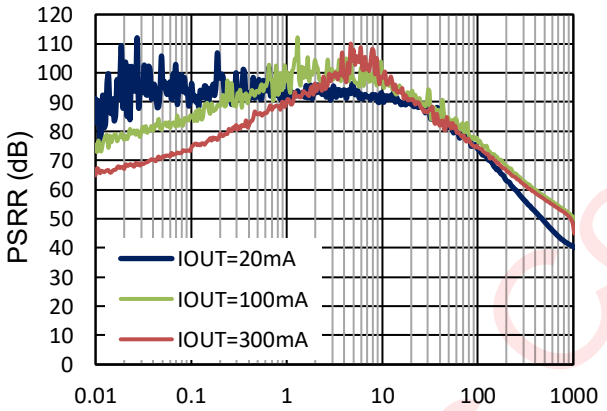
VINx PSRR vs Frequency

LDO5/7



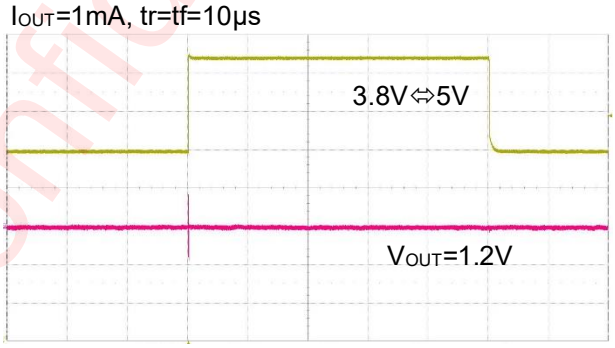
VSYS PSRR vs Frequency

LDO5/7



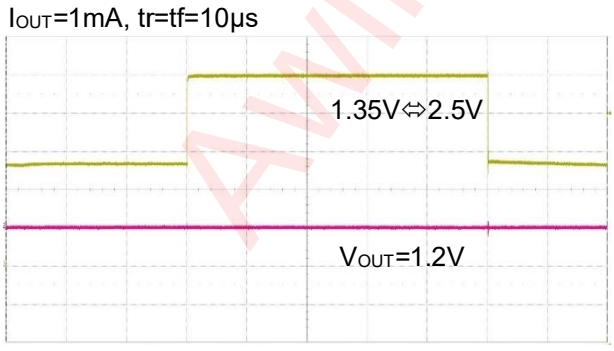
VINx PSRR vs Frequency

LDO1/2



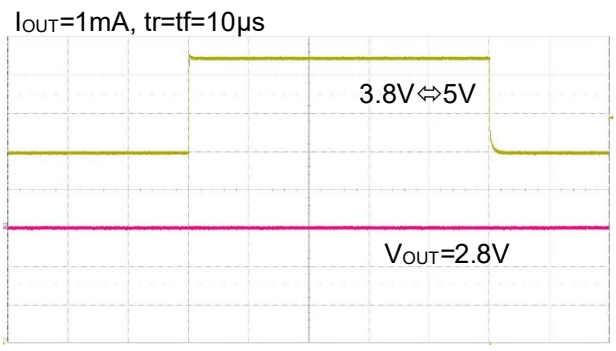
Line Transient of VSYS

LDO1/2



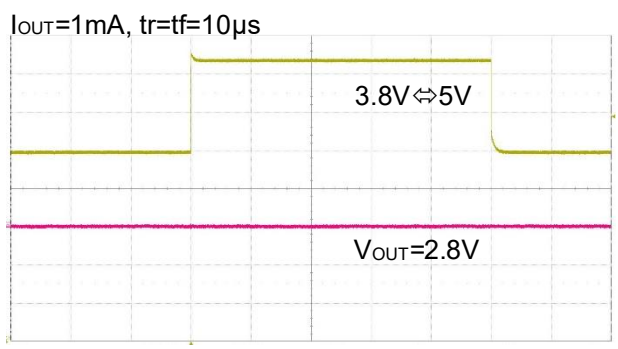
Line Transient of VINx

LDO3/4/6



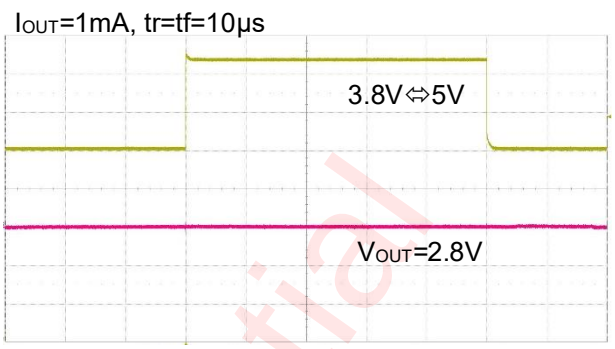
Line Transient of VSYS

LDO3/4/6



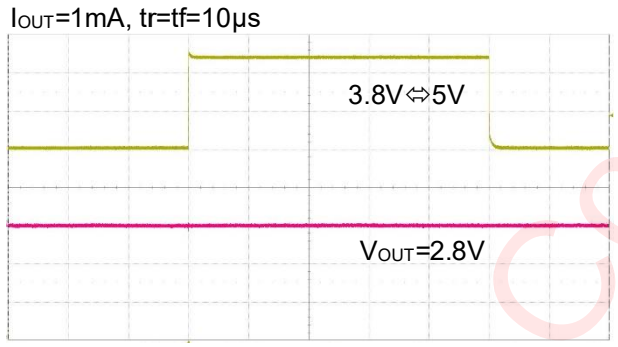
Line Transient of VINx

LDO5/7



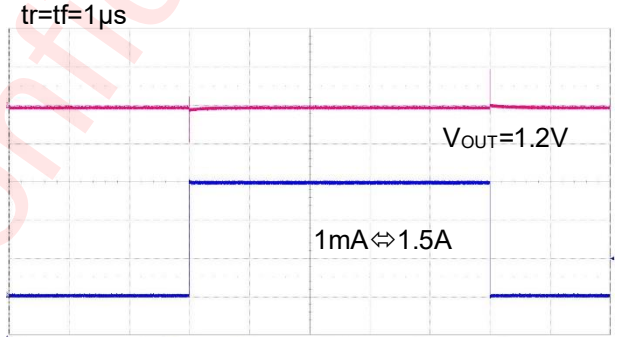
Line Transient of VSYS

LDO5/7



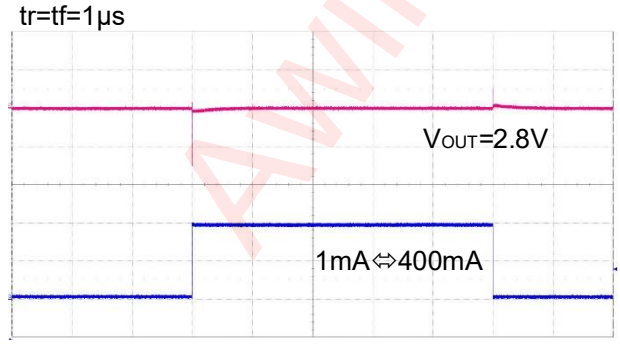
Line Transient of VINx

LDO1/2



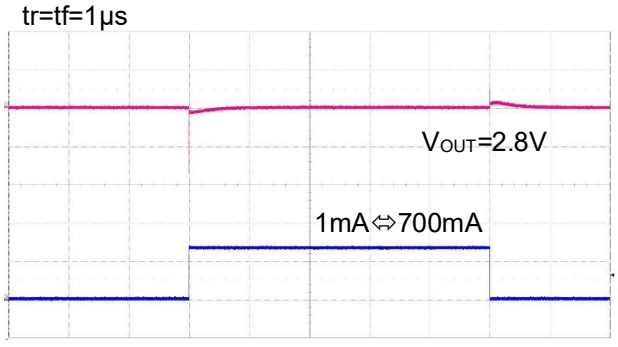
Load Transient Response

LDO3/4/6



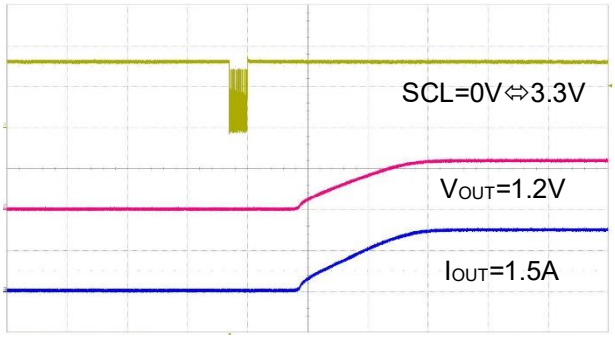
Load Transient Response

LDO5/7



Load Transient Response

LDO1/2

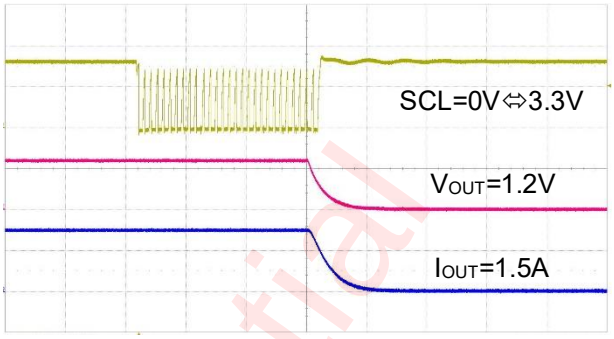


SCL: 2V/div VOUT: 1V/div IOUT: 1A/div

Time(100μs/div)

Turn On

LDO1/2

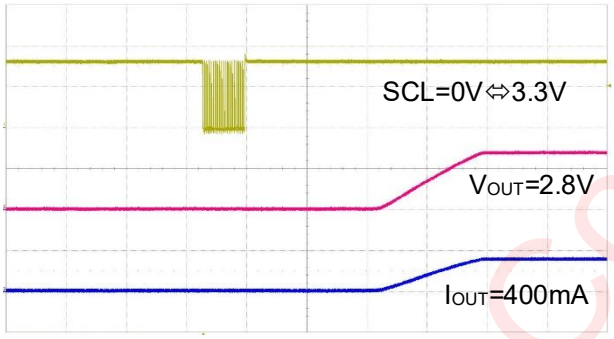


SCL: 2V/div VOUT: 1V/div IOUT: 1A/div

Time(10μs/div)

Turn Off

LDO3/4/6

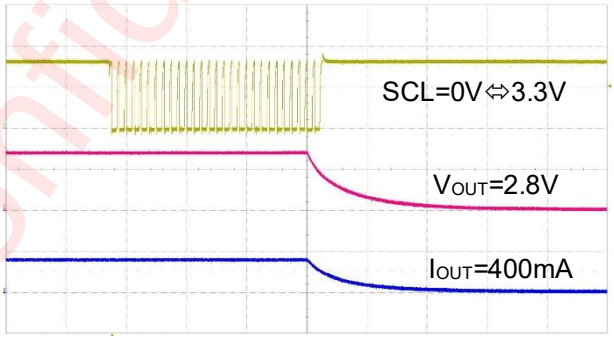


SCL: 2V/div VOUT: 2V/div IOUT: 500mA/div

Time(100μs/div)

Turn On

LDO3/4/6

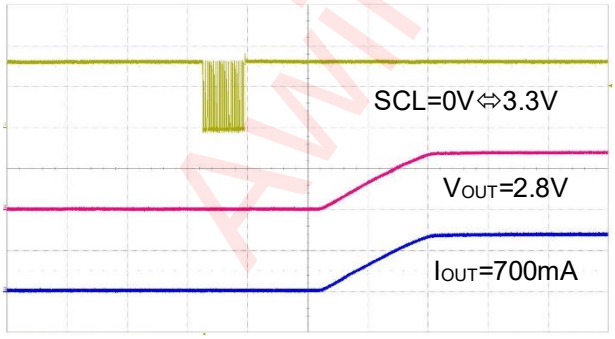


SCL: 2V/div VOUT: 2V/div IOUT: 500mA/div

Time(20μs/div)

Turn Off

LDO5/7

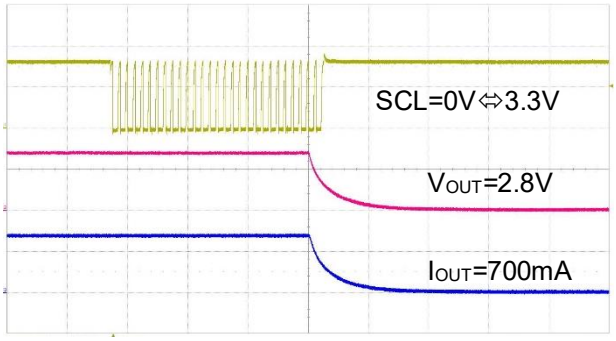


SCL: 2V/div VOUT: 2V/div IOUT: 500mA/div

Time(100μs/div)

Turn On

LDO5/7



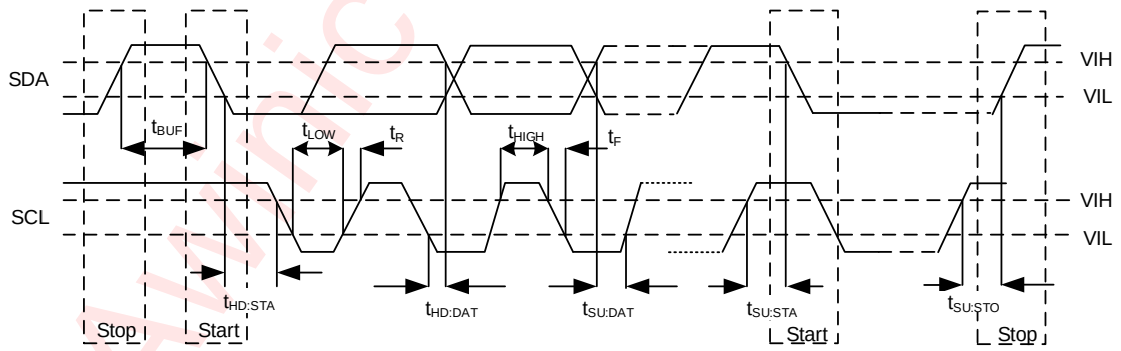
SCL: 2V/div VOUT: 2V/div IOUT: 500mA/div

Time(20μs/div)

Turn Off

I²C Interface Timing

PARAMETER		FAST MODE			FAST MODE PLUS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
F_{SCL}	Interface clock frequency	-		400	-		1000	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	0.26		-	μs
T_{LOW}	Low level width of SCL	1.3		-	0.5		-	μs
T_{HIGH}	High level width of SCL	0.6		-	0.26		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	0.26		-	μs
$T_{HD:DAT}$	Data hold time	0		-	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	0.05		-	μs
T_R	Rising time of SDA and SCL	-		0.3	-		0.12	μs
T_F	Falling time of SDA and SCL	-		0.3	-		0.12	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	0.26		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	0.5		-	μs



Detailed Functional Description

AW37007 is a PMIC with 7 LDO regulators, 2 of which are high current low dropout LDOs to power the digital circuits and 5 of which are high PSRR low noise LDOs to power the analog circuit. Each LDO output voltage and power up sequence can be programmed through the I²C interface.

Under-Voltage Lockout (UVLO)

When the RSTN pin is pulled high, the assigned UVLO interrupt bit and UVLO status bit will be set in two conditions:

- The voltage of VSYS is higher than the power-on reset (POR) voltage which is 2V but lower than VSYS UVLO rising threshold.
- The V_{INX} of the LDOx are below their UVLO rising threshold.

Meanwhile, the IRQ pin will be asserted high. The UVLO status bit remains set as long as the input voltage is below its UVLO rising threshold. The interrupt bit remains set to “1” unless the interrupt bit register is cleared manually.

When the voltage of VSYS or VINx fall below their UVLO falling threshold, one or more LDOs will be shut down, causing a UVLO interrupt. The UVLO status bit will not change until the input voltage rises above its UVLO rising threshold, and then one or more LDOs start up immediately.

As soon as the LDO is shut down, the suspend bits will be set. The LDOs will remain in the shutdown state for at least 20ms and will try to restart if VSYS or VINx have risen above their UVLO rising threshold. The suspend bits are cleared as soon as the LDO restarts. The LDOs will be disabled permanently after the 4th UVLO fault.

Thermal Management

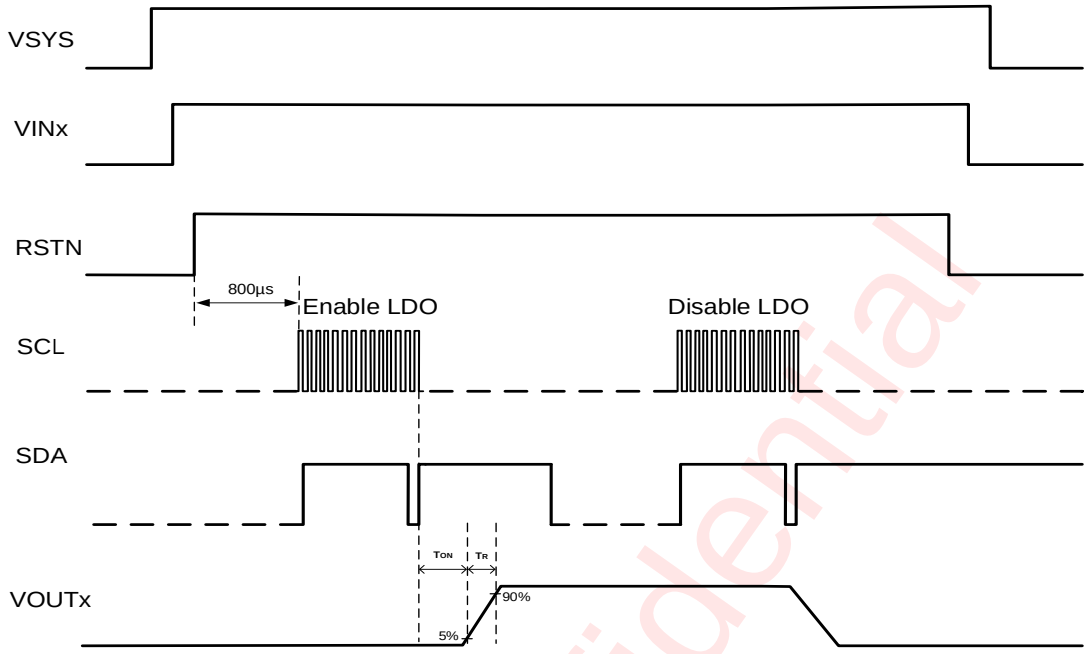
When the die temperature rises to a nominal 115°C, the thermal Warning status bit will be set to‘1’and remain set until the die temperature drops to a nominal 90°C. If the die temperature continues to rise to a nominal 155°C, a Thermal Shutdown event is activated, all the LDOs are disabled, the Thermal Shutdown interrupt bit is set but I²C communication remains. The Thermal Shutdown status bit is also set and will remain set as long as the device is above the Thermal Warning temperature. The chip suspend bit is set upon shutdown. The LDOs will be disabled permanently after the 4th Thermal Shutdown fault.

Enabling / Disabling

The LDOs can be enabled and disabled independently with the LDOx_EN bits in the ENABLE register. To enable the LDOs, RSTN pin should be high and SYS_EN bit= ‘1’, set the LDOx_EN bits to ‘1’. The LDOs have internal soft−start, which limits the inrush current to a lower value. The LDOs will ignore faults during the first 1.5ms at startup. After 1.5ms, if the LDO output fails to reach the UVP rising threshold, an UVP fault will be declared. To disable the LDOs, set the LDOx_EN bits to “0”. The active discharge feature is enabled by default, with which, an approximate 120Ω resister is connected between V_{OUT} and GND to discharge the output capacitors when the LDOx_EN bits are set to ‘0’.

To do a global shutdown of all LDOs, set RSTN pin low or write the SYS_EN bit to ‘0’.

The recommended power on sequence of AW37007 is to power on VSYS first, then power on input power VINx, then set RSTN to high level, and then enable LDOx. The I²C communication function is available after about 800μs when both VSYS POR and RSTN is ok. The corresponding power off sequence is to turn off LDOx first, then set RSTN to low level, then power off input power VINx, and finally power of VSYS.



Over-Current Protection (OCP)

The LDOs are protected from excessive load. The current limit level can be programmed through the I^2C interface. When an overload event occurs, the current is automatically limited to the programmed current limit. And once the current limit is detected, the associated OCP status bit is set, and if the LDO remains in current limit for more than 1ms which is default, the OCP interrupt bit will be set and the IRQ pin will be pulled high. Then the LDO will go into hiccup mode.

Under Voltage Protection (UVP)

If the output voltage falls approximately 128mV(10% for LDO1/2) below the target VOUT, the associated UVP status bit will be set. The UVP interrupt bit will be set of which the deglitch time is 125μs, and the IRQ pin will be pulled high. The LDO will then be disabled and the suspend bit is set. The interrupt bit will be cleared upon a read of the bit. The LDO will attempt a restart in 20ms and the suspend bit will be reset to '0' upon restart. And after the 4th UVP fault, the LDO shuts down permanently.

Reset

When the RSTN pin is pulled low, all registers will be cleared. Additionally, all fault counters will reset to 0. All registers can also be reset to their default values by writing "1011" to bit [7:4] in RESET register. At startup, RSTN must be kept low (below 0.36V) until VINx and VSYS are established.

LDO On/off Control and Sequencing

A. Individual LDO on/off control

Power-up and shut down of each regulator can be controlled by the register 0x03. LDOx_EN is an internal signal to enable the individual LDOs. If LDOx_SEQ set to '000', the LDOx can be controlled directly by the bit LDOx_EN specified in register 0x03.

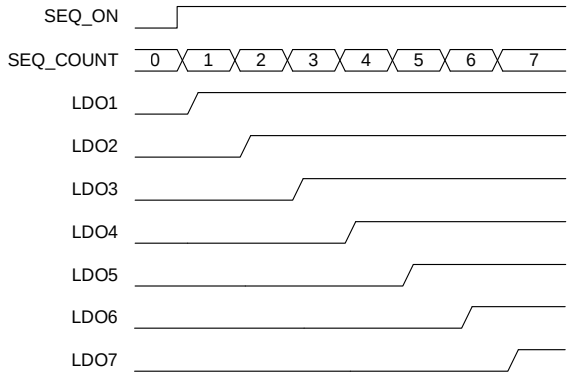
B. Automatic Power Up/Down Sequence Control

AW37007 has 7 SLOTs to which each regulator can be assigned.

SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7

They are started by SEQ_ON signal. When SEQ_ON is high, internal counter SEQ_COUNT starts increment from 0 (3'b000) to 7 (3'b111). When SEQ_ON is low, SEQ_COUNT decrements from 7 (3'b111) to 0 (3'b000). Regulators assigned to one of SLOTs starts power-up or power-down when SEQ_COUNT matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I²C, writing 2'b10 to SEQ_CONTROL will set SEQ_ON to '0', while writing 2'b01 to SEQ_CONTROL will set SEQ_ON to '1'.



Example of Power-up in the case of LDO1~LDO7

Example of Power-down in the case of LDO7~LDO1

Output Discharge Setting

There are the pull down resistors at each LDO output which will discharge the output capacitors quickly during power off, the discharge is enabled by default and can be disabled by set the individual bits in register 0x10.

4-Fault Shutdown

The LDO will be shut down permanently when the device detected 4 failures to prevent repetitive starting and faulting of an LDO or of the IC itself. The entire IC will be shut down permanently if it is a system fault.

Individual LDO Fault: the LDO will be latched off after the 4th individual LDO fault. Set the LDOx_EN bits to "1" to clear the latch-off and re-enable the LDOs.

Chip Fault: all the LDOs will be latched off after the 4th chip fault including VSYS UVLO and Thermal Shutdown with all the LDOx_EN bits cleared. In order to clear the latch-off, RSTN pin needs to be pulled low.

No Fault Shutdown

AW37007 provides a "No Fault Shutdown" feature, which prevents LDOs from shutting down during an OCP or UVP event. It is activated by setting the FLT_SD_B bit in RESET register to '1'. By setting FLT_SD_B to '1', it prevents the shutdown during an OCP or UVP event, but not during LDO VINx UVLO event. With FLT_SD_B=1, when LDO VINx UVLO, OCP or UVP event occurs, the interrupt and status bits will still indicate the fault has occurred, but the fault counter will not be incremented.

I²C Interface

AW37007 supports the I²C protocol. The maximum frequency supported by the I²C is 1MHz. The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C, 1kΩ is recommended for 1MHz I²C. The voltage from 1.8V to 3.3V is allowed for the I²C interface.

Additionally, the I²C device supports continuous reading and writing operations.

Device Address

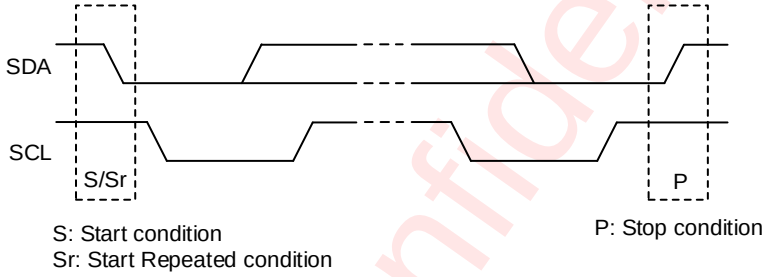
The I²C device address is 7-bit (A7~A1), followed by the R/W bit A0 (Read=1/Write=0). Set A0 to “0” for writing and “1” for reading.

A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	1	0	1	R/W

I²C Start/Stop

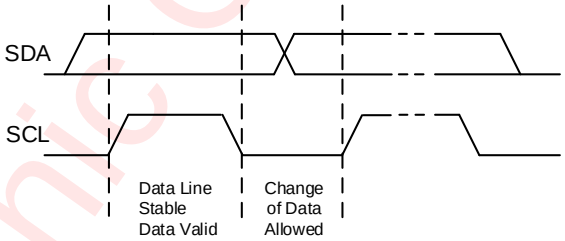
I²C Start: SDA changes from high level to low level when SCL is high level.

I²C Stop: SDA changes from low level to high level when SCL is high level.



Data Validation

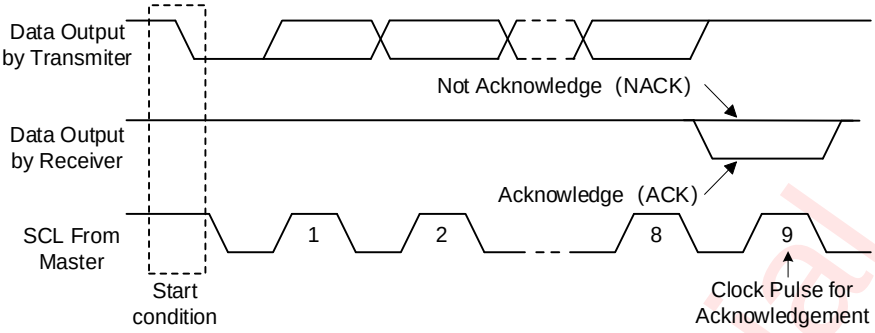
When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.



ACK (Acknowledgement)

ACK means the successful transition of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C STOP is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.



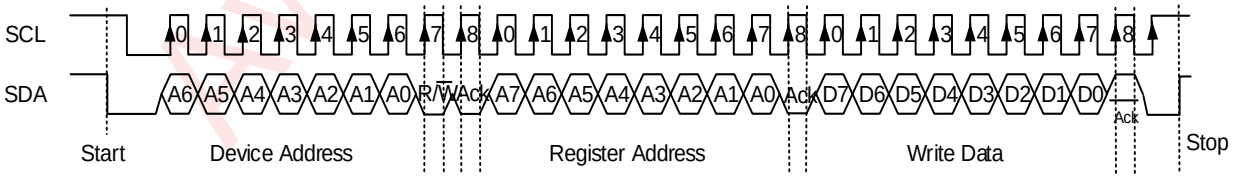
Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates Start condition. The "Start" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master sends data byte to be written to the addressed register.
g) Slave sends acknowledge signal.
h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g).
i) Master generates Stop condition to indicate write cycle end.



Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates Start condition.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master generates Stop condition followed with Start condition or Repeat Start condition.

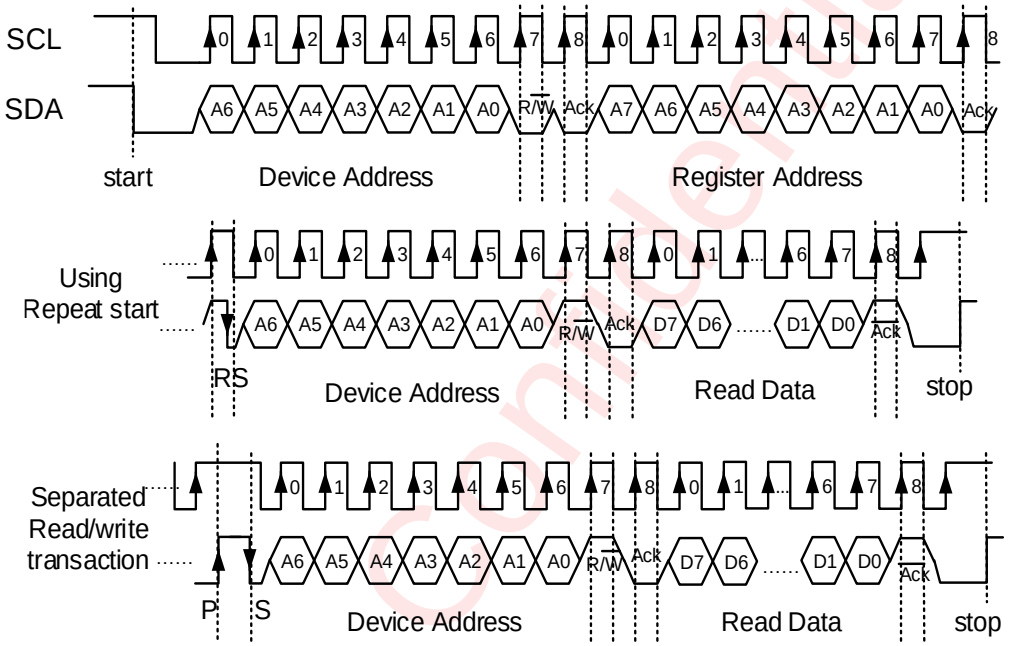
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates Stop condition, the read cycle ends.



Register Description

Addr	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Init
0x00	PRODUCT_ID	R	Product_ID								0x08
0x01	SILICON_REV_ID	R	Revision								0x01
0x02	IOUT	R/W	0	LDO7_ILIM	LDO6_ILIM	LDO5_ILIM	LDO4_ILIM	LDO3_ILIM	LDO2_ILIM	LDO1_ILIM	0x53
0x03	ENABLE	R/W	VSYS_EN	LDO7_EN	LDO6_EN	LDO5_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN	0x80
0x04	LDO1	R/W	LDO1_VOUT								0x58
0x05	LDO2	R/W	LDO2_VOUT								0x58
0x06	LDO3	R/W	LDO3_VOUT								0xA2
0x07	LDO4	R/W	LDO4_VOUT								0xA2
0x08	LDO5	R/W	LDO5_VOUT								0xA2
0x09	LDO6	R/W	LDO6_VOUT								0xA2
0x0A	LDO7	R/W	LDO7_VOUT								0xA2
0x0B	LDO12_SEQ	R/W	0		LDO2_SEQ			LDO1_SEQ			0x00
0x0C	LDO34_SEQ	R/W	0		LDO4_SEQ			LDO3_SEQ			0x00
0x0D	LDO56_SEQ	R/W	0		LDO6_SEQ			LDO5_SEQ			0x00
0x0E	LDO7_SEQ	R/W	0					LDO7_SEQ			0x00
0x0F	SEQUENCING	R/W	SEQ_SPEED		SEQ_CONTROL		SEQ_ON	SEQ_COUNT			0x00
0x10	DISCHARGE	R/W	0	LDO1_DIS	LDO2_DIS	LDO3_DIS	LDO4_DIS	LDO5_DIS	LDO6_DIS	LDO7_DIS	0x7F
0x11	RESET	R/W	SOFT_RESET				0	OCP_TIMER		FLT_SD_B	0x06
0x12	I2C_ADDR	R/W	IRQ_LEVEL	IRQ_OUT MODE_SEL	0				I2C_ADDR_SEL		0x81
0x13	RESERVED	R/W	0								0x00
0x14	RESERVED	R/W	0								0x00
0x15	INTERRUP1	R/WC	0	LDO7_UVP_INT	LDO6_UVP_INT	LDO5_UVP_INT	LDO4_UVP_INT	LDO3_UVP_INT	LDO2_UVP_INT	LDO1_UVP_INT	0x00
0x16	INTERRUP2	R/WC	0	LDO7_OCP_INT	LDO6_OCP_INT	LDO5_OCP_INT	LDO4_OCP_INT	LDO3_OCP_INT	LDO2_OCP_INT	LDO1_OCP_INT	0x00
0x17	INTERRUP3	R/WC	TSD_INT	TSD_WRN_INT	VSYS_UVLO_INT	LDO7_UVLO_INT	LDO6_UVLO_INT	LDO5_UVLO_INT	LDO34_UVLO_INT	LDO12_UVLO_INT	0x00
0x18	STATUS1	R	0	LDO7_UVP_STAT	LDO6_UVP_STAT	LDO5_UVP_STAT	LDO4_UVP_STAT	LDO3_UVP_STAT	LDO2_UVP_STAT	LDO1_UVP_STAT	0x00
0x19	STATUS2	R	0	LDO7_OCP_STAT	LDO6_OCP_STAT	LDO5_OCP_STAT	LDO4_OCP_STAT	LDO3_OCP_STAT	LDO2_OCP_STAT	LDO1_OCP_STAT	0x00
0x1A	STATUS3	R	TSD_STAT	TSD_WRN_STAT	VSYS_UVLO_STAT	LDO7_UVLO_STAT	LDO6_UVLO_STAT	LDO5_UVLO_STAT	LDO34_UVLO_STAT	LDO12_UVLO_STAT	0x00
0x1B	SUSD	R	CHIP_SUSD	LDO7_SUSD	LDO6_SUSD	LDO5_SUSD	LDO4_SUSD	LDO3_SUSD	LDO2_SUSD	LDO1_SUSD	0x00
0x1C	MINT1	R/W	0	LDO7_UVP_MSK	LDO6_UVP_MSK	LDO5_UVP_MSK	LDO4_UVP_MSK	LDO3_UVP_MSK	LDO2_UVP_MSK	LDO1_UVP_MSK	0x00
0x1D	MINT2	R/W	0	LDO7_OCP_MSK	LDO6_OCP_MSK	LDO5_OCP_MSK	LDO4_OCP_MSK	LDO3_OCP_MSK	LDO2_OCP_MSK	LDO1_OCP_MSK	0x00

0x1E	MINT3	R/W	TSD_MSK	TSD_WRN_MSK	VSYS_UVLO_MSK	LDO7_UVLO_MSK	LDO6_UVLO_MSK	LDO5_UVLO_MSK	LDO34_UVLO_MSK	LDO12_UVLO_MSK	0x00
0x22	CTRL_VSYS	R/W	0							EN_VSYS	0x01
0x23	CTRL_LDO1	R/W	0					ILIM_LDO1	DIS_LDO1	EN_LDO1	0x06
0x24	CTRL_LDO2	R/W	0					ILIM_LDO2	DIS_LDO2	EN_LDO2	0x06
0x25	CTRL_LDO3	R/W	0					ILIM_LDO3	DIS_LDO3	EN_LDO3	0x02
0x26	CTRL_LDO4	R/W	0					ILIM_LDO4	DIS_LDO4	EN_LDO4	0x02
0x27	CTRL_LDO5	R/W	0					ILIM_LDO5	DIS_LDO5	EN_LDO5	0x06
0x28	CTRL_LDO6	R/W	0					ILIM_LDO6	DIS_LDO6	EN_LDO6	0x02
0x29	CTRL_LDO7	R/W	0					ILIM_LDO7	DIS_LDO7	EN_LDO7	0x06

Register Detailed Description

0x00: PRODUCT_ID

Bit	Symbol	Type	Description	Init
7:0	Product ID	R	Identifies vendor and device type	0x08

0x01: SILICON_REV_ID

Bit	Symbol	Type	Description	Init
7:0	Revision	R	Identifies silicon revision	0x01

0x02: IOUT

Bit	Symbol	Type	Description		Init
7	Reserved	R/W	Not used		0x0
6	LDO7_ILIM	R/W	**Code**	**Current Limit (Min.)**	0x1
			0	650mA	
			1	950mA	
5	LDO6_ILIM	R/W	**Code**	**Current Limit (Min.)**	0x0
			0	450mA	
			1	650mA	
4	LDO5_ILIM	R/W	**Code**	**Current Limit (Min.)**	0x1
			0	650mA	
			1	950mA	
3	LDO4_ILIM	R/W	**Code**	**Current Limit (Min.)**	0x0
			0	450mA	
			1	650mA	
2	LDO3_ILIM	R/W	**Code**	**Current Limit (Min.)**	0x0

Bit	Symbol	Type	Description		Init
			0	450mA	
			1	650mA	
1	LDO2_ILIM	R/W	**Code**	**Current Limit (Min.)**	0x1
			0	1300mA	
			1	1800mA	
0	LDO1_ILIM	R/W	**Code**	**Current Limit (Min.)**	0x1
			0	1300mA	
			1	1800mA	

0x03: ENABLE

Bit	Symbol	Type	Description		Init
7	VSYS_EN	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit7=1 and RSTN is pulled high.		0x1
			Code	**Status**	
			0	Disabled	
			1	Enable	
6	LDO7_EN	R/W	Enable bit for LDO7. This bit only controls the state of LDO7 if LDO7_SEQ = 000.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enable	
5	LDO6_EN	R/W	Enable bit for LDO6. This bit only controls the state of LDO6 if LDO6_SEQ = 000.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enable	
4	LDO5_EN	R/W	Enable bit for LDO5. This bit only controls the state of LDO5 if LDO5_SEQ = 000.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enable	
3	LDO4_EN	R/W	Enable bit for LDO4. This bit only controls the state of LDO4 if LDO4_SEQ = 000.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enable	
2	LDO3_EN	R/W	Enable bit for LDO3. This bit only controls the state of LDO3 if LDO3_SEQ = 000.		0x0
			Code	**Status**	

Bit	Symbol	Type	Description		Init
			0	Disabled	
			1	Enable	
1	LDO2_EN	R/W	Enable bit for LDO2. This bit only controls the state of LDO2 if LDO2_SEQ = 000.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enable	
0	LDO1_EN	R/W	Enable bit for LDO1. This bit only controls the state of LDO1 if LDO1_SEQ = 000.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enable	

0x04: LDO1

Bit	Symbol	Type	Description	Init
7:0	LDO1_VOUT	R/W	Sets LDO1 regulation target voltage. Equation: VOUT=0.496V+d×8mV, where d is the decimal value of the register. 0x00: 0.496V 0x01: 0.504V 0x02: 0.512V … 0x57: 1.192V **0x58: 1.200V** 0x59: 1.208V … 0x7F: 1.512V	0x58

0x05: LDO2

Bit	Symbol	Type	Description	Init
7:0	LDO2_VOUT	R/W	Sets LDO2 regulation target voltage. Equation: VOUT=0.496V+d×8mV, where d is the decimal value of the register. 0x00: 0.496V 0x01: 0.504V 0x02: 0.512V … 0x57: 1.192V **0x58: 1.200V** 0x59: 1.208V … 0x7F: 1.512V	0x58

0x06: LDO3

Bit	Symbol	Type	Description	Init
7:0	LDO3_VOUT	R/W	Sets LDO3 regulation target voltage. Equation: VOUT=1.504V+d×8mV, where d is the decimal value of the register. 0x00: 1.504V 0x01: 1.512V 0x02: 1.520V … 0xA1: 2.792V **0xA2: 2.800V** 0xA3: 2.808V … 0xFF: 3.544V	0xA2

0x07: LDO4

Bit	Symbol	Type	Description	Init
7:0	LDO4_VOUT	R/W	Sets LDO4 regulation target voltage. Equation: VOUT=1.504V+d×8mV, where d is the decimal value of the register. 0x00: 1.504V 0x01: 1.512V 0x02: 1.520V … 0xA1: 2.792V **0xA2: 2.800V** 0xA3: 2.808V … 0xFF: 3.544V	0xA2

0x08: LDO5

Bit	Symbol	Type	Description	Init
7:0	LDO5_VOUT	R/W	Sets LDO5 regulation target voltage. Equation: VOUT=1.504V+d×8mV, where d is the decimal value of the register. 0x00: 1.504V 0x01: 1.512V 0x02: 1.520V … 0xA1: 2.792V **0xA2: 2.800V** 0xA3: 2.808V … 0xFF: 3.544V	0xA2

0x09: LDO6

Bit	Symbol	Type	Description	Init
7:0	LDO6_VOUT	R/W	Sets LDO6 regulation target voltage. Equation: VOUT=1.504V+d×8mV, where d is the decimal value of the register. 0x00: 1.504V 0x01: 1.512V 0x02: 1.520V … 0xA1: 2.792V **0xA2: 2.800V** 0xA3: 2.808V … 0xFF: 3.544V	0xA2

0x0A: LDO7

Bit	Symbol	Type	Description	Init
7:0	LDO7_VOUT	R/W	Sets LDO7 regulation target voltage. Equation: VOUT=1.504V+d×8mV, where d is the decimal value of the register. 0x00: 1.504V 0x01: 1.512V 0x02: 1.520V … 0xA1: 2.792V **0xA2: 2.800V** 0xA3: 2.808V … 0xFF: 3.544V	0xA2

0x0B: LDO12_SEQ

<table>
<tr><th>Bit</th><th>Symbol</th><th>Type</th><th colspan="2">Description</th><th>Init</th></tr>
<tr><td>7:6</td><td>Reserved</td><td>R/W</td><td colspan="2">Not used</td><td>0x0</td></tr>
<tr><td rowspan="9">5:3</td><td rowspan="9">LDO2_SEQ</td><td rowspan="9">R/W</td><td colspan="2">The LDO2 sequencing is selected by setting bits [5:3].</td><td rowspan="9">0x0</td></tr>
<tr><td>Code</td><td>Slot Selected</td></tr>
<tr><td>000</td><td>Controlled through I²C by setting the LDO2_EN bit.</td></tr>
<tr><td>001</td><td>Selects slot 1 for the LDO2 to be enabled at power up.</td></tr>
<tr><td>010</td><td>Selects slot 2 for the LDO2 to be enabled at power up.</td></tr>
<tr><td>011</td><td>Selects slot 3 for the LDO2 to be enabled at power up.</td></tr>
<tr><td>100</td><td>Selects slot 4 for the LDO2 to be enabled at power up.</td></tr>
<tr><td>101</td><td>Selects slot 5 for the LDO2 to be enabled at power up.</td></tr>
<tr><td>110</td><td>Selects slot 6 for the LDO2 to be enabled at power up.</td></tr>
</table>

Bit	Symbol	Type	Description		Init
			111	Selects slot 7 for the LDO2 to be enabled at power up.	
2:0	LDO1_SEQ	R/W	The LDO1 sequencing is selected by setting bits [2:0].		0x0
			Code	**Slot Selected**	
			000	Controlled through I²C by setting the LDO1_EN bit.	
			001	Selects slot 1 for the LDO1 to be enabled at power up.	
			010	Selects slot 2 for the LDO1 to be enabled at power up.	
			011	Selects slot 3 for the LDO1 to be enabled at power up.	
			100	Selects slot 4 for the LDO1 to be enabled at power up.	
			101	Selects slot 5 for the LDO1 to be enabled at power up.	
			110	Selects slot 6 for the LDO1 to be enabled at power up.	
			111	Selects slot 7 for the LDO1 to be enabled at power up.	

0x0C: LDO34_SEQ

Bit	Symbol	Type	Description		Init
7:6	Reserved	R/W	Not used		0x0
5:3	LDO4_SEQ	R/W	The LDO4 sequencing is selected by setting bits [5:3].		0x0
			Code	**Slot Selected**	
			000	Controlled through I²C by setting the LDO4_EN bit.	
			001	Selects slot 1 for the LDO4 to be enabled at power up.	
			010	Selects slot 2 for the LDO4 to be enabled at power up.	
			011	Selects slot 3 for the LDO4 to be enabled at power up.	
			100	Selects slot 4 for the LDO4 to be enabled at power up.	
			101	Selects slot 5 for the LDO4 to be enabled at power up.	
			110	Selects slot 6 for the LDO4 to be enabled at power up.	
			111	Selects slot 7 for the LDO4 to be enabled at power up.	
2:0	LDO3_SEQ	R/W	The LDO3 sequencing is selected by setting bits [2:0].		0x0
			Code	**Slot Selected**	
			000	Controlled through I²C by setting the LDO1_EN bit.	
			001	Selects slot 1 for the LDO3 to be enabled at power up.	
			010	Selects slot 2 for the LDO3 to be enabled at power up.	

Bit	Symbol	Type	Description		Init
			011	Selects slot 3 for the LDO3 to be enabled at power up.	
			100	Selects slot 4 for the LDO3 to be enabled at power up.	
			101	Selects slot 5 for the LDO3 to be enabled at power up.	
			110	Selects slot 6 for the LDO3 to be enabled at power up.	
			111	Selects slot 7 for the LDO3 to be enabled at power up.	

0x0D: LDO56_SEQ

Bit	Symbol	Type	Description		Init
7:6	Reserved	R/W	Not used		0x0
5:3	LDO6_SEQ	R/W	The LDO6 sequencing is selected by setting bits [5:3].		0x0
			Code	**Slot Selected**	
			000	Controlled through I^2C by setting the LDO6_EN bit.	
			001	Selects slot 1 for the LDO6 to be enabled at power up.	
			010	Selects slot 2 for the LDO6 to be enabled at power up.	
			011	Selects slot 3 for the LDO6 to be enabled at power up.	
			100	Selects slot 4 for the LDO6 to be enabled at power up.	
			101	Selects slot 5 for the LDO6 to be enabled at power up.	
			110	Selects slot 6 for the LDO6 to be enabled at power up.	
			111	Selects slot 7 for the LDO6 to be enabled at power up.	
2:0	LDO5_SEQ	R/W	The LDO5 sequencing is selected by setting bits [2:0].		0x0
			Code	**Slot Selected**	
			000	Controlled through I^2C by setting the LDO5_EN bit.	
			001	Selects slot 1 for the LDO5 to be enabled at power up.	
			010	Selects slot 2 for the LDO5 to be enabled at power up.	
			011	Selects slot 3 for the LDO5 to be enabled at power up.	
			100	Selects slot 4 for the LDO5 to be enabled at power up.	
			101	Selects slot 5 for the LDO5 to be enabled at power up.	
			110	Selects slot 6 for the LDO5 to be enabled at power up.	
			111	Selects slot 7 for the LDO5 to be enabled at power up.	

0x0E: LDO7_SEQ

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2:0	LDO7_SEQ	R/W	The LDO7 sequencing is selected by setting bits [2:0].		0x0
			Code	**Slot Selected**	
			000	Controlled through I²C by setting the LDO7_EN bit.	
			001	Selects slot 1 for the LDO7 to be enabled at power up.	
			010	Selects slot 2 for the LDO7 to be enabled at power up.	
			011	Selects slot 3 for the LDO7 to be enabled at power up.	
			100	Selects slot 4 for the LDO7 to be enabled at power up.	
			101	Selects slot 5 for the LDO7 to be enabled at power up.	
			110	Selects slot 6 for the LDO7 to be enabled at power up.	
			111	Selects slot 7 for the LDO7 to be enabled at power up.	

0x0F: SEQUENCING

Bit	Symbol	Type	Description		Init
7:6	SEQ_SPEED	R/W	**Code**	**Period per Slot**	0x0
			00	500μs	
			01	1.0ms	
			10	1.5ms	
			11	2.0ms	
5:3	SEQ_CONTROL	R/W	**Code**	**Initialize Power-Up or Power-Down**	0x0
			00	Default	
			01	Starts an LDO power-up sequence.	
			10	Starts an LDO shutdown sequence.	
			11	Bit configuration is ignored.	
3	SEQ_ON	R/W	**Code**	**The indicator of the sequencer status. Read only.**	0x0
			0	Shut down	
			1	Power up	
2:0	SEQ_COUNT	R/W	**Code**	**Present Slot**	0x0
			000	Indicates sequencing has completed or not started.	
			001	Indicates sequencing is in slot 1 during register read.	

Bit	Symbol	Type	Description		Init
			010	Indicates sequencing is in slot 2 during register read.	
			011	Indicates sequencing is in slot 3 during register read.	
			100	Indicates sequencing is in slot 4 during register read.	
			101	Indicates sequencing is in slot 5 during register read.	
			110	Indicates sequencing is in slot 6 during register read.	
			111	Indicates sequencing is in slot 7 during register read.	

0x10: DISCHARGE

Bit	Symbol	Type	Description		Init
7	Reserved	R/W	Not used		0x0
6	LDO1_DIS	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO1 Active Discharge feature is disable. Pull-down will not be activated when LDO1 is disabled by any event.	
			1	LDO1 Active Discharge feature is enabled. Pull-down will be activated when LDO1 is disabled by RSTN going low or LDO1_EN=0 or a sequenced shutdown or in a UVP event.	
5	LDO2_DIS	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO2 Active Discharge feature is disable. Pull-down will not be activated when LDO1 is disabled by any event.	
			1	LDO2 Active Discharge feature is enabled. Pull-down will be activated when LDO2 is disabled by RSTN going low or LDO2_EN=0 or a sequenced shutdown or in a UVP event.	
4	LDO3_DIS	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO3 Active Discharge feature is disable. Pull-down will not be activated when LDO3 is disabled by any event.	
			1	LDO3 Active Discharge feature is enabled. Pull-down will be activated when LDO3 is disabled by RSTN going low or LDO3_EN=0 or a sequenced shutdown or in a UVP event.	
3	LDO4_DIS	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO4 Active Discharge feature is disable. Pull-down will not be activated when LDO4 is disabled by any event.	
			1	LDO4 Active Discharge feature is enabled. Pull-down will be activated when LDO4 is disabled by RSTN going low or LDO4_EN=0 or a sequenced shutdown or in a UVP event.	
2	LDO5_DIS	R/W	**Code**	**Discharge Enabled/Disabled**	0x1

Bit	Symbol	Type	Description		Init
			0	LDO5 Active Discharge feature is disable. Pull-down will not be activated when LDO5 is disabled by any event.	
			1	LDO5 Active Discharge feature is enabled. Pull-down will be activated when LDO5 is disabled by RSTN going low or LDO5_EN=0 or a sequenced shutdown or in a UVP event.	
1	LDO6_DIS	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO6 Active Discharge feature is disable. Pull-down will not be activated when LDO6 is disabled by any event.	
			1	LDO6 Active Discharge feature is enabled. Pull-down will be activated when LDO6 is disabled by RSTN going low or LDO6_EN=0 or a sequenced shutdown or in a UVP event.	
0	LDO7_DIS	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO7 Active Discharge feature is disable. Pull-down will not be activated when LDO7 is disabled by any event.	
			1	LDO7 Active Discharge feature is enabled. Pull-down will be activated when LDO7 is disabled by RSTN going low or LDO7_EN=0 or a sequenced shutdown or in a UVP event.	

0x11: RESET

Bit	Symbol	Type	Description		Init
7:4	SOFT_RESET	R/W	**Code**	**Software Reset**	0x0
			1011	Writing a “1011” begins a soft reset of the device I^2C registers to their default values. This bit is cleared upon the execution of the reset function.	
				Any other value than “1011” will be ignored.	
3	Reserved	R/W	Not used		0x0
2:1	OCP_TIMER	R/W	Option bits to control the length of the deglitch timer for the current limit on all LDOs before a fault is triggered.		0x3
			Code	**Deglitch Timer**	
			00	125μs	
			01	250μs	
			10	500μs	
			11	1ms	
0	FLT_SD_B	R/W	**Code**	**Prevents shutdown when a fault occurs**	0x0
			0	LDO shuts down if a UVP or OCP event occurs or if the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event.	

Bit	Symbol	Type	Description		Init
			1	LDO does not shut down if a UVP or OCP event occurs. If the LDO's input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event, the associated LDO will shut down until the supply returns, but the fault will not be counted.	
			NOTE: If this bit function is desired, FLT_SD_B should be set to 1' prior to enabling any LDOs after a Power-On-Reset.		

0x12: I2C_ADDR

Bit	Symbol	Type	Description		Init
7	IRQ_LEVEL	R/W	**Code**	**IRQ Output Level Select**	0x1
			0	1.8V level when IRQ high	
			1	1.2V level when IRQ high	
6	IRQ_OUTMODE_SEL	R/W	**Code**	**IRQ Output Mode Select**	0x0
			0	Using PUSH-PULL for output	
			1	Using OPEN-DRAIN for output	
5:2	Reserved	R/W	Not used		0x0
1:0	I2C_ADDR_SEL	R/W	**Code**	**I²C Address Settings**	0x01
			00	0x20	
			01	0x35	
			10	0x61	
			11	0x72	

0x13, 0x14: RESERVED

Bit	Symbol	Type	Description	Init
7:0	Reserved	R/W	Not used	0x0

0x15: INTERRUP1

Bit	Symbol	Type	Description		Init
7	Reserved	R/WC	Not used		0x0
6	LDO7_UVP_INT	R/WC	**Code**	**LDO7 UVP Interrupt**	0x0
			0	Clear	
			1	Under−voltage event occurred on LDO7 output	
5	LDO6_UVP_INT	R/WC	**Code**	**LDO6 UVP Interrupt**	0x0
			0	Clear	
			1	Under−voltage event occurred on LDO6 output	
4	LDO5_UVP_INT	R/WC	**Code**	**LDO5 UVP Interrupt**	0x0
			0	Clear	

Bit	Symbol	Type	Description		Init
			1	Under−voltage event occurred on LDO5 output	
3	LDO4_UVP_INT	R/WC	**Code**	**LDO4 UVP Interrupt**	0x0
			0	Clear	
			1	Under−voltage event occurred on LDO4 output	
2	LDO3_UVP_INT	R/WC	**Code**	**LDO3 UVP Interrupt**	0x0
			0	Clear	
			1	Under−voltage event occurred on LDO3 output	
1	LDO2_UVP_INT	R/WC	**Code**	**LDO2 UVP Interrupt**	0x0
			0	Clear	
			1	Under−voltage event occurred on LDO2 output	
0	LDO1_UVP_INT	R/WC	**Code**	**LDO1 UVP Interrupt**	0x0
			0	Clear	
			1	Under−voltage event occurred on LDO1 output	

0x16: INTERRUP2

Bit	Symbol	Type	Description		Init
7	Reserved	R/WC	Not used		0x0
6	LDO7_OCP_INT	R/WC	**Code**	**LDO7 OCP Interrupt**	0x0
			0	Clear	
			1	OCP event occurred on LDO7 output	
5	LDO6_OCP_INT	R/WC	**Code**	**LDO6 OCP Interrupt**	0x0
			0	Clear	
			1	OCP event occurred on LDO6 output	
4	LDO5_OCP_INT	R/WC	**Code**	**LDO5 OCP Interrupt**	0x0
			0	Clear	
			1	OCP event occurred on LDO5 output	
3	LDO4_OCP_INT	R/WC	**Code**	**LDO4 OCP Interrupt**	0x0
			0	Clear	
			1	OCP event occurred on LDO4 output	
2	LDO3_OCP_INT	R/WC	**Code**	**LDO3 OCP Interrupt**	0x0
			0	Clear	
			1	OCP event occurred on LDO3 output	
1	LDO2_OCP_INT	R/WC	**Code**	**LDO2 OCP Interrupt**	0x0
			0	Clear	
			1	OCP event occurred on LDO2 output	
0	LDO1_OCP_INT	R/WC	**Code**	**LDO1 OCP Interrupt**	0x0

Bit	Symbol	Type	Description		Init
			0	Clear	
			1	OCP event occurred on LDO1 output	

0x17: INTERRUP3

Bit	Symbol	Type	Description		Init
7	TSD_INT	R/WC	**Code**	**Thermal Shutdown Interrupt**	0x0
			0	Clear	
			1	Thermal Shutdown event is detected or the temperature has fallen below the hysteresis level.	
6	TSD_WRN_INT	R/WC	**Code**	**Thermal Warning Interrupt**	0x0
			0	Clear	
			1	Thermal Shutdown Warning threshold was surpassed or the temperature has fallen below the hysteresis level.	
5	VSYS_UVLO_INT	R/WC	**Code**	**VSYS UVLO Interrupt**	0x0
			0	Clear	
			1	VSYS fell below the UVLO falling threshold or that VSYS have risen above the UVLO rising threshold after a UVLO fault.	
4	LDO7_UVLO_INT	R/WC	**Code**	**VIN7 UVLO Interrupt**	0x0
			0	Clear	
			1	V_{IN7} fell below the UVLO falling threshold while LDO7 was enabled or V_{IN7} has risen above the UVLO rising threshold after a UVLO fault.	
3	LDO6_UVLO_INT	R/WC	**Code**	**VIN6 UVLO Interrupt**	0x0
			0	Clear	
			1	V_{IN6} fell below the UVLO falling threshold while LDO6 was enabled or V_{IN6} has risen above the UVLO rising threshold after a UVLO fault.	
2	LDO5_UVLO_INT	R/WC	**Code**	**VIN5 UVLO Interrupt**	0x0
			0	Clear	
			1	V_{IN5} fell below the UVLO falling threshold while LDO5 was enabled or V_{IN5} has risen above the UVLO rising threshold after a UVLO fault.	
1	LDO34_UVLO_INT	R/WC	**Code**	**VIN34 UVLO Interrupt**	0x0
			0	Clear	
			1	V_{IN34} fell below the UVLO falling threshold while LDO34 was enabled or V_{IN34} has risen above the UVLO rising threshold after a UVLO fault.	
0	LDO12_UVLO_INT	R/WC	**Code**	**VIN12 UVLO Interrupt**	0x0
			0	Clear	
			1	V_{IN12} fell below the UVLO falling threshold while LDO12 was enabled or V_{IN12} has risen	

Bit	Symbol	Type	Description		Init
				above the UVLO rising threshold after a UVLO fault.	
For bit0~bit5, reading the associated status bit provides present state of the input voltage.					

0x18: STATUS1

Bit	Symbol	Type	Description		Init
7	Reserved	R	Not used		0x0
6	LDO7_UVP_STAT	R	**Code**	**LDO7 UVP Status**	0x0
			0	Normal operation	
			1	An under-voltage condition exists on LDO7 output.	
5	LDO6_UVP_STAT	R	**Code**	**LDO6 UVP Status**	0x0
			0	Normal operation	
			1	An under-voltage condition exists on LDO6 output.	
4	LDO5_UVP_STAT	R	**Code**	**LDO5 UVP Status**	0x0
			0	Normal operation	
			1	An under-voltage condition exists on LDO5 output.	
3	LDO4_UVP_STAT	R	**Code**	**LDO4 UVP Status**	0x0
			0	Normal operation	
			1	An under-voltage condition exists on LDO4 output.	
2	LDO3_UVP_STAT	R	**Code**	**LDO3 UVP Status**	0x0
			0	Normal operation	
			1	An under-voltage condition exists on LDO3 output.	
1	LDO2_UVP_STAT	R	**Code**	**LDO2 UVP Status**	0x0
			0	Normal operation	
			1	An under-voltage condition exists on LDO2 output.	
0	LDO1_UVP_STAT	R	**Code**	**LDO1 UVP Status**	0x0
			0	Normal operation	
			1	An under-voltage condition exists on LDO1 output.	

0x19: STATUS2

Bit	Symbol	Type	Description		Init
7	Reserved	R	Not used		0x0
6	LDO7_OCP_STAT	R	**Code**	**LDO7 OCP Status**	0x0
			0	Normal operation	
			1	An over-current condition exists on LDO7 output.	

Bit	Symbol	Type	Description		Init
5	LDO6_OCP_STAT	R	**Code**	**LDO6 OCP Status**	0x0
			0	Normal operation	
			1	An over-current condition exists on LDO6 output.	
4	LDO5_OCP_STAT	R	**Code**	**LDO5 OCP Status**	0x0
			0	Normal operation	
			1	An over-current condition exists on LDO5 output.	
3	LDO4_OCP_STAT	R	**Code**	**LDO4 OCP Status**	0x0
			0	Normal operation	
			1	An over-current condition exists on LDO4 output.	
2	LDO3_OCP_STAT	R	**Code**	**LDO3 OCP Status**	0x0
			0	Normal operation	
			1	An over-current condition exists on LDO3 output.	
1	LDO2_OCP_STAT	R	**Code**	**LDO2 OCP Status**	0x0
			0	Normal operation	
			1	An over-current condition exists on LDO2 output.	
0	LDO1_OCP_STAT	R	**Code**	**LDO1 OCP Status**	0x0
			0	Normal operation	
			1	An over-current condition exists on LDO1 output.	

0x1A: STATUS3

Bit	Symbol	Type	Description		Init
7	TSD_STAT	R	**Code**	**Thermal Shutdown Status**	0x0
			0	Normal operation	
			1	Device is in Thermal Shutdown.	
6	TSD_WRN_STAT	R	**Code**	**Thermal Warning Status**	0x0
			0	Normal operation	
			1	The temperature is above the Thermal Warning level and shutdown is impending.	
5	VSYS_UVLO_STAT	R	**Code**	**VSYS UVLO Status**	0x0
			0	Normal operation	
			1	VSYS is below the UVLO threshold.	

Bit	Symbol	Type	Description		Init
4	LDO7_UVLO_STAT	R	**Code**	**VIN7 UVLO Status**	0x0
			0	Normal operation	
			1	V_{IN7} is below the UVLO threshold while LDO7 is enabled.	
3	LDO6_UVLO_STAT	R	**Code**	**VIN6 UVLO Status**	0x0
			0	Normal operation	
			1	V_{IN6} is below the UVLO threshold while LDO6 is enabled.	
2	LDO5_UVLO_STAT	R	**Code**	**VIN5 UVLO Status**	0x0
			0	Normal operation	
			1	V_{IN5} is below the UVLO threshold while LDO5 is enabled.	
1	LDO34_UVLO_STAT	R	**Code**	**VIN34 UVLO Status**	0x0
			0	Normal operation	
			1	V_{IN34} is below the UVLO threshold while LDO3q4 is enabled.	
0	LDO12_UVLO_STAT	R	**Code**	**VIN12 UVLO Status**	0x0
			0	Normal operation	
			1	V_{IN12} is below the UVLO threshold while LDO12 is enabled.	

0x1B: SUSD

Bit	Symbol	Type	Description		Init
7	CHIP_SUSD	R	**Code**	**Chip Suspension**	0x0
			0	Chip in normal state	
			1	The entire chip has been suspended due to a global fault condition.	
6	LDO7_SUSD	R	**Code**	**LDO7 Output Suspended**	0x0
			0	LDO7 in normal state	
			1	LDO7 has been suspended due to a fault condition.	
5	LDO6_SUSD	R	**Code**	**LDO6 Output Suspended**	0x0
			0	LDO6 in normal state	
			1	LDO6 has been suspended due to a fault condition.	
4	LDO5_SUSD	R	**Code**	**LDO5 Output Suspended**	0x0

Bit	Symbol	Type	Description		Init
			0	LDO5 in normal state	
			1	LDO5 has been suspended due to a fault condition.	
3	LDO4_SUSD	R	**Code**	**LDO4 Output Suspended**	0x0
			0	LDO4 in normal state	
			1	LDO4 has been suspended due to a fault condition.	
2	LDO3_SUSD	R	**Code**	**LDO3 Output Suspended**	0x0
			0	LDO3 in normal state	
			1	LDO3 has been suspended due to a fault condition.	
1	LDO2_SUSD	R	**Code**	**LDO2 Output Suspended**	0x0
			0	LDO2 in normal state	
			1	LDO2 has been suspended due to a fault condition.	
0	LDO1_SUSD	R	**Code**	**LDO1 Output Suspended**	0x0
			0	LDO1 in normal state	
			1	LDO1 has been suspended due to a fault condition.	

0x1C: MINT1

Bit	Symbol	Type	Description		Init
7	Reserved	R/W	Not used		0x0
6	LDO7_UVP_MSK	R/W	**Code**	**LDO7 UVP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO7 under−voltage interrupt occurs	
5	LDO6_UVP_MSK	R/W	**Code**	**LDO6 UVP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO6 under−voltage interrupt occurs	
4	LDO5_UVP_MSK	R/W	**Code**	**LDO5 UVP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO5 under−voltage interrupt occurs	
3	LDO4_UVP_	R/W	**Code**	**LDO4 UVP MASK**	0x0

Bit	Symbol	Type	Description		Init
	MSK		0	No masking of interrupt	
			1	IRQ pin will not change states when LDO4 under−voltage interrupt occurs	
2	LDO3_UVP_ MSK	R/W	**Code**	**LDO3 UVP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO3 under−voltage interrupt occurs	
1	LDO2_UVP_ MSK	R/W	**Code**	**LDO2 UVP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO2 under−voltage interrupt occurs	
0	LDO1_UVP_ MSK	R/W	**Code**	**LDO1 UVP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO1 under−voltage interrupt occurs	

0x1D: MINT2

Bit	Symbol	Type	Description		Init
7	Reserved	R/W	Not used		0x0
6	LDO7_OCP_ MSK	R/W	**Code**	**LDO7 OCP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO7 UVP interrupt occurs	
5	LDO6_OCP_ MSK	R/W	**Code**	**LDO6 OCP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO6 UVP interrupt occurs	
4	LDO5_OCP_ MSK	R/W	**Code**	**LDO5 OCP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO5 UVP interrupt occurs	
3	LDO4_OCP_ MSK	R/W	**Code**	**LDO4 OCP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO4 UVP interrupt occurs	
2	LDO3_OCP_	R/W	**Code**	**LDO3 OCP MASK**	0x0

Bit	Symbol	Type	Description		Init
	MSK		0	No masking of interrupt	
			1	IRQ pin will not change states when LDO3 UVP interrupt occurs	
1	LDO2_OCP_MSK	R/W	**Code**	**LDO2 OCP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO2 UVP interrupt occurs	
0	LDO1_OCP_MSK	R/W	**Code**	**LDO1 OCP MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when LDO1 UVP interrupt occurs	

0x1E: MINT3

Bit	Symbol	Type	Description		Init
7	TSD_MSK	R/W	**Code**	**Thermal Shutdown MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when a Thermal Shutdown interrupt occurs.	
6	TSD_WRN_MSK	R/W	**Code**	**Thermal Warning MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when a Thermal Warning interrupt occurs.	
5	VSYS_UVLO_MSK	R/W	**Code**	**VSYS UVLO MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when VSYS input power under−voltage interrupt occurs	
4	LDO7_UVLO_MSK	R/W	**Code**	**VIN7 UVLO MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when V_{IN7} input power under−voltage interrupt occurs	
3	LDO6_UVLO_MSK	R/W	**Code**	**VIN6 UVLO MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when V_{IN6} input power under−voltage interrupt occurs	
2	LDO5_UVLO_MSK	R/W	**Code**	**VIN5 UVLO MASK**	0x0
			0	No masking of interrupt	

Bit	Symbol	Type	Description		Init
			1	IRQ pin will not change states when V_{IN5} input power under−voltage interrupt occurs	
1	LDO34_UVLO_MSK	R/W	**Code**	**VIN34 UVLO MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when V_{IN34} input power under−voltage interrupt occurs	
0	LDO12_UVLO_MSK	R/W	**Code**	**VIN12 UVLO MASK**	0x0
			0	No masking of interrupt	
			1	IRQ pin will not change states when V_{IN12} input power under−voltage interrupt occurs	

0x22: CTRL_VSYS

Bit	Symbol	Type	Description		Init
7:1	Reserved	R/W	Not used		0x0
0	EN_VSYS	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x1
			Code	**Status**	
			0	Disabled	
			1	Enabled	

0x23: CTRL_LDO1

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2	ILIM_LDO1	R/W	**Code**	**Current Limit**	0x1
			0	1300mA	
			1	1800mA	
1	DIS_LDO1	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO Active Discharge feature is disable. Pull-down will not be activated when LDO is disabled by any event.	
			1	LDO Active Discharge feature is enabled. Pull-down will be activated when LDO is disabled by RESET_B going low or LDO_EN = 0 or a sequenced shutdown or in a UVP event.	
0	EN_LDO1	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x0
			Code	**Status**	
			0	Disabled	

Bit	Symbol	Type	Description		Init
			1	Enabled	

0x24: CTRL_LDO2

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2	ILIM_LDO2	R/W	**Code**	**Current Limit**	0x1
			0	1300mA	
			1	1800mA	
1	DIS_LDO2	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO Active Discharge feature is disable. Pull-down will not be activated when LDO is disabled by any event.	
			1	LDO Active Discharge feature is enabled. Pull-down will be activated when LDO is disabled by RESET_B going low or LDO_EN = 0 or a sequenced shutdown or in a UVP event.	
0	EN_LDO2	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enabled	

0x25: CTRL_LDO3

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2	ILIM_LDO3	R/W	**Code**	**Current Limit**	0x0
			0	450mA	
			1	650mA	
1	DIS_LDO3	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO Active Discharge feature is disable. Pull-down will not be activated when LDO is disabled by any event.	
			1	LDO Active Discharge feature is enabled. Pull-down will be activated when LDO is disabled by RESET_B going low or LDO_EN = 0 or a sequenced shutdown or in a UVP event.	
0	EN_LDO3	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x0
			Code	**Status**	
			0	Disabled	

Bit	Symbol	Type	Description		Init
			1	Enabled	

0x26: CTRL_LDO4

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2	ILIM_LDO4	R/W	**Code**	**Current Limit**	0x0
			0	450mA	
			1	650mA	
1	DIS_LDO4	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO Active Discharge feature is disable. Pull-down will not be activated when LDO is disabled by any event.	
			1	LDO Active Discharge feature is enabled. Pull-down will be activated when LDO is disabled by RESET_B going low or LDO_EN = 0 or a sequenced shutdown or in a UVP event.	
0	EN_LDO4	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enabled	

0x27: CTRL_LDO5

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2	ILIM_LDO5	R/W	**Code**	**Current Limit**	0x1
			0	650mA	
			1	950mA	
1	DIS_LDO5	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO Active Discharge feature is disable. Pull-down will not be activated when LDO is disabled by any event.	
			1	LDO Active Discharge feature is enabled. Pull-down will be activated when LDO is disabled by RESET_B going low or LDO_EN = 0 or a sequenced shutdown or in a UVP event.	
0	EN_LDO5	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x0
			Code	**Status**	
			0	Disabled	

Bit	Symbol	Type	Description		Init
			1	Enabled	

0x28: CTRL_LDO6

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2	ILIM_LDO6	R/W	**Code**	**Current Limit**	0x0
			0	450mA	
			1	650mA	
1	DIS_LDO6	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO Active Discharge feature is disable. Pull-down will not be activated when LDO is disabled by any event.	
			1	LDO Active Discharge feature is enabled. Pull-down will be activated when LDO is disabled by RESET_B going low or LDO_EN = 0 or a sequenced shutdown or in a UVP event.	
0	EN_LDO6	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x0
			Code	**Status**	
			0	Disabled	
			1	Enabled	

0x29: CTRL_LDO7

Bit	Symbol	Type	Description		Init
7:3	Reserved	R/W	Not used		0x0
2	ILIM_LDO7	R/W	**Code**	**Current Limit**	0x1
			0	650mA	
			1	950mA	
1	DIS_LDO7	R/W	**Code**	**Discharge Enabled/Disabled**	0x1
			0	LDO Active Discharge feature is disable. Pull-down will not be activated when LDO is disabled by any event.	
			1	LDO Active Discharge feature is enabled. Pull-down will be activated when LDO is disabled by RESET_B going low or LDO_EN = 0 or a sequenced shutdown or in a UVP event.	
0	EN_LDO7	R/W	Enable bit for system. The system bias will be getting ready for enabling individual LDO if bit0 = 1 and RESET_N is pulled high.		0x0
			Code	**Status**	
			0	Disabled	

Bit	Symbol	Type	Description		Init
			1	Enabled	

Application Information

Capacitors Selection

IN pin: Input Capacitor

AW37007 advises to use a X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit. The rated voltage of C_{IN} should be higher than input voltage. The input capacitance for VIN12 should be 4.7μF or greater, , the input capacitance for VIN34/VIN5/VIN6/VIN7 should be 2.2μF or greater, the input capacitance for VSYS should be 1μF or greater, and C_{VBIAS} should be 0.1μF.

OUT pin: Output Capacitor

AW37007 advises to use X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit. The rated voltage of C_{OUT} should be higher than output voltage. The recommended output capacitor is 4.7uF for C_{LDO1-2} and 2.2uF for C_{LDO3-7}.

For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design, the minimum effective capacitance for C_{LDO1-2} is 2μF, and the minimum effective capacitance for C_{LDO3-7} is 0.7μF.

SCL, SDA, and IRQ resistor

The recommended resistance for SCL and SDA is 2.2kΩ when a voltage of 1.2V is applied to the I^2C. When I^2C is at 1.8V, the recommended value range is from 2.2kΩ to 4.7kΩ. The recommended values are applicable across the frequency range from 100kHz to 1MHz. The IRQ requires a pull-up resistor (100kΩ typically) in open-drain mode but not in push-pull mode.

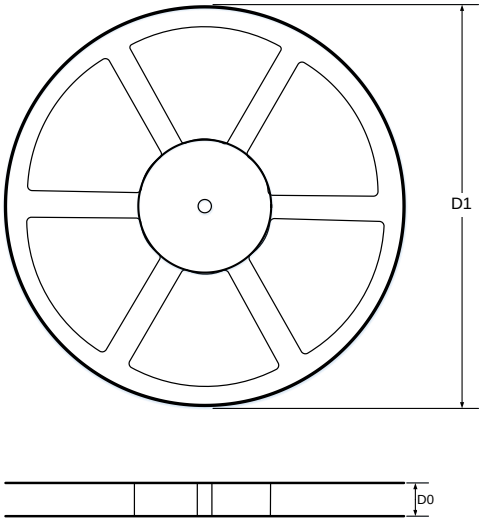
PCB Layout Consideration

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37007 should be obeyed:

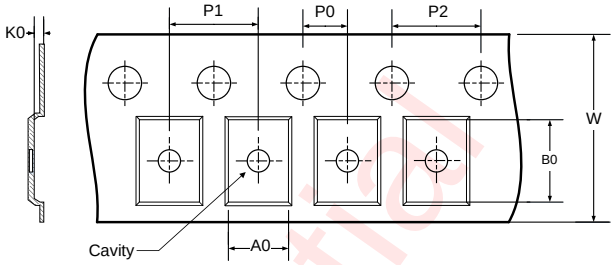
1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information

REEL DIMENSIONS

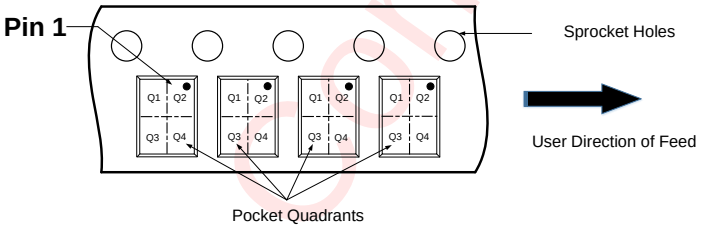


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



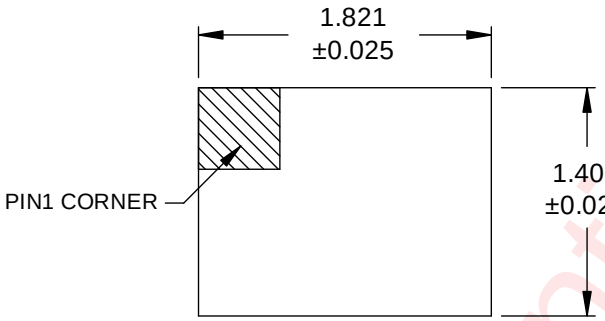
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

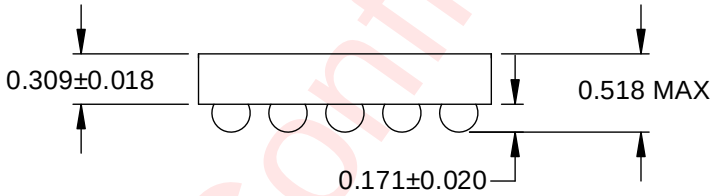
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.0	9.0	1.53	1.95	0.65	2.00	4.00	4.00	8.00	Q2

All dimensions are nominal

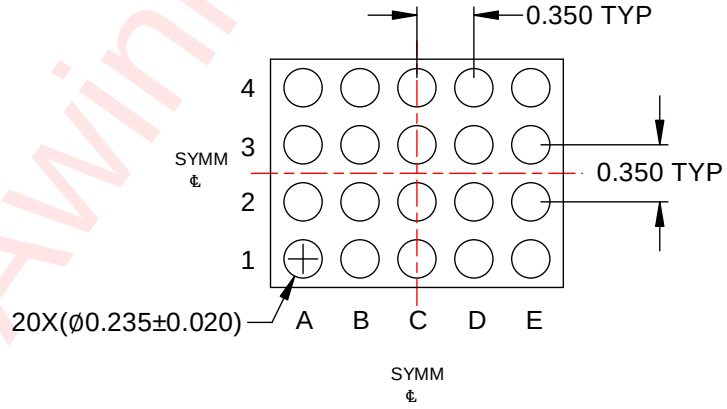
Package Description



Top View



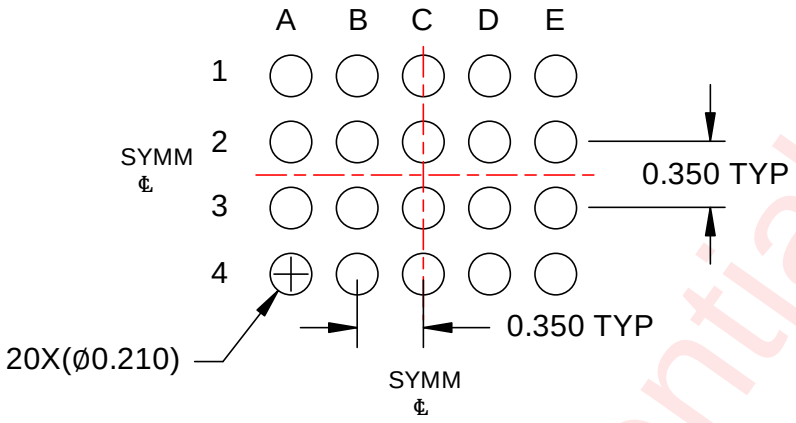
Side View

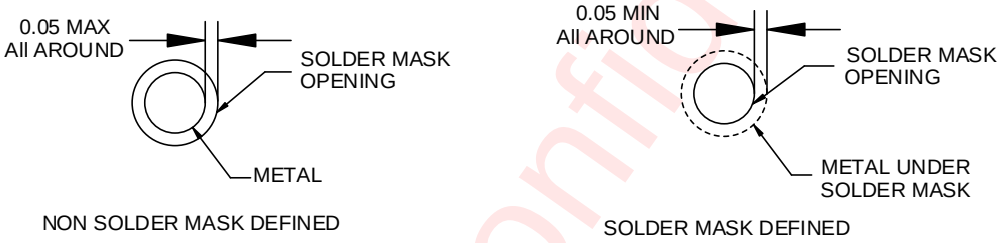


Bottom View

Unit:mm

Land Pattern Data





Unit: mm

Revision History

Version	Date	Change Record
V1.0	Aug. 2025	Officially released

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.