

Force and Capacitive Touch Controller

Features

- 4/5-channel force or 10/12-channel capacitive sensor
- Self/Mutual capacitive sensing techniques
- Force PGA up to 125, 21-bit ADC
- Capacitance resolution down to 1aF
- Force offset compensation up to 1V
- Capacitance offset compensation up to 220pF
- Auto-Offset-Tuning (AOT)
- Adaptive temperature compensation
- Multi-threshold judgment
- Effective waterproof
- Independent configurations per channel
- Built-in gesture/event recognition:
- 1.2V/1.8V 400kHz I²C interface
 - Default address: 0x12
 - Address configurable via pin CS2
- Embedded 8KB DATARAM and 12KB CODERAM
- Ultra-low power consumption^(NOTE1)
 - Active mode: 23.5μA
 - Doze mode: 10.7μA
 - Sleep mode: 8.9μA
 - DeepSleep mode: 6.1μA
- 1.65V~3.6V power supply
- Package
 - AW93804QNR: QFN 2×2-14L
 - AW93805QNR: QFN 3×3-24L
 - AWS93805PLR: FOPLP 1.729×1.538-20B

NOTE1: Power test configuration of each mode is shown in Table Electrical Characteristics.

Applications

- Wearable devices
- Mobile phones
- Tablets
- Notebooks

General Description

AW93804QNR, AW93805QNR and AWS93805PLR are force/capacitive sensing which supports up to 4/5-channel force or 10/12-channel capacitive detection and mainly used for wear detection, touch key, linear slider, wheel slider, etc.

Advanced force technology is adopted in AW9380X. With a high-resolution ADC and advanced digital signal processing (DSP) algorithm.

Advanced self/mutual capacitance technology is adopted in AW9380X. With a high-resolution ADC and advanced digital signal processing (DSP) algorithm, the minimal capacitance that can be detected is as low as 1aF in typical application.

AW9380X contains the I²C serial communication bus. Through I²C, Host can configure the chip to work. Upon event detection, the interrupt pin outputs asserts, enabling Host to receive the event information such as distance.

A built-in ultra-low power MCU realizes AFE sampling control, signal filtering, RF noise suppression, adaptive temperature compensation, baseline tracking, touch/wearing status determination, etc.

With the advanced DSP algorithm, AW9380X is able to track gradual environmental variations (such as temperature, humidity, etc.).

AW9380X can recognize various gestures, such as single/double/triple click, short/long press, linear slide and wheel slide with the high-resolution force/capacitive sensing. The chip integrates force/capacitive technology and dedicated algorithm, which greatly improve the waterproof performance for touch key.

Typical Application Circuit

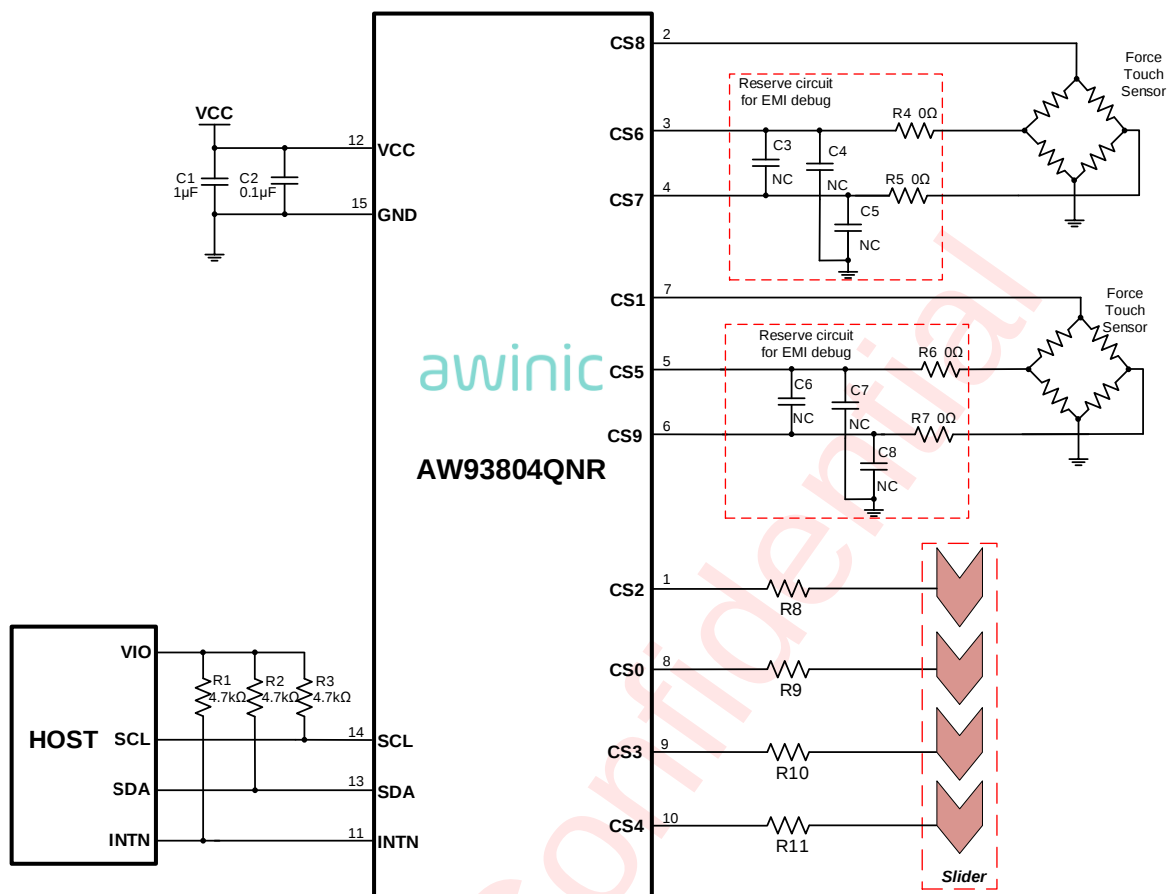


Figure 1 AW93804QNR Typical Application Circuit (force and 1D slide)

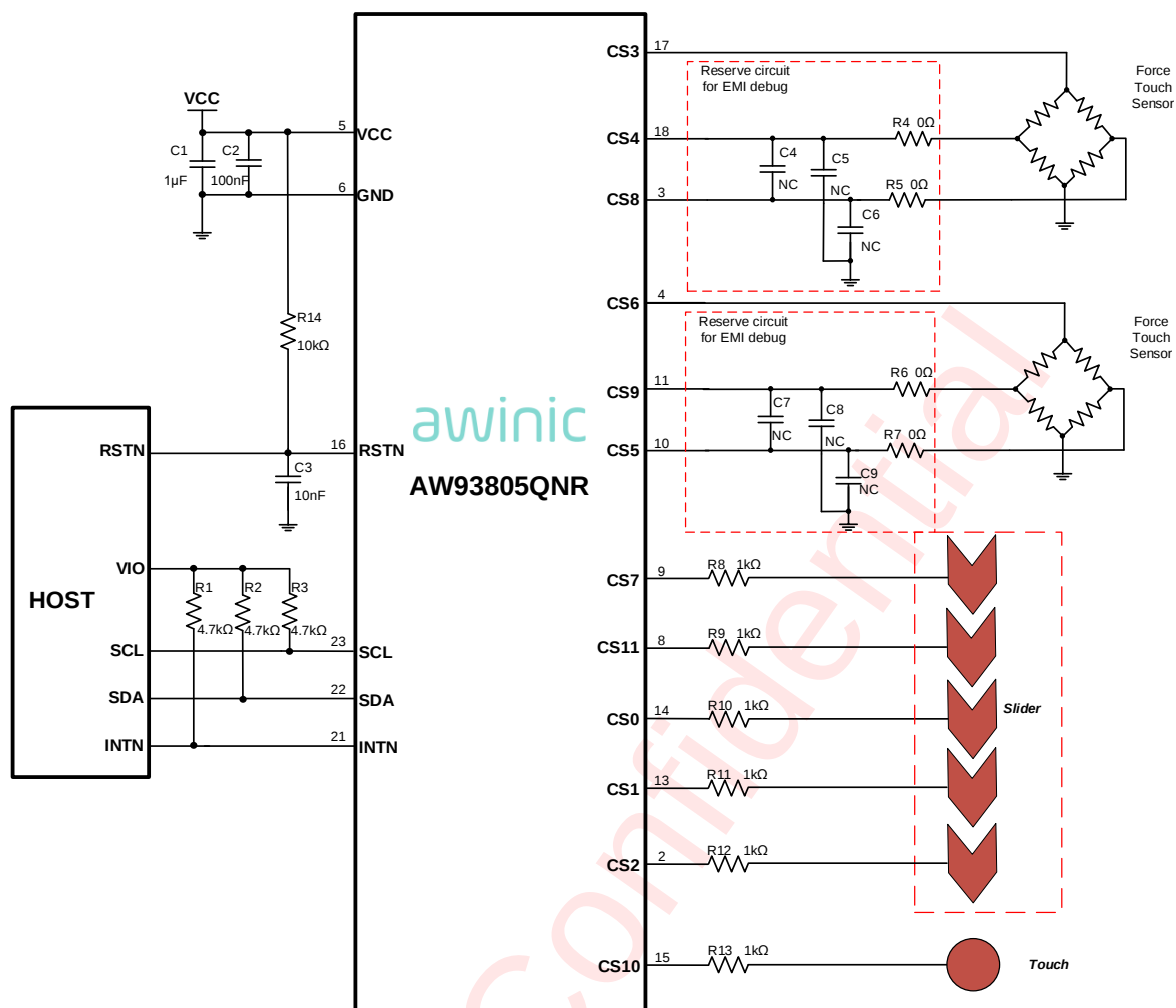


Figure 2 AW93805QNR Typical Application Circuit (force, touch and 1D slide)

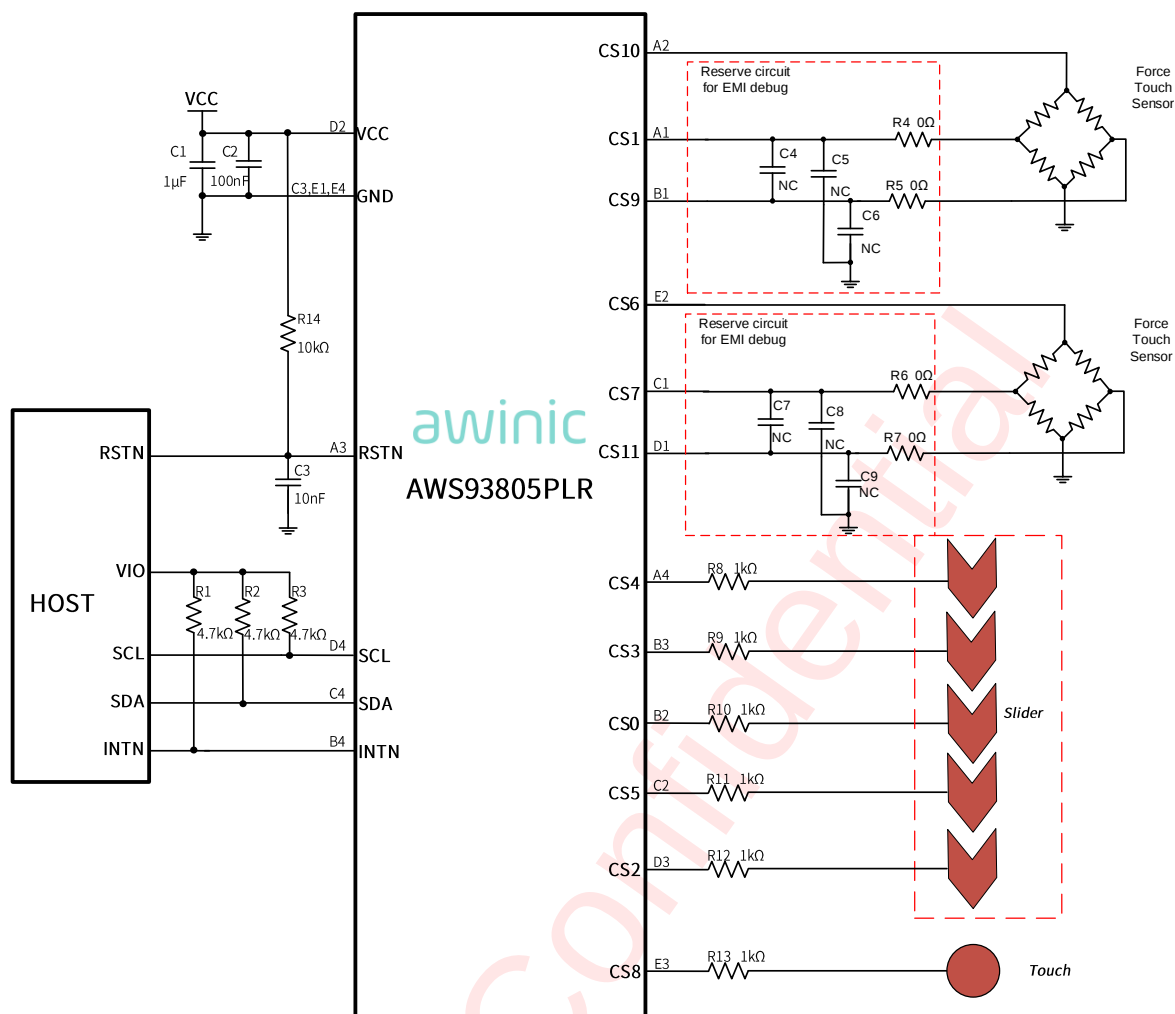
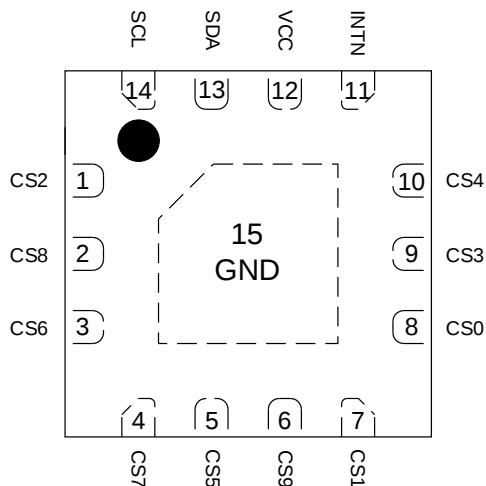
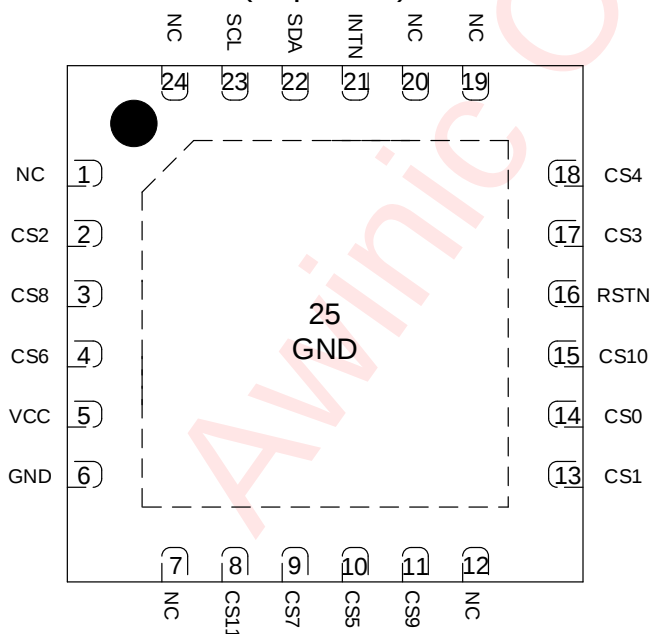
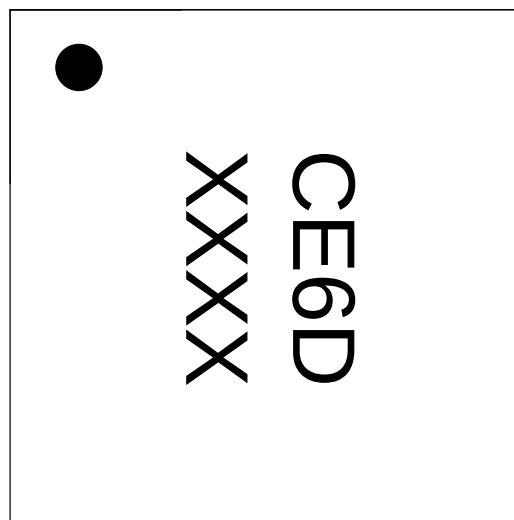


Figure 3 AWS93805PLR Typical Application Circuit (force, touch and 1D slide)

PIN CONFIGURATION AND TOP MARK

AW93804QNR
(Top View)AW93804QNR Marking
(Top View)

YJSG - AW93804QNR
XXXX - Production Tracing Code

AW93805QNR
(Top View)AW93805QNR Marking
(Top View)

CE6D - AW93805QNR
XXXX - Production Tracing Code

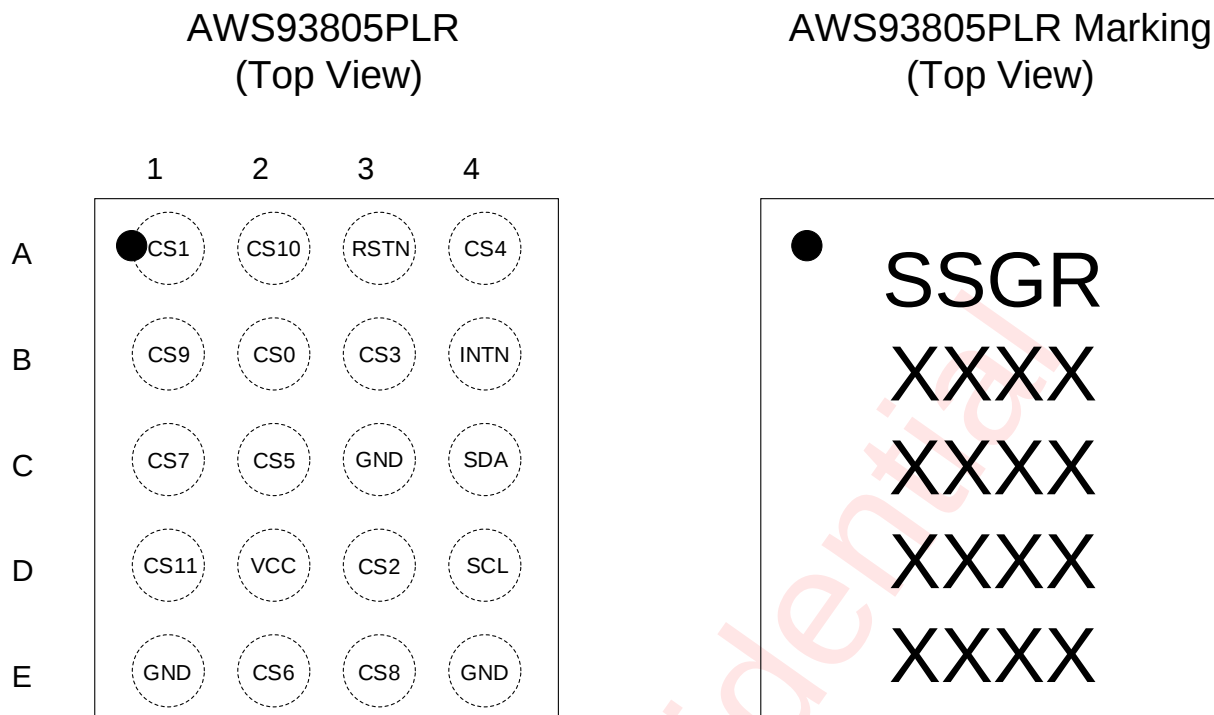


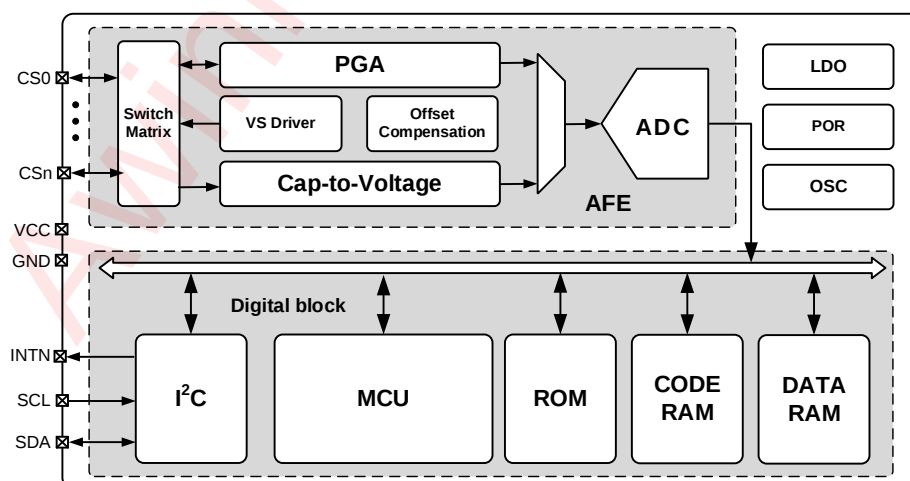
Figure 4 Pin Configuration and Marking

Pin Definition

Name	Pin No.		Description
	AW93805QNR	AW93804QNR	
NC	1,7,12,19,20,24	-	Not connect
CS2	2	1	Capacitive sensor input or I ² C address select input (Floating: 0x12, GND: 0x13, VCC: 0x14)
CS8	3	2	Force sensor input/VS or capacitive sensor input
CS6	4	3	Force sensor input/VS or capacitive sensor input
VCC	5	12	Power supply (1.65V~3.6V), requires decoupling capacitor
GND	6	15	Ground
CS11	8	-	Force sensor input/VS or capacitive sensor input
CS7	9	4	Force sensor input/VS or capacitive sensor input
CS5	10	5	Force sensor input/VS or capacitive sensor input
CS9	11	6	Force sensor input/VS or capacitive sensor input
CS1	13	7	Force sensor input/VS or capacitive sensor input
CS0	14	8	Force sensor input/VS or capacitive sensor input
CS10	15	-	Force sensor input/VS or capacitive sensor input
RSTN	16	-	RESET pin, active low
CS3	17	9	Force sensor input/VS or capacitive sensor input
CS4	18	10	Force sensor input/VS or capacitive sensor input
INTN	21	11	Interrupt output, requires pull-up resistor
SDA	22	13	I ² C data, requires pull-up resistor
SCL	23	14	I ² C clock, requires pull-up resistor
Thermal pad	25	15	Beneath the IC for heat dissipation. Always solder to the PCB ground.

Name	Pin No.	Description
	AWS93805PLR	
CS1	A1	Force sensor input/VS or capacitive sensor input
CS10	A2	Force sensor input/VS or capacitive sensor input
RSTN	A3	RESET pin, active low
CS4	A4	Force sensor input/VS or capacitive sensor input
CS9	B1	Force sensor input/VS or capacitive sensor input
CS0	B2	Force sensor input/VS or capacitive sensor input
CS3	B3	Force sensor input/VS or capacitive sensor input
INTN	B4	Interrupt output, requires pull-up resistor
CS7	C1	Force sensor input/VS or capacitive sensor input
CS5	C2	Force sensor input/VS or capacitive sensor input
GND	C3	Ground
SDA	C4	I ² C data, requires pull-up resistor
CS11	D1	Force sensor input/VS or capacitive sensor input
VCC	D2	Power supply (1.65V~3.6V), requires decoupling capacitor
CS2	D3	Capacitive sensor input or I ² C address select input (Floating: 0x12, GND: 0x13, VCC: 0x14)
SCL	D4	I ² C clock, requires pull-up resistor
GND	E1	Ground
CS6	E2	Force sensor input/VS or capacitive sensor input
CS8	E3	Force sensor input/VS or capacitive sensor input
GND	E4	Ground

Functional Block Diagram



Notes: AFE means Analog Front-End.

Figure 5 AW9380X Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW93804QNR	-40°C~85°C	QFN 2×2-14L	YJSG	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93805QNR	-40°C~85°C	QFN 3×3-24L	CE6D	MSL1	ROHS+HF	6000 units/ Tape and Reel
AWS93805PLR	-40°C~85°C	FOPLP 1.729X1.538-20B	SSGR	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings ^(NOTE2)

PARAMETERS	RANGE
Supply voltage range VCC	-0.5V to 4.0V
Input voltage range (non-supply pins)	-0.5V to VCC+0.3V
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T _{JMAX}	150°C
Storage temperature T _{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including HBM CDM) ^(NOTE3)	
HBM	±8kV
CDM	±1.5kV
Latch-Up	
Test condition: according to JESD78F.02	+IT: 350mA -IT: -350mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The HBM test method of AW93804QNR/AW93805QNR: ESDA/JEDEC JS-001-2017, the CDM test method of AW93804QNR/AW93805QNR: ESDA/JEDEC JS-002-2018. The HBM test method of AWS93805PLR: ESDA/JEDEC JS-001-2024, the CDM test method of AWS93805PLR: ESDA/JEDEC JS-002-2025.

Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Supply voltage	VCC	1.65 ^(NOTE4)	3.6	V
Pull-up voltage	VIO	1.1	3.6	V

Ambient temperature	T _A	-40	85	°C
---------------------	----------------	-----	----	----

NOTE4: Recommend VCC≥1.7V for optimum analog performance.

Electrical Characteristics

Note: Typical values are given for T_A = +25°C, VCC=1.8V unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CHIP CURRENTS						
I _{DEEPSLEEP}	DeepSleep Mode Current	LDO on, OSC off I ² C listening		6.1	15	μA
I _{SLEEP}	Sleep Mode Current	LDO on, OSC on I ² C listening		8.9	18	μA
I _{DOZE}	Doze Mode Current	SCANPERIOD = 400ms FREQ = 100kHz; CDCRES = 6 CVIREF=3 CHEN = b000001 Digital filter features off I ² C listening. No load		10.7	22	μA
I _{ACTIVE}	Active Mode Current	SCANPERIOD = 30ms FREQ = 100kHz CDCRES = 6 CVIREF=3 CHEN = b000001 Digital filter features off I ² C listening. No load		23.5	42	μA
CAPACITANCE SENSING						
C _{RANGE}	Measurement Range		1.1	4.4	19.8	pF
C _{RES}	Measurement Resolution			1		aF
C _{DCEXT}	External DC Cap. to GND per Measurement Phase	One CSx as measured input			220	pF
R _{FILTIN}	Input driving Res		0		15	kΩ
CAPACITANCE AND FORCE SENSING						
N _{BIT}	Measurement Resolution			21		bits
F _{OSC}	Nominal OSC Frequency			8		MHz
F _{Trim}	OSC Trim Accuracy	Around Nominal Value, Ta=25°C, VCC=2.8V	-4		4	%
F _{Temp} ^(NOTE5)	OSC Temp. Dependency	Around Nominal Value, Full Ta range, VCC=2.8V	-1		1	%
F _{VCC} ^(NOTE5)	OSC VCC Dependency	Around Nominal Value, Ta=25°C, Full VCC range	-0.6		0.6	%
F _S	Nominal Sampling Freq	Programmable with FREQ	F _{osc} / 2048		F _{osc} / 32	kHz
I²C INTERFACE						
I _{OL} (SDA, INTN)	Output low current	V _{OL} ≤ 0.4V	8			mA
V _{IH}	Input high level	SCL, SDA	0.9		3.6	V
V _{IL}	Input low level	SCL, SDA	-0.5		0.36	V
t _{DEG_SDA}	SDA deglitch time	SDA		88		ns

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t _{DEG_SCL}	SCL deglitch time	SCL		77		ns
FORCE SENSING						
I _{VSH}	High supply current of VS	VCC=2.8V	8			mA
C _{in}	amplification factor		1		15	
V _S	supply voltage	TA=25°C, No load		VCC		V
PGA	Gain		0.76	$8.8 \cdot (C_{in} + 0.7) / C_{RANGE}$	125	
V _{off_max}	Max Offset voltage	C _{in} =15, VCC=2.8V		1		V

NOTE5: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

I²C Interface Timing

Parameter		Min	Typ	Max	Unit
F _{SCL}	Interface Clock frequency			400	kHz
t _{HD:STA}	(Repeat-start) Start condition hold time	0.6			μs
t _{LOW}	Low level width of SCL	1.3			μs
t _{HIGH}	High level width of SCL	0.6			μs
t _{SU:STA}	(Repeat-start) Start condition setup time	0.6			μs
t _{HD:DAT}	Data hold time	0			μs
t _{SU:DAT}	Data setup time	0.1			μs
t _R	Rising time of SDA and SCL			0.3	μs
t _F	Falling time of SDA and SCL			0.3	μs
t _{SU:STO}	Stop condition setup time	0.6			μs
t _{BUF}	Time between start and stop condition	1.3			μs

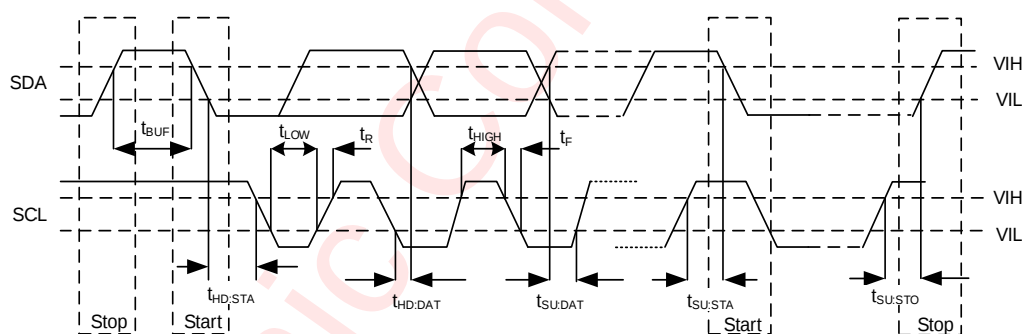


Figure 6 I²C Interface Timing

Detailed Functional Description

Overview

AW9380X is a force and capacitive proximity sensor with a built-in ultra-low-power MCU. It is comprised of high-performance self/mutual capacitance detecting Analog-Front-End (AFE), embedded 32-bit MCU, ROM, RAM, OSC and I²C interface, etc. The AFE drives the sensor electrode, and converts the capacitance of sensor to digital data. The MCU executes the algorithm program stored in ROM or CODERAM, and performs complete data process that contains signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency (RF) noise suppression, proximity decision, force detection, etc.

Force Sensor Introduction

When an object (such as a finger) presses against a pressure detection sensor, a differential voltage is generated between the positive and negative terminals of the sensor. The chip detects this voltage to determine if there is a pressing event.

Capacitive Sensor Introduction

When a conductive object, such as a finger, comes in contact or close proximity with the sensing electrode, the capacitance of one or more sensors changes. The figure 7 shows the basic structure and equivalent model of a capacitive sensor. The top layer is the overlay, and the middle layer which is green is a copper sensor pad. The sensor is usually surrounded by ground with a parasitic capacitance(C_{PARA}).

There are two main operational modes in the capacitance sensing circuits: self-capacitance sensing and mutual capacitance sensing. An electric field is created around the sensor when system is working. In the self-capacitance sensing mode, with target object approaching, some of the electric field lines couple to the target object and a small amount of target object capacitance (C_{PROX}) adds to the existing C_{PARA} . This feature can be used to detect proximity or touch action.

At least two electrodes are needed in the mutual capacitance sensing mode: one is a transmitter (Tx) and the other is a receiver (Rx). Tx and ground will form a capacitance (C_{TX}); Rx and ground will form a capacitance (C_{RX}); Tx and Rx will form a capacitance (C_M). When target object approaches, Tx and Rx will form a capacitance (C_M') which is less than C_M .

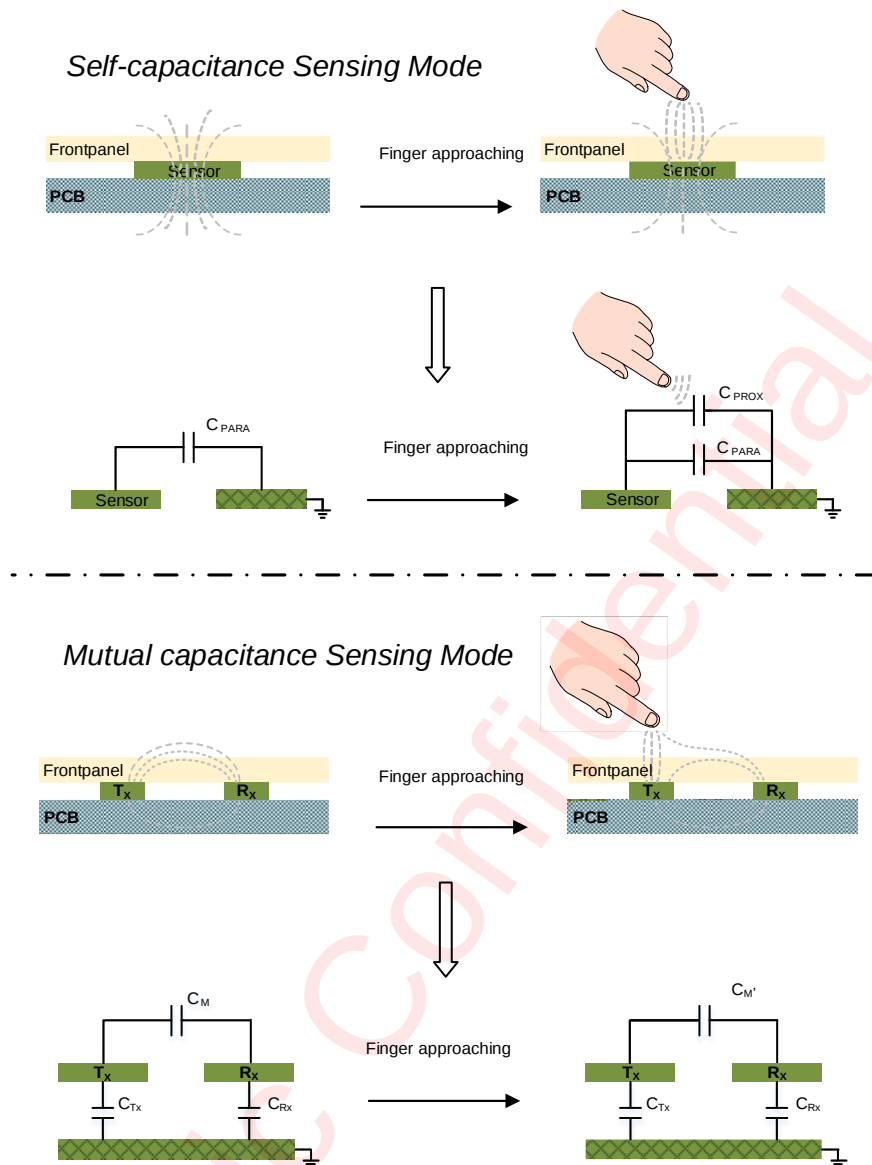


Figure 7 Capacitive Sensor Structure

Force and capacitive Sensing Techniques

The force sensing system consists of three parts: force sensor, AFE, and DSP. The function of AFE is to amplify the force sensor P port and N port voltage and convert the difference voltage to digital data. The function of DSP is to process the data from AFE and transmit calibrated force sensing detection value to the host.

The proximity sensing system consists of three parts: capacitive sensor, AFE and DSP. The function of AFE is to drive the capacitive sensor electrode, and convert the sensor capacitance to digital data. The function of DSP is to process the data from AFE and transmit the sensor capacitance value (*CapDiff*) together with proximity status (*status*) to the Host. When the target object is approaching or moving away, the proximity sensing system will transmit key information to the Host after dedicated processing.

AFE DESCRIPTION

- ※ Block Switch Matrix selects pin CSx as capacitance measurement input, force measurement input or VS(force measurement power supply).

- ※ Block Cap-to-Voltage integrates a charge amplifier which detects the sensor capacitance with a charge-transfer method. The capacitance is converted into a voltage signal, which is the input of block ADC.
- ※ Block Offset Compensation measures parasitic capacitance (C_{PARA}), which is compensated during the process of charge transferring. Thus, the effective input capacitance of Cap-to-Voltage is approximately equal to C_{PROX} .
- ※ ADC converts voltage signals obtained from Cap-to-Voltage or Temp Sensor to digital data (*AdcData*).
- ※ Block PGA integrates a charge amplifier which amplifies the differential output voltage of the resistance bridge and serves as the input of the ADC after amplification.
- ※ Block Offset Compensation measures offset voltage at force mode, which is compensated during the process of charge transferring.

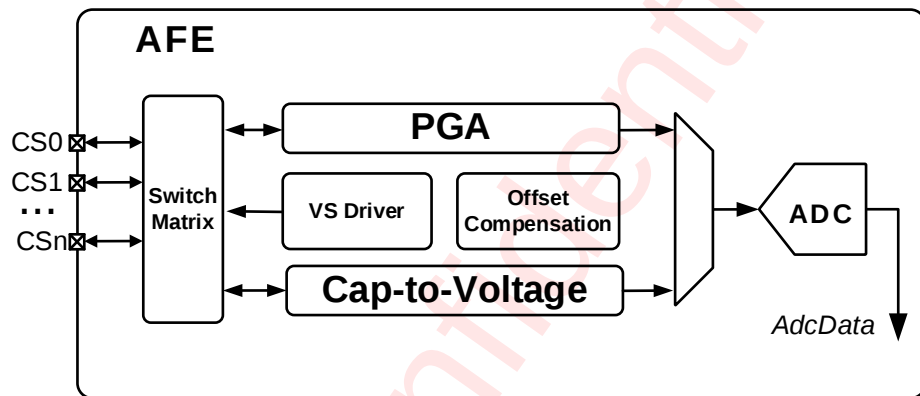


Figure 8 AFE Block Diagram

DSP DESCRIPTION

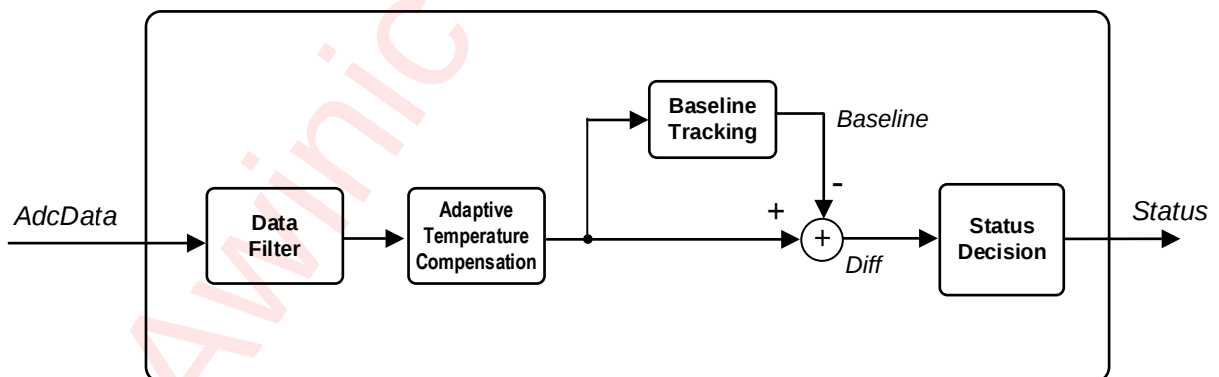


Figure 9 Digital Signal Processing Diagram

- ※ DSP processes the *AdcData* from the AFE, and finally outputs a series of reliable proximity status.
- ※ Data Filter effectively filters the high-frequency noise and interference, which greatly improves the signal-to-noise ratio(SNR).
- ※ Block Adaptive Temperature Compensation can automatically compensate for environmental drift in real time, especially temperature drift. Thereby, the final proximity status will not be misjudged.
- ※ The role of the *Baseline* is to further track the slowly varying data caused by the residual temperature compensation or other gradual environmental drift.

- ※ Finally, block Status Decision outputs a certain and reliable proximity status based on the data *CapDiff* and the proximity threshold.

SCAN PERIOD

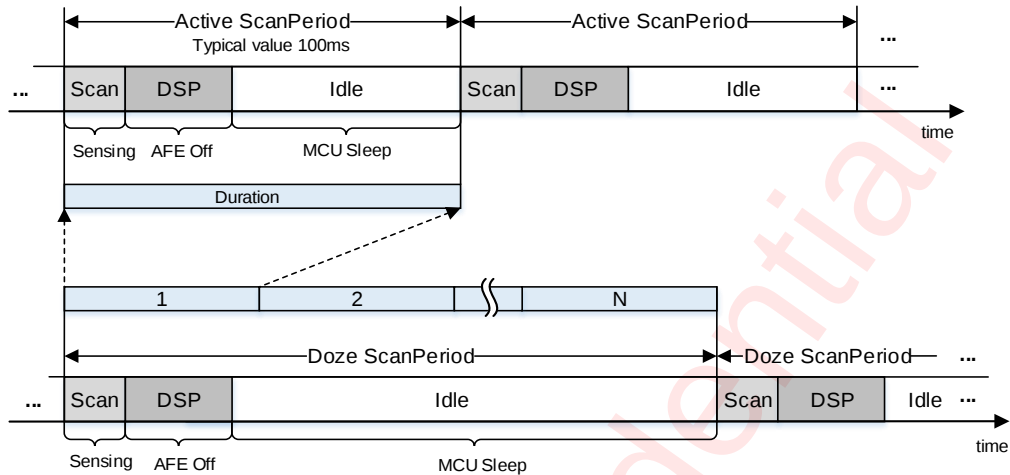


Figure 10 Active Mode and Doze Mode Scan Period

Each scan period can be divided into three stages. In the first stage, the selected sensor channels are scanned and *AdcData* of each channel is generated. In the second stage, the AFE stops working and the DSP begins to process the obtained *AdcData*. In the last stage, all data processing has been completed and the chip enters idle status. In idle status, in order to reduce power consumption, neither AFE nor MCU works.

The figure 10 shows the composition and meaning of the Active mode and Doze mode scan periods. Generally, Doze mode consumes lower power than Active mode.

Reset

POWER ON RESET

The chip of AW93804QNR, When VIO and VCC are powered on. Reset operation is triggered during power up, the initialization process starts to perform and will last for about 20ms. INTN will be set to low when the initialization process is completed, then I²C can communicate normally.

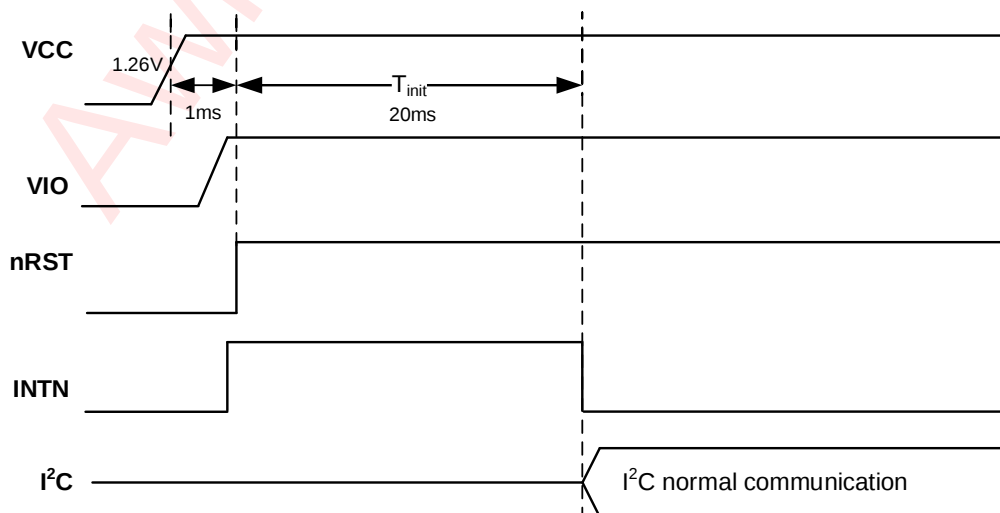


Figure 11 AW93804QNR Power On Timing

The chip of AW93805QNR and AWS93805PLR, When VIO and VCC are powered on. When RSTN signal is high, the initialization process starts to perform and will last for about 20ms. INTN will be set to low when the initialization process is completed, then I²C can communicate normally.

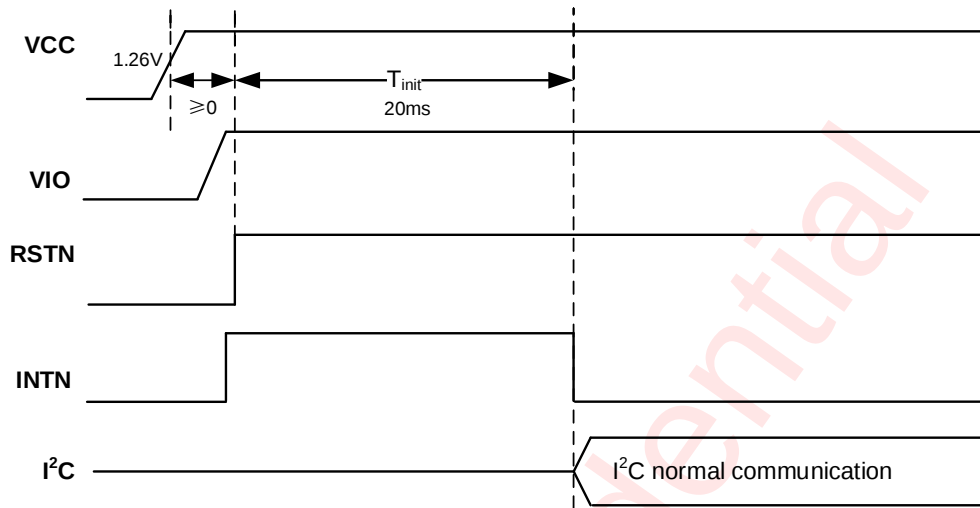


Figure 12 AW93805QNR/AWS93805PLR Power On Timing

SOFT RESET

The soft reset operation can be triggered by writing “0x0” to the soft reset register. After completion of soft reset operation, all the registers will be reset to the default value.

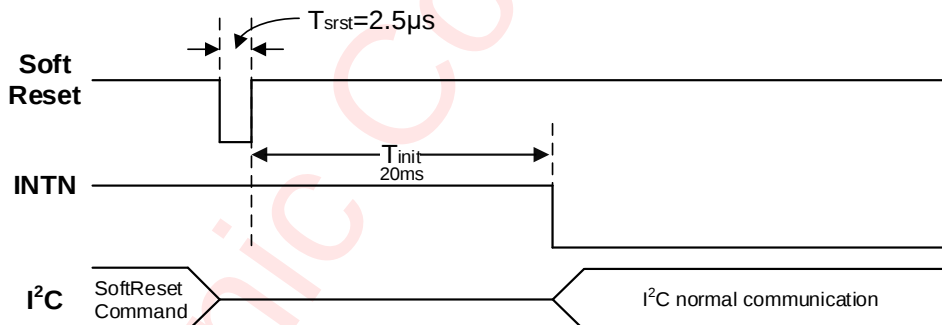


Figure 13 Soft Reset Timing

Clock

The chip uses a built-in 8MHz OSC clock.

Initialization

After power on, first OSC runs, and then MCU starts to execute the initialization process in ROM or RAM. The initialization program contains the following operations.

- Read information from NVM
- Confirm and configure I²C device address according to pin CS2
- Interrupt message is wrote to state register of interrupt
- Enter into Sleep mode

Operation Mode

There are four operation modes in the chip: DeepSleep, Sleep, Active and Doze.

DEEPSLEEP

The chip power consumption is lowest in this mode. OSC, AFE and MCU are inactive, only I²C interface is active.

SLEEP

The chip is in a low power state. AFE and MCU are inactive, OSC is active, waiting for interrupt to wake up.

ACTIVE

The chip works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When touch or proximity has not been detected for a period of time, it will automatically switch to Doze mode. In this mode, the external Host can send Sleep command to switch the chip into Sleep mode.

DOZE

In this mode, MCU and AFE work intermittently with a longer scan period. During large part of a scan period, most modules are inactive. So the average power consumption is lower.

Once proximity is detected in Doze mode, it will automatically return to Active mode. The external Host can also send Sleep command to switch the chip to Sleep mode.

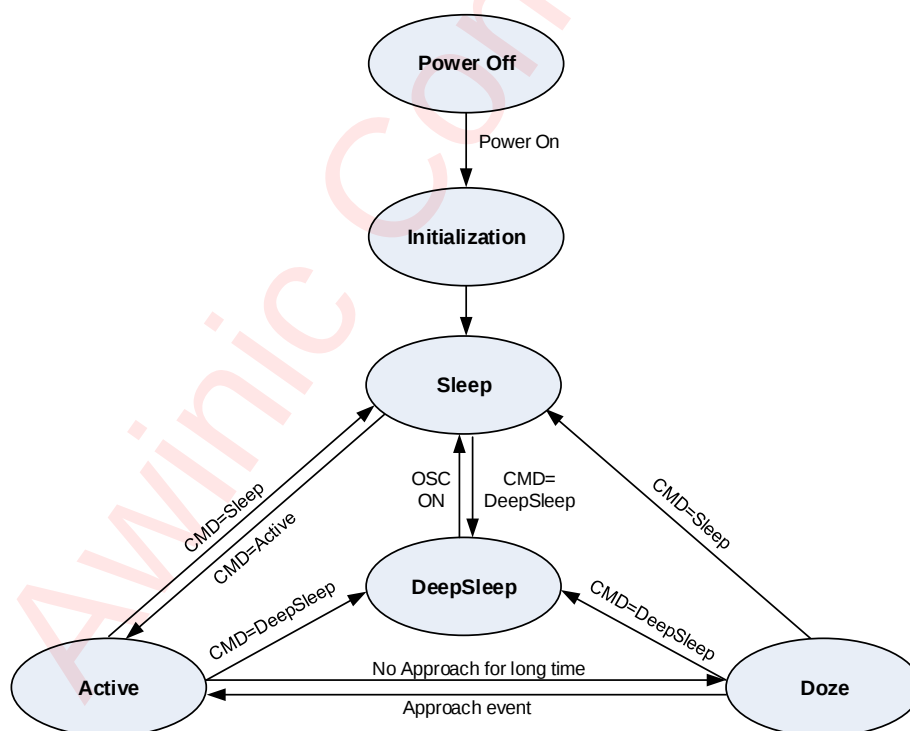


Figure 14 Operation Mode Switching

Interrupt

AW9380X report the interrupt signal to the host through the INTN pin. Register IRQSRC (Address: 0xF080) stores interrupt information, including the completion of parasitic capacitance calibration, scan cycle completion, and so on. Register IRQSRC is cleared after Host read. The specified interrupt signal can be masked by configuring register IRQEN(Address: 0xF084).

I²C Interface

AW9380X supports the serial I²C-bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. The I²C interface supports different pull-up voltage values. Additionally, the I²C device supports continuous read and write operations. The I²C register address is 16-bit and register data is 32-bit, and the data transmission is in big-endian mode.

DEVICE ADDRESS

I²C Device Address Configuration

CS2 Connection	Device Address
Floating	0x12
GND	0x13
VCC	0x14

The I²C device address of AW9380X depends on the status of pin CS2. The default value is 0x12. Connecting pin CS2 to GND or VCC will change the device address as showed in table above. Note that when pin CS2 is connected to GND or VCC, it can't be used as sensor pad. The power supply of the pin of CS2 and the chip power need to use the same power supply.

The CS2 pin should not be used for the force detection input/VS.

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

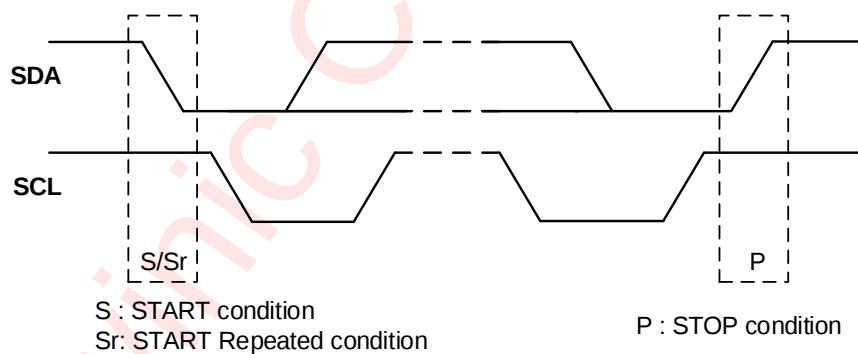


Figure 15 I²C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

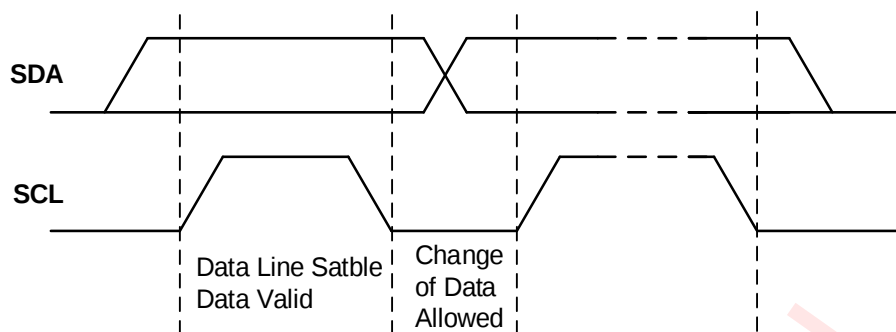
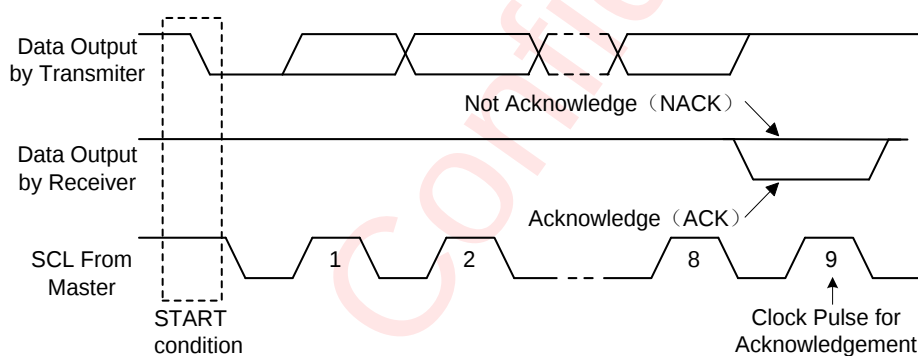


Figure 16 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

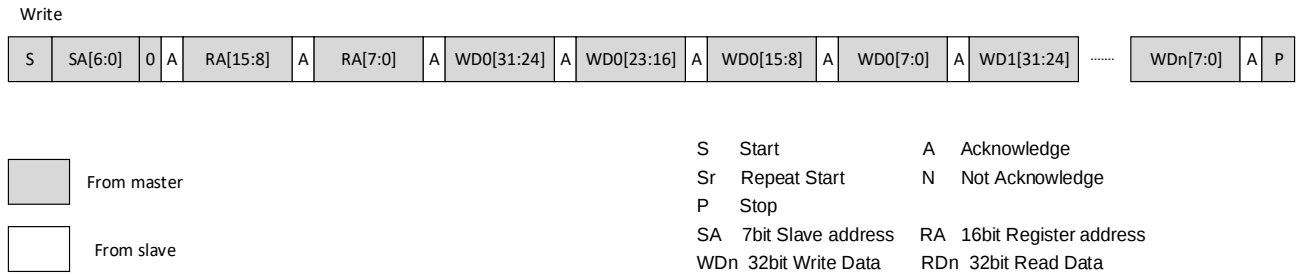
Figure 17 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

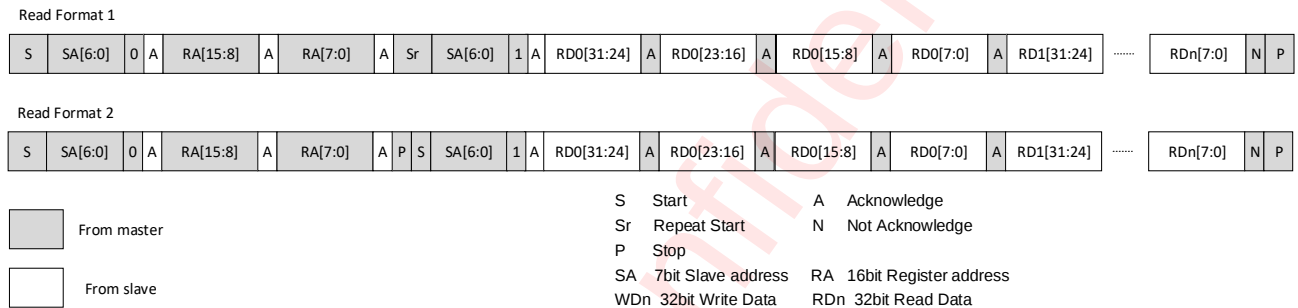
Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 16-bit and register data is 32-bit. Writing process of I²C is shown as figure 18.

Figure 18 I²C Write Byte Cycle

READ CYCLE

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is shown as figure 19.

Figure 19 I²C Read Byte Cycle

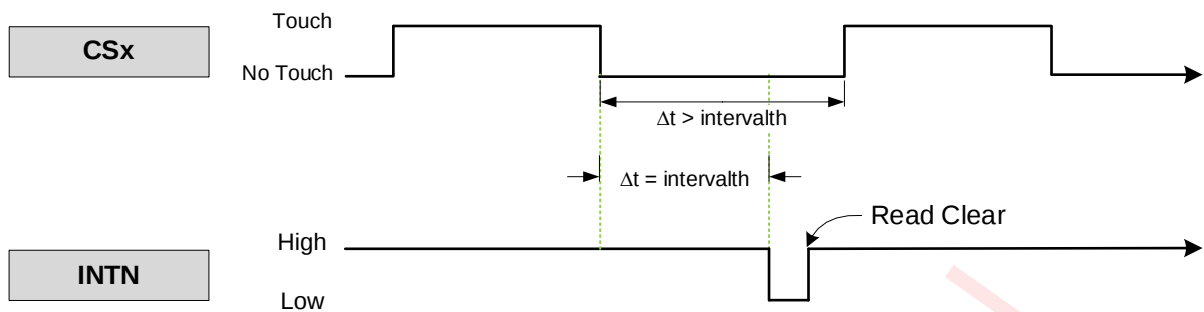
Gestures

AW9380X can implement several gestures on the button and slider, including **single-click**, **double-click**, **triple-click**, **short-press**, **long-press** and **slide**.

Single-click

Single-click refers to a quick tap event, when a touch is triggered and then released in the same location within a short period of time. The *clickth* and *intervalth* threshold can be adjusted according to practical application requirements. **Single-click** event is based on the following condition:

The time between two touch states must be more than the *intervalth*.



Notes:

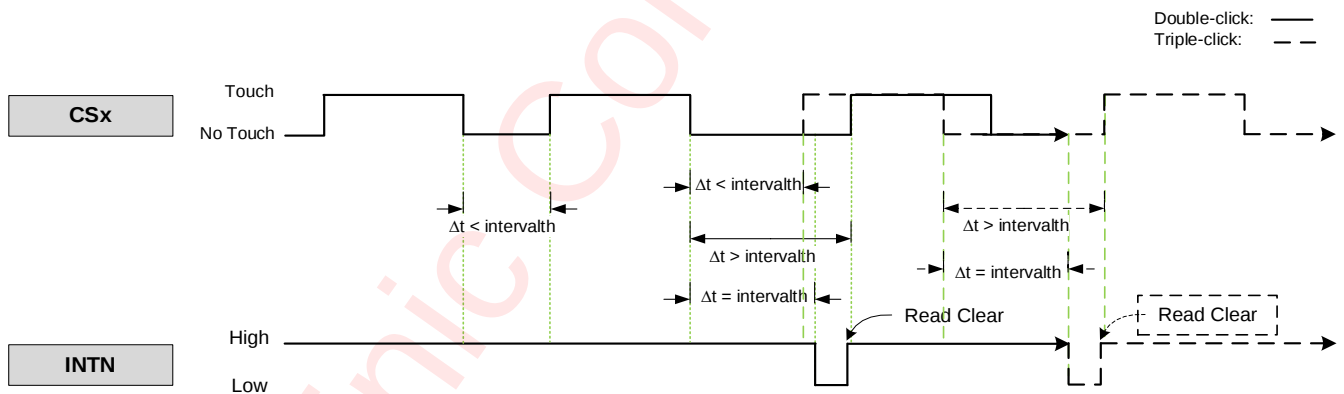
Intervalth: the maximum interval between two valid single-click events

Figure 20 Single-click Sequence Diagram

Double-click and Triple-click

Double-click refers to two quick tap events and **triple-click** refers to three quick tap events. The definition of **triple-click** and **double-click** are different in the number of taps. **Double-click** and **triple-click** events are based on the following condition:

The time between two adjacent touch states must be less than the *intervalth*.



Notes:

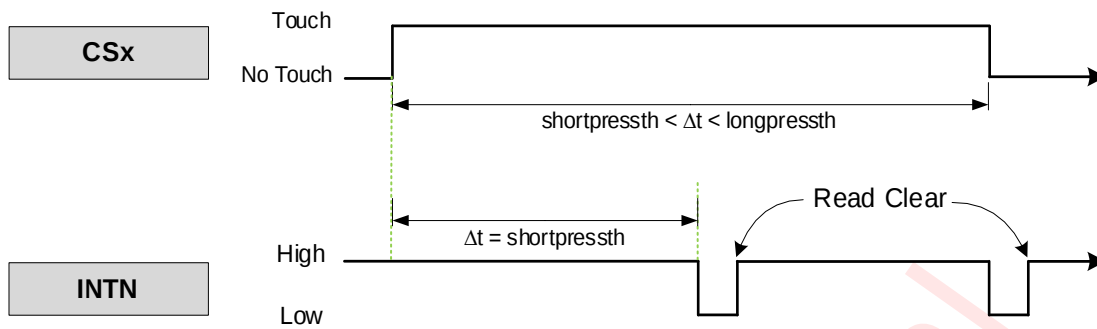
Intervalth: the maximum interval between two valid single-click events

Figure 21 Double-click and Triple-click Sequence Diagram

Short-press

Short-press refers to a short time touch event, **Short-press** gesture is based on the following condition: The time during the touch state must be less than the *longpressth* and more than *shortpressth*.

Short-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch state is released.



Notes:

Shortpressth: the minimum touch time of a short-press event

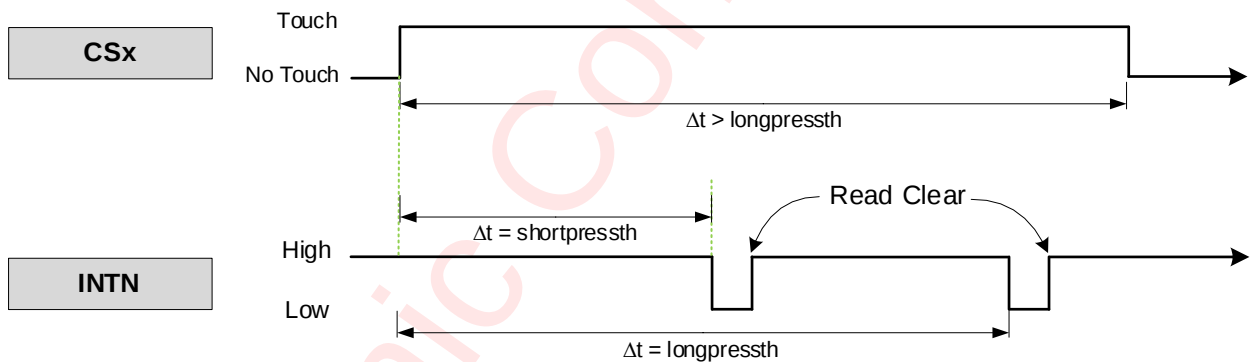
Longpressth: the minimum touch time of a long-press event

Figure 22 Short-press Sequence Diagram

Long-press

Long-press refers to a long time touch event. **Long-press** is based on the following condition: The time during the touch state must be more than the *longpressth*.

Long-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch time reaches the *longpressth* threshold.



Notes:

Shortpressth: the minimum touch time of a short-press event

Longpressth: the minimum touch time of a long-press event

Figure 23 Long-press Sequence Diagram

Slide

Slide is based on the following condition: The coordinate change during the touch state must be more than the *slideth* (the minimum slip distance of a slide event).

A click(or press) is more difficultly recognized as a **slide** with a higher *slideth*. A **slide** is more difficultly recognized as a click(or press) with a lower *slideth*.

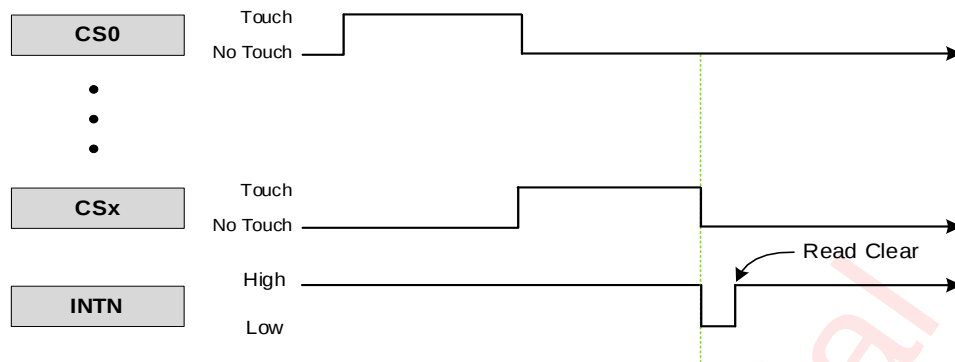


Figure 24 Slide Sequence Diagram

Single sliding definition: The finger touches the slide bar, slide for distance on the slide bar, and the sliding event is reported after the finger leaves.

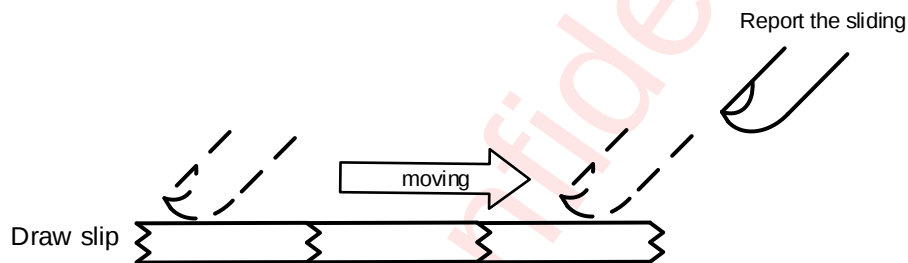


Figure 25 Single Sliding Diagram

Continuous sliding definition: The finger touches the slider without leaving the hand, sliding events will be reported every time the finger slide a certain distance (configurable).

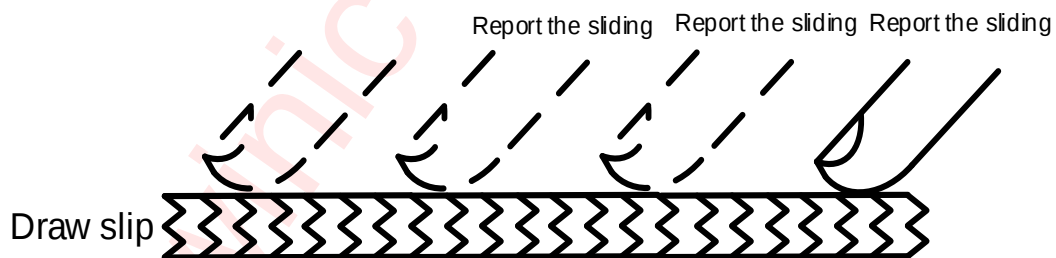
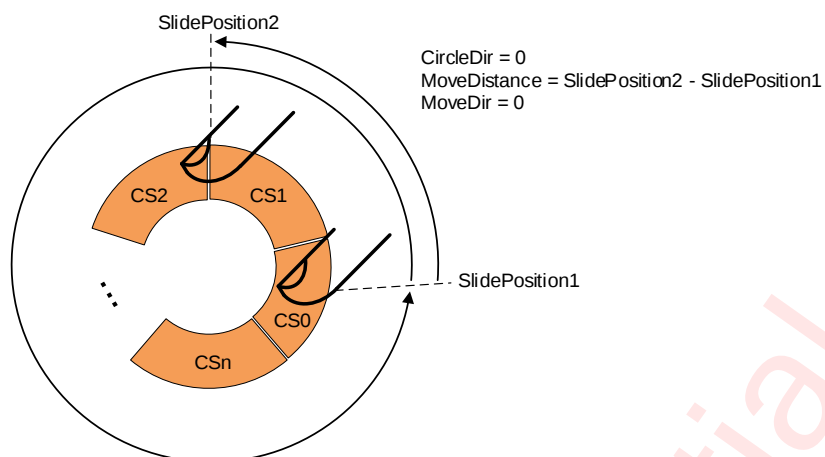
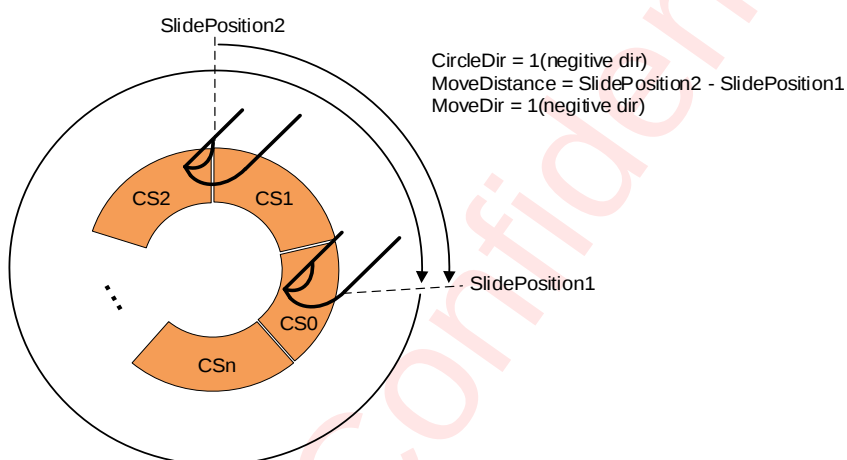


Figure 26 Continuous Sliding Diagram

The parameters of wheel sliders include **SlidePosition**, **MoveDistance**, **MoveDir**, and **CircleDir**. **SlidePosition** means the touch position; **MoveDistance** means the distance between the start position and the end position; **MoveDir** means the relationship between the start position and the end position of the slide; **CircleDir** means the direction of the sliding number of turns, such as counterclockwise or clockwise.

**Figure 27 Counterclockwise Diagram****Figure 28 Clockwise Diagram**

2D slider can report the event of sliding action in four directions, real time coordinates of sliding, move distance which means the distance between the start position and the end position.

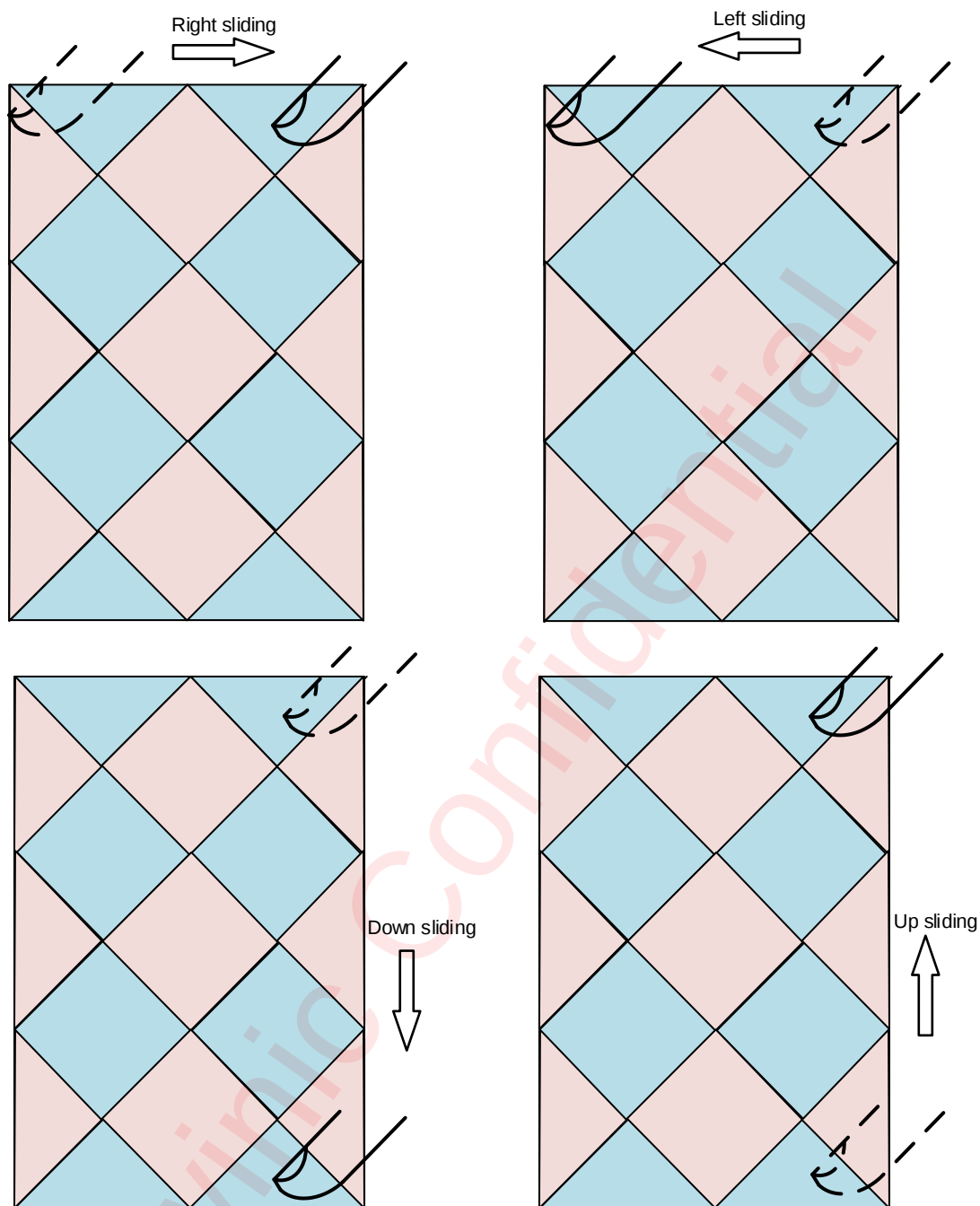


Figure 29 2D Sliding Diagram

Application Information

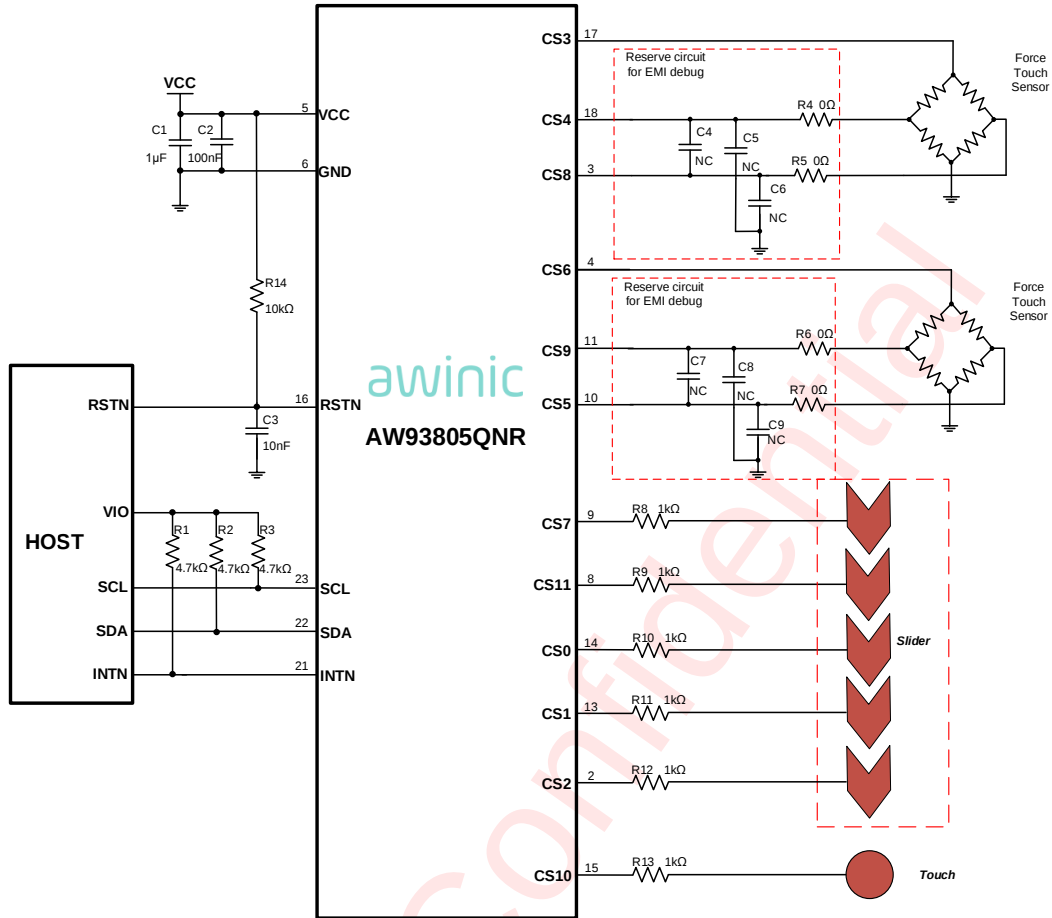


Figure 30 AW93805QNR Typical Application Circuit (force, touch and 1D slide)

Capacitors Selection

The recommended value of the capacitance C1 is 1μF, C2 is 0.1μF and C3 is 10nF.

Resistor Selection

The recommended values of the resistor R1~R3, which were applied in pin INTN, SDA and SCL, are 4.7kΩ.

The recommended values of the resistor R4~R7, C4~C9, which were applied in force detection channels, the value is based on the actual application circuits.

The recommended values of the resistor R8~R13, which were applied in capacitor detection channels, are 1kΩ.

The recommended values of the resistor R14, which is a pull-up resistor applied to RSTN signal, is 10kΩ.

Recommended Components List

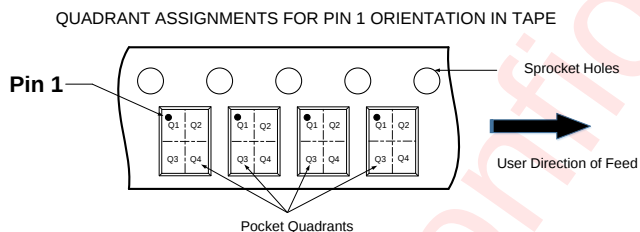
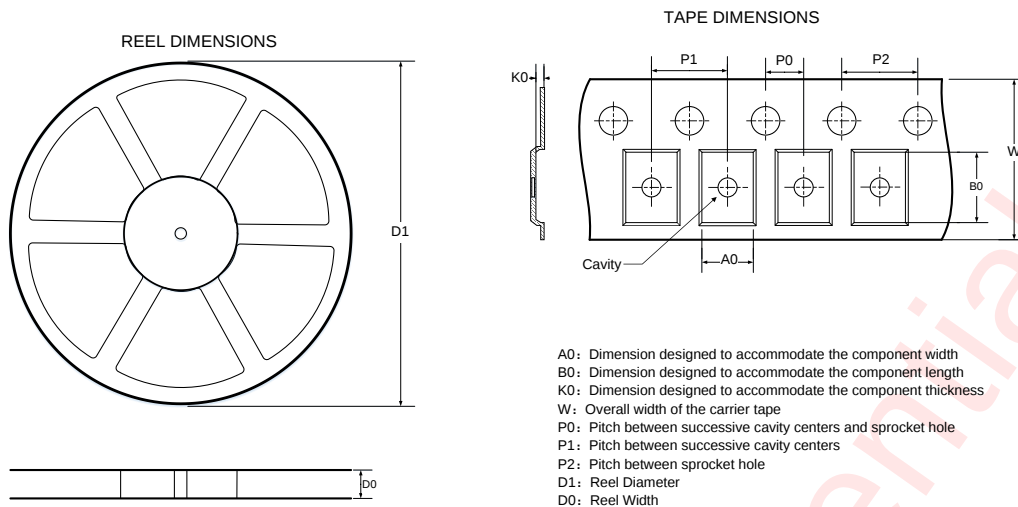
Component	Name	Description	Typ.	Unit
C	C1	-	1	μF
	C2	-	0.1	μF
	C3	-	10	nF
R	R1~R3	$\pm 5\%$	4.7	k Ω
	R8~R13	$\pm 5\%$	1	k Ω
	R14	$\pm 5\%$	10	k Ω

PCB Layout Consideration

AW9380X is a force and capacitive sensor. To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC.
2. Place the chip close to capacitive sensor and make trace as short as possible.
3. Make sure the sensor and traces be away from mic, earphone line in case of disturbing audio line.
4. Place differential channel (in Figure 30, pins CS4, CS8 and CS9, CS5 as shown) along with sensor channel to get better performance.
5. Force detection channel and In-ear detection channel is recommended to use the differential lines.
6. Use LDO for VCC supply.

Tape And Reel Information

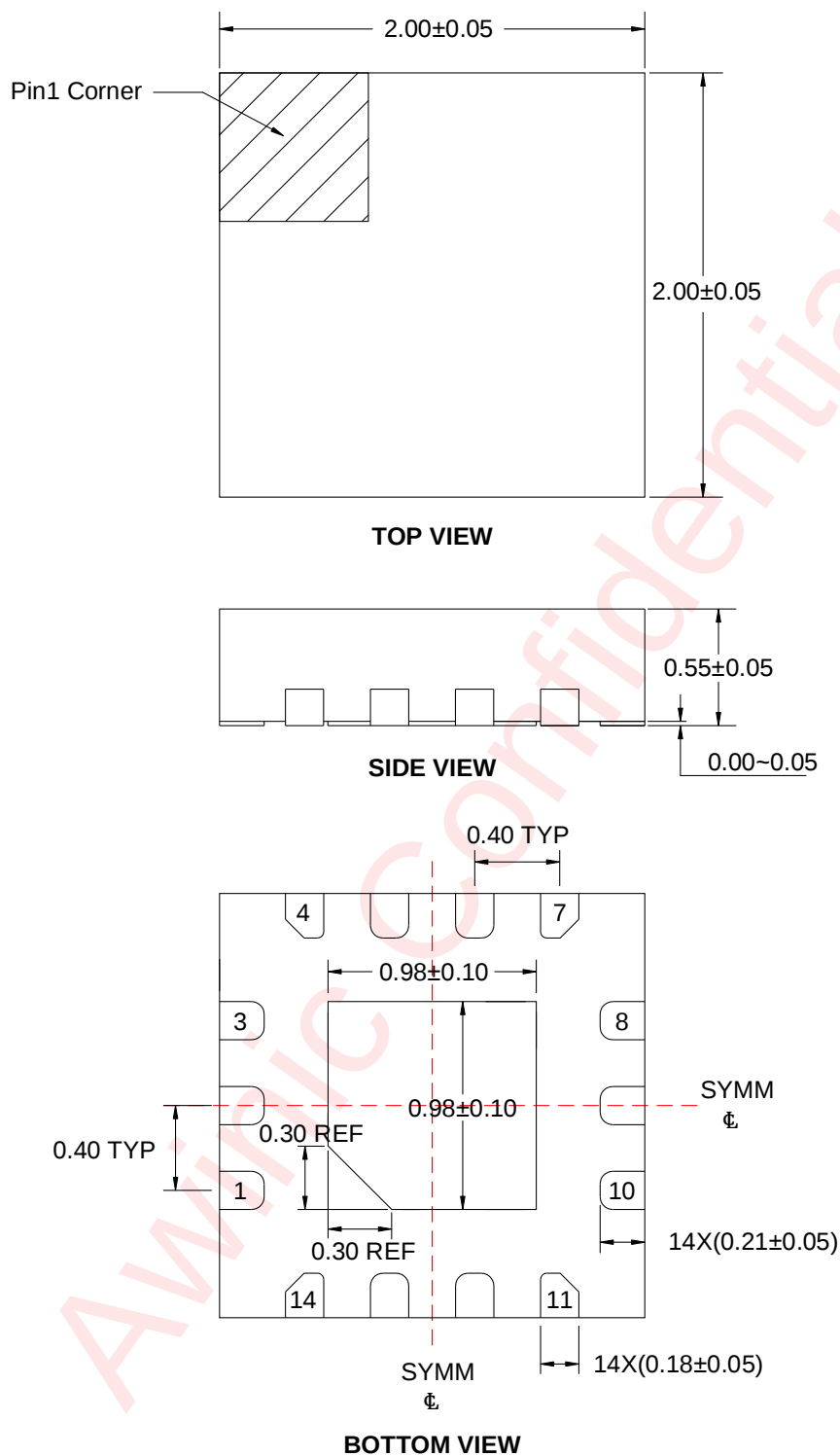


Note: The above picture is for reference only. Please refer to the value in the table below for the actual size DIMENSIONS AND PIN1 ORIENTATION

Device Name	D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
AW93804QNR	178.0	8.40	2.25	2.25	0.75	2.00	4.00	4.00	8.00	Q1
AW93805QNR	330.0	12.40	3.25	3.25	0.75	2.00	8.00	4.00	12.00	Q1
AWS93805PLR	182.0	8.50	1.80	2.05	0.78	2.00	4.00	4.00	8.00	Q1

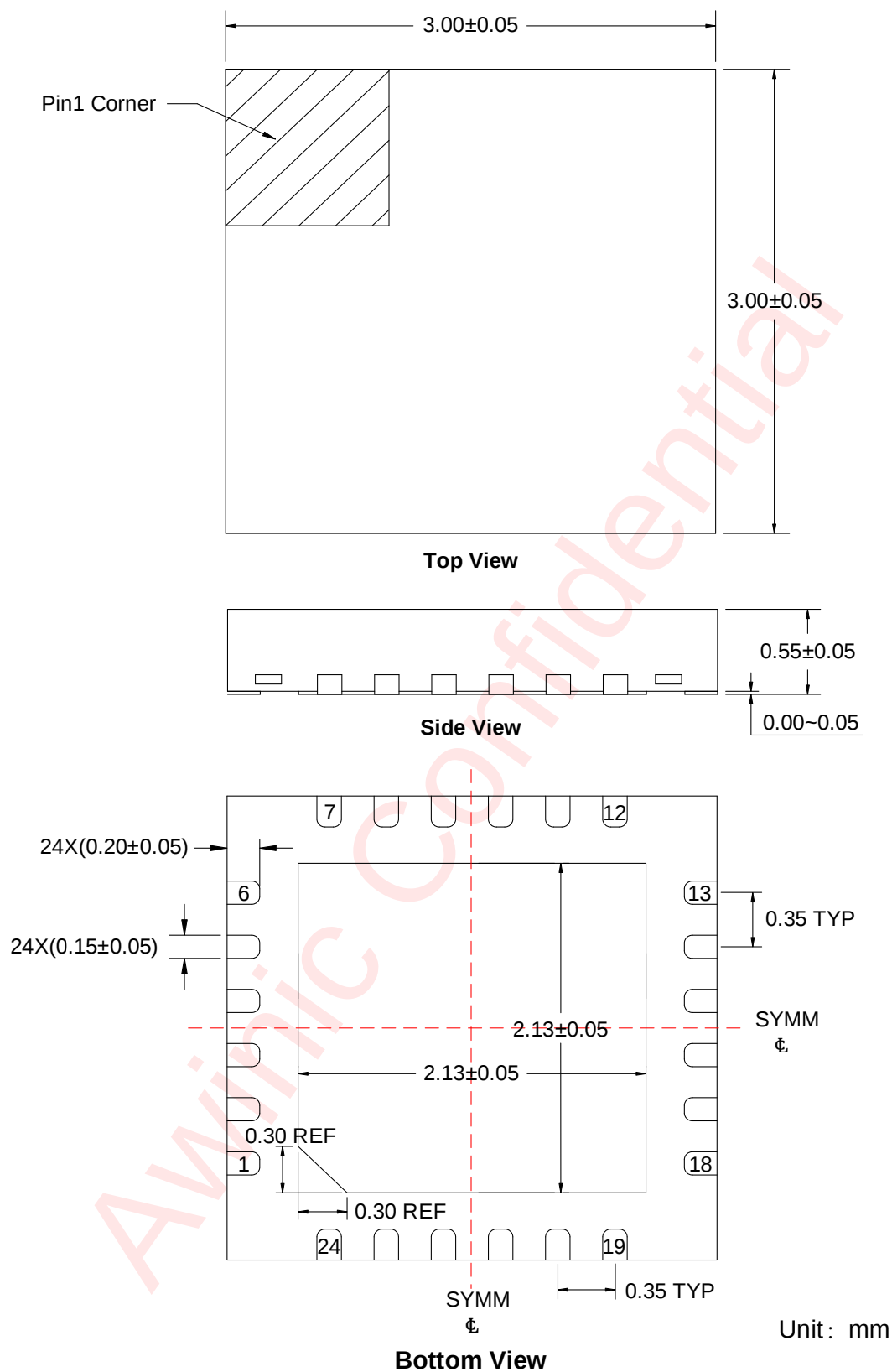
All dimensions are nominal

Package Description

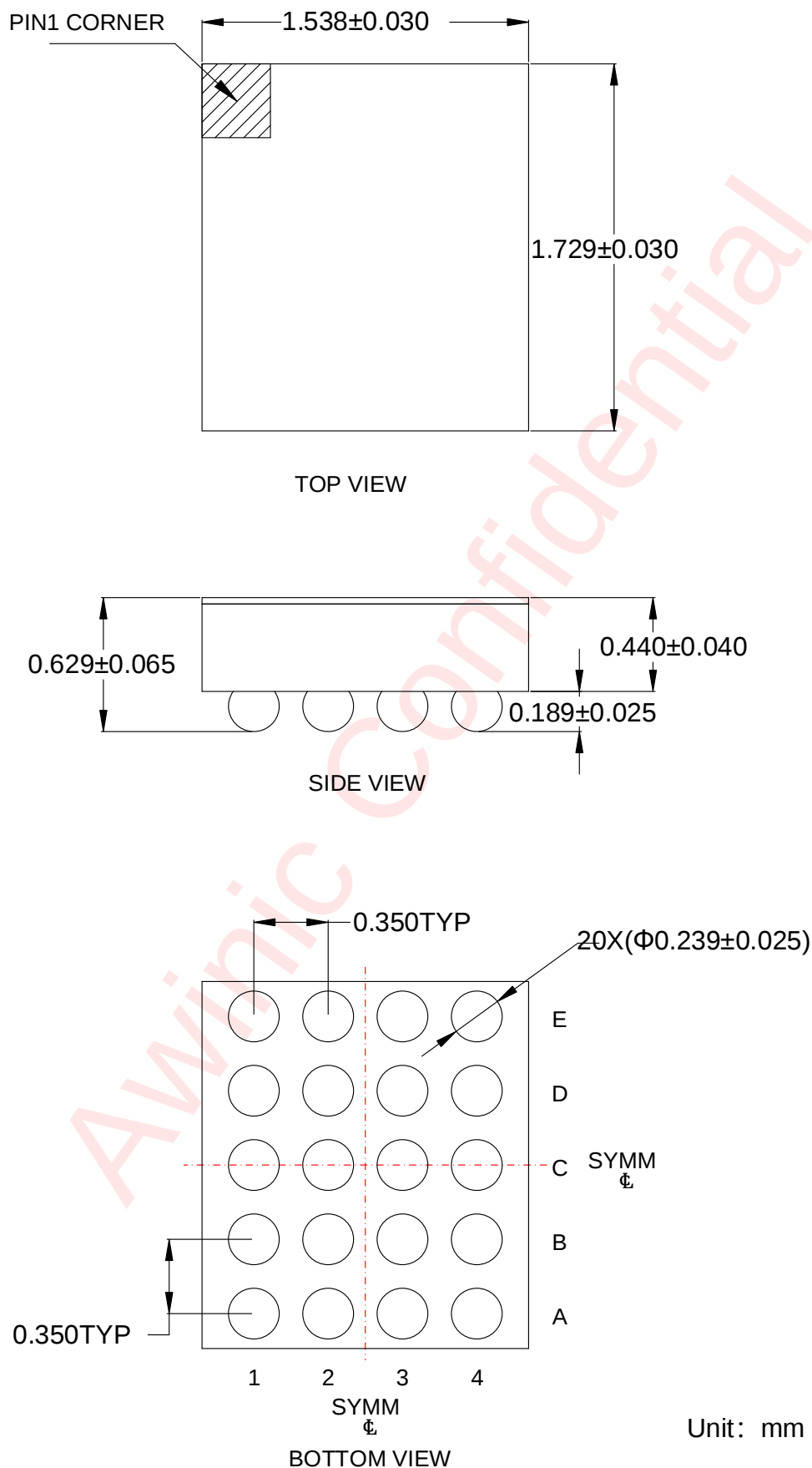


Unit: mm

AW93804QNR Package Description

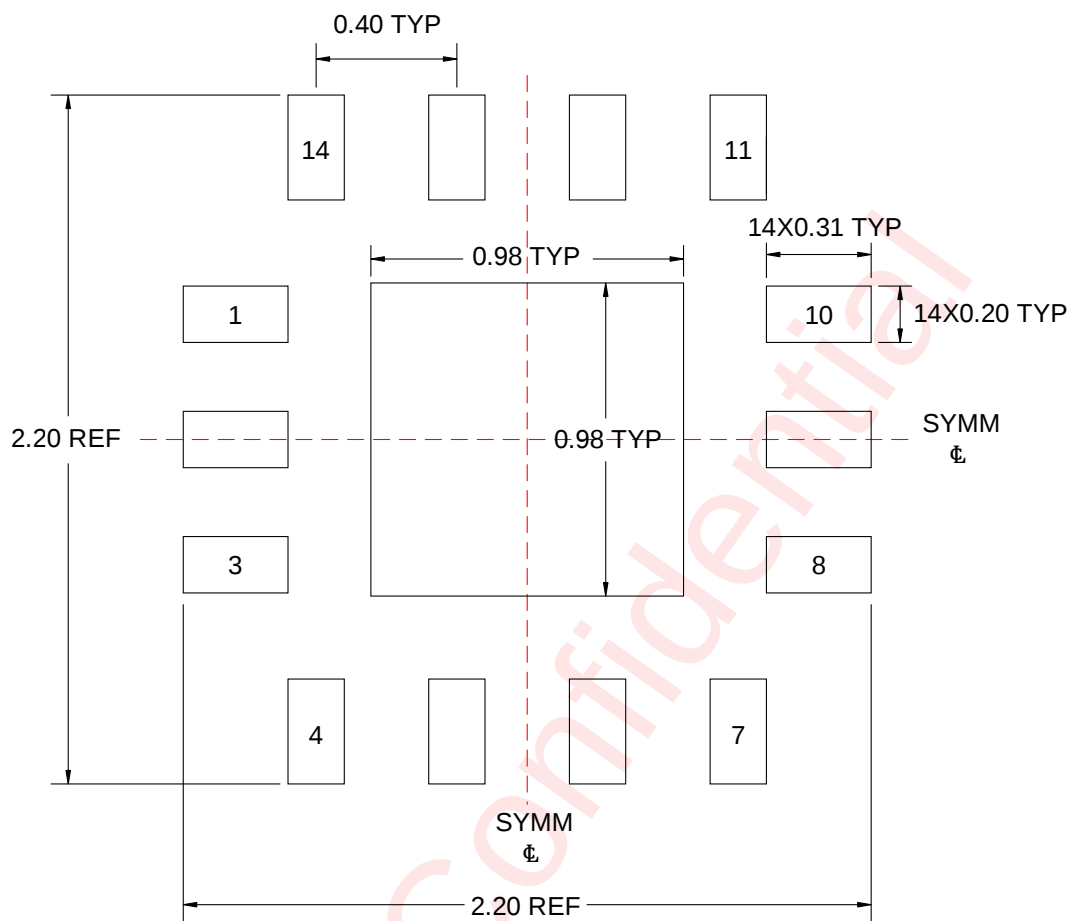


AW93805QNR Package Description

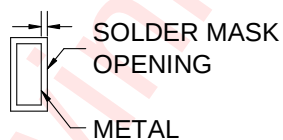


AWS93805PLR Package Description

Land Pattern Data

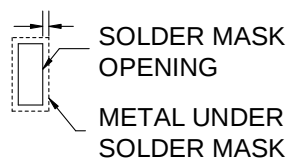


0.05 MAX
All AROUND



NON-SOLDER MASK DEFINED

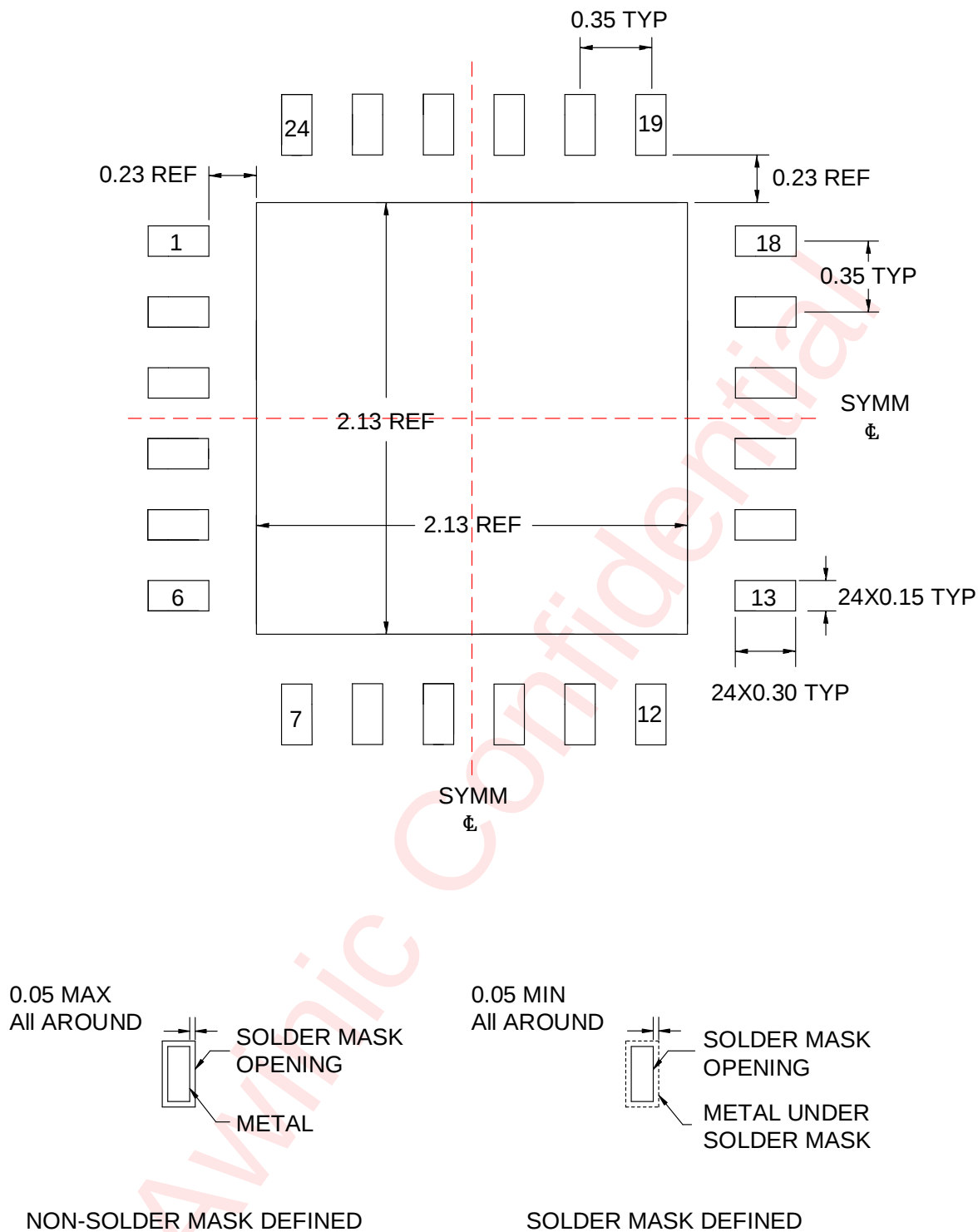
0.05 MIN
All AROUND



SOLDER MASK DEFINED

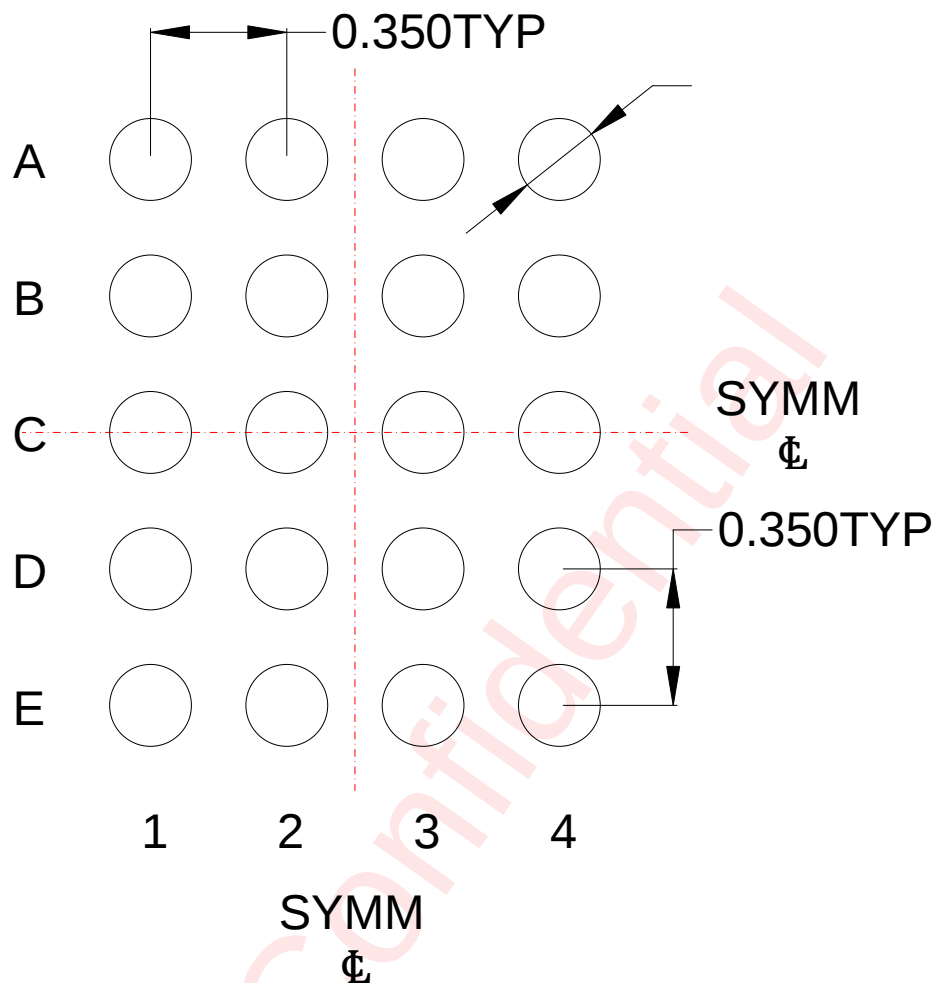
Unit: mm

AW93804QNR Land Pattern

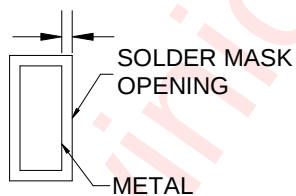


Unit: mm

AW93805QNR Land Pattern

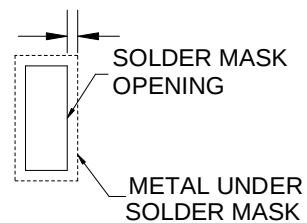


0.05 MAX
All AROUND



NON SOLDER MASK DEFINED

0.05 MIN
All AROUND



SOLDER MASK DEFINED

Unit: mm

AWS93805PLR Land Pattern

Revision History

Version	Date	Change Record
V0.9	Sep. 2023	Initially released.
V1.0	Sep. 2024	Officially released.
V1.1	Nov. 2024	1 Add the AW93804QNR. 2 Update the electrical characteristics of the force. 3 Update the Power On Timing of AW93805QNR
V1.2	Feb. 2025	1 Correct the Pin Definition. 2 Update the functional block diagram and related description.
V1.3	Jul. 2025	1 Modify package description. (P7) 2 Update the Pin Configuration and Pin Definition. (P4 and P5)
V1.4	Nov.2025	Add the AWS93805PLR

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.